Design Example Report

Title	***4.8W Charger using LNK520P***
Specification	Input: 85 – 265 VAC 50/60Hz Output: 12V / 400mA
Application	UPS Battery Charger
Author	Power Integrations Applications Department
Document Number	DER-56
Date	April 20, 2005
Revision	1.0

Summary and Features

- Low component count battery charger to replace linear transformer and regulator
- Highly efficient operation
- Current limited output
- Optimized switching characteristics minimizes EMI
  - Achieves greater than 8dBµV margin to composite conducted limits
  - No Y1 safety capacitor required for EMI compliance
- Small low cost EE16 transformer

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is an engineering prototype report describing a +12V 400mA charger power supply. The power supply utilizes the LinkSwitch LNK520 device. The LinkSwitch integrates a 700V MOSFET, PWM controller, high-voltage start-up, thermal shutdown, and fault protection circuitry. This power supply is a cost effective replacement of linear transformer based power supplies with the additional features of universal input voltage range and high-energy efficiency.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.6	W	
Output						
Output Voltage 1	V_{OUT1}		12		V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$				mV	20 MHz bandwidth
Output Current 1	I_{OUT1}		400		mA	
Total Output Power						
Continuous Output Power	P_{OUT}			4.8	W	
Peak Output Power	P_{OUT_PEAK}			4.8	W	
Efficiency	η	75			%	Measured at P_{OUT} (4.8 W), 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge			TBD		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Surge			TBD		kV	100 kHz ring wave, 500 A short circuit current, differential and common mode
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

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3 Schematic

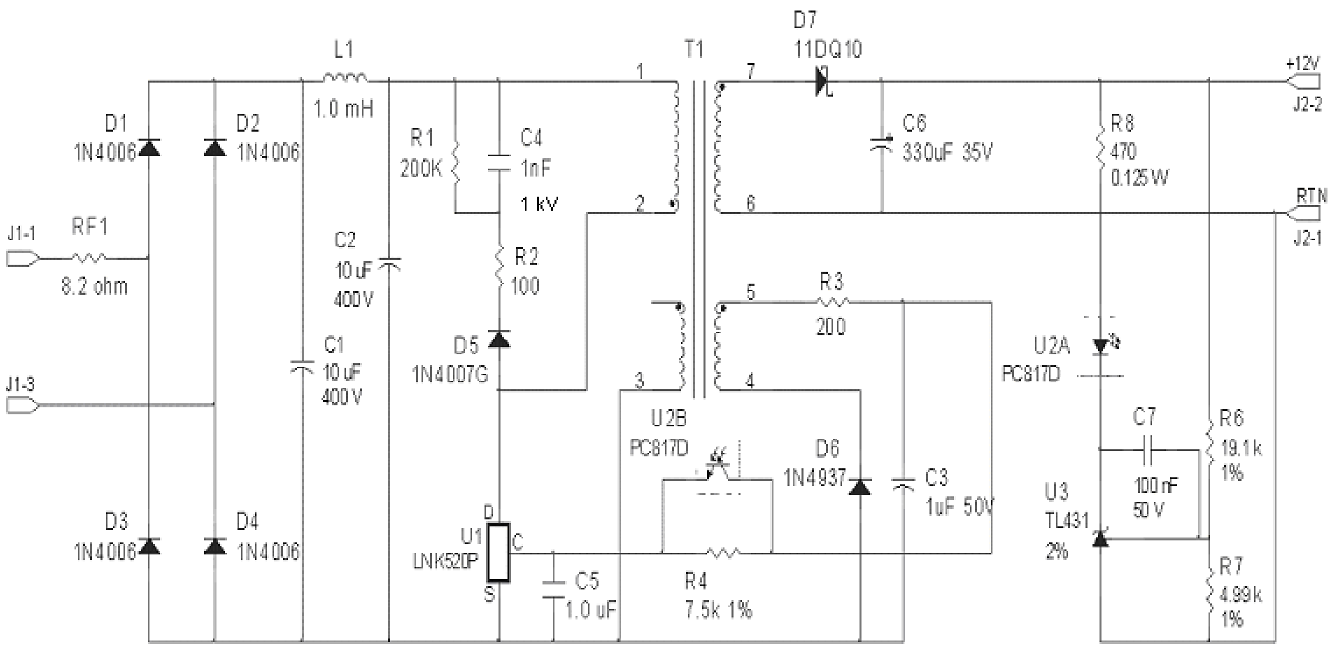

Figure 2 – Schematic

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4 Circuit Description

The circuit schematic shown in Figure 2 shows a design that provides a constant voltage / constant current (CV/CC) output characteristic from a universal input voltage range of 85 VAC-265 VAC. This design delivers 4.8 W with nominal peak power point voltage of 12 V and a current of 400mA.

4.1 Input EMI Filtering

The bridge rectifier, D1-D4, rectifies the AC input and is smoothed by C1 and C2, with inductor L1 forming a π-filter to attenuate differential mode conducted EMI. Resistor RF1 is a fusible, flameproof type, providing protection from primary-side short circuits and line surges and provides additional differential EMI filtering. The switching frequency of 42kHz allows a simple EMI filter to be used without the need for a Y capacitor while still meeting international EMI standards.

Capacitors C1 and C2 are sized to maintain a minimum DC voltage of around 127 V at the minimum AC input voltage. Their ESR should also be as low as possible to reduce differential mode EMI generation. The value of L1 is selected to give acceptable differential mode EMI attenuation with a current rating to meet the RMS input current at low line (or acceptable temperature rise). Conducted emissions in this design are compliant with EN55022B / CISPR 22B and FCC B limits with no input Y1 safety capacitor.

4.2 LinkSwitch Primary and Output Feedback

The LNK520P contains the necessary functions to implement start-up and auto-restart (output protection) operation, output constant voltage (CV) and constant-current (CC) control.

When power is applied, high voltage DC appears at the DRAIN pin of *LinkSwitch* (U1). The CONTROL pin capacitor C5 is then charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin reaches approximately 5.6 V relative to the SOURCE pin, the internal current source is turned off. The internal control circuitry is activated and the high voltage MOSFET starts to switch, using the energy in C5 to power the IC.

Diode D6 rectifies the output of the bias winding, which is then smoothed by C3 to provide a DC voltage to be fed to the CONTROL pin via R4. Resistor R3 is added to filter noise due to leakage inductance. The value of R4 is set such that, at the peak power point, where the output is still in CV regulation, the CONTROL pin current is approximately 2.2mA.

As the output load is increased, the peak power point (defined by $0.5 \times L \times I^2 \times f$) is exceeded. The output voltage and therefore primary side bias voltage reduce. The reduction in the bias voltage results in a proportional reduction of CONTROL pin current, which lowers the internal *LinkSwitch* current limit (current limit control).

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Constant current (CC) operation controls secondary-side output current by reducing the primary-side current limit. The current limit reduction characteristic has been optimized to maintain an approximate constant output current as the output voltage and bias voltage is reduced.

If the load is increased further and the CONTROL pin current falls below approximately 0.8mA, the CONTROL pin capacitor C5 will discharge and *LinkSwitch* will enter auto-restart operation.

Current limit control removes the need for any secondary-side current sensing components. Removing the secondary sense circuit dramatically improves efficiency, giving the associated benefit of reduced enclosure size.

Diode D5, C4, R1, and R2 form the primary clamp network. This limits the peak DRAIN voltage due to leakage inductance. Resistor R2 allows the use of a slow, low cost rectifier diode by limiting the reverse current through D5 when U1 turns on. The selection of a slow diode improves radiated EMI and also improves CV regulation, especially at no load. A glass passivated diode should be used with specified recovery time.

4.3 Output Rectification

Output rectification is provided by Schottky diode D7. The low forward voltage provides high efficiency across the operating range. Low ESR capacitor C6 achieves minimum output ripple and maximizes operating efficiency.

4.4 Output Feedback

Resistors R6 and R7 divide down the supply output voltage and apply it to the reference pin of error amplifier U3. Shunt regulator U3 drives Optocoupler U2 through resistor R8 to provide feedback information to the U1 CONTROL pin. Capacitor C7 rolls off the gain of U3 and is sufficient to compensate the control loop of the power supply.

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5 PCB Layout

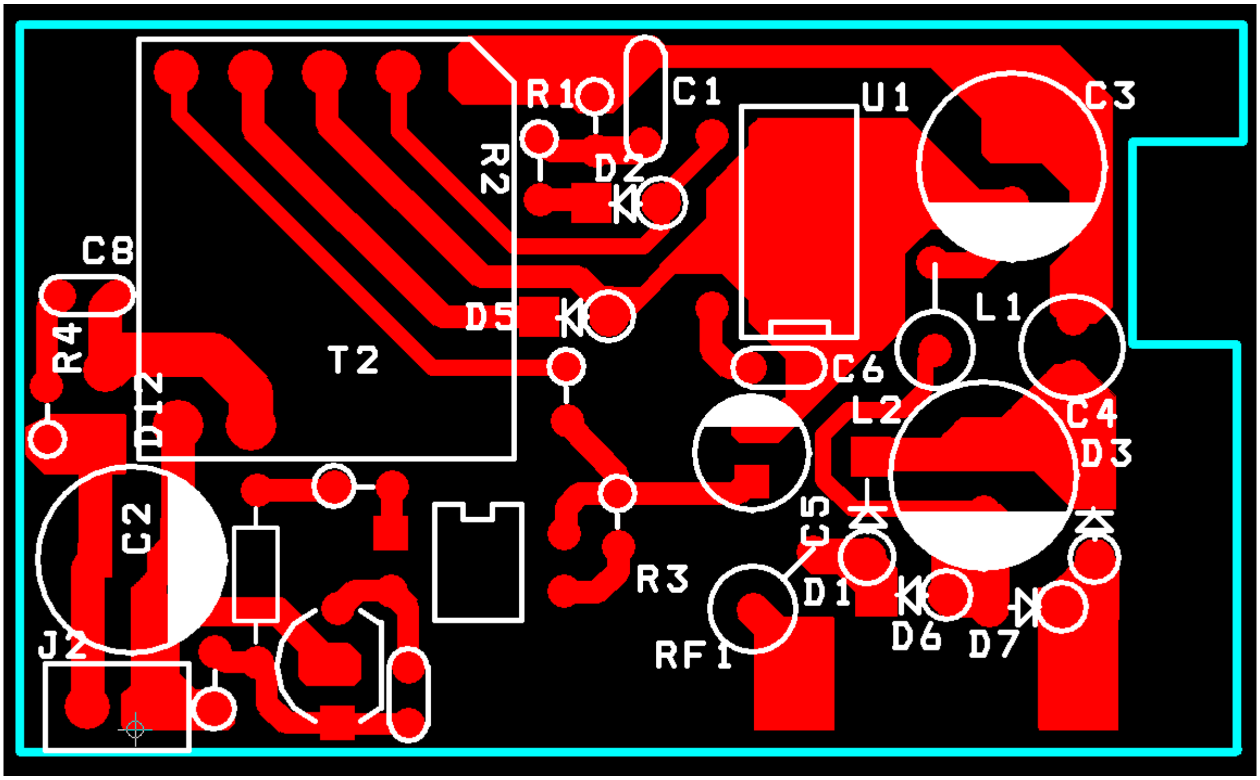

Figure 3 – Printed Circuit Layout

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6 Bill Of Materials

Item	*QTY*	*Ref Des*	*Description*	*Manufacturer*	*Mfg Part Number*
1	2	C1 C2	10uF, 400 V, Electrolytic, Low ESR, 2.9 Ohms, (10 x 20)	UCC	KMX400VB10RM10X20LL
2	1	C3	1uF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	UCC	KMG50VB1R0M5X11LL
3	1	C4	1nF, 1 kV, Disc Ceramic	Panasonic	ECK-D3A102KBP
4	1	C5	1.0uF, 50 V, Ceramic, X7R	Panasonic	ECU-S1H105KBB
5	1	C6	330uF, 35 V, Electrolytic, Very Low ESR, 38mOhm, (10 x 16)	UCC	KZE35VB331MJ16LL
6	1	C7	100nF, 50 V, Ceramic, X7R	Panasonic	ECU-S1H104KBB
7	4	D1 D2 D3 D4	800 V, 1 A, Rectifier, DO-41		1N4006
8	1	D5	1000 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41		1N4007GP
9	1	D6	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41		1N4937
10	1	D7	100 V, 1.1 A, Schottky, DO-41		11DQ10
11	1	L1	1mH, 0.15 A, Ferrite Core	Tokin	SBCP-47HY102B
12	1	R1	200 k, 5%, 1/2 W, Carbon Film		CFR-50JB-200K
13	1	R2	100 R, 5%, 1/8 W, Carbon Film		CFR-12JB-91R
14	1	R3	200 R, 5%, 1/4 W, Carbon Film		CFR-25JB-200R
15	1	R4	7.5 k, 1%, 1/4 W, Metal Film		MFR-25FBF-7K50
16	1	R6	19.1 k, 1%, 1/4 W, Metal Film		MFR-25FBF-19K1
17	1	R7	4.99 k, 1%, 1/4 W, Metal Film		MFR-25FBF-4K99
18	1	R8	470 R, 5%, 1/8 W, Carbon Film		CFR-12JB-470R
19	1	RF1	8.2 R, 2.5 W, Fusible/Flame Proof Wire Wound		CRF253-4 5T 8R2
20	1	T1	EE16 Flyback Transformer		
21	1	U1	LinkSwitch, LNK520P, DIP-8B	Power Integrations	LNK520P
22	1	U2	Opto coupler, 35 V, CTR 300-600%, 4-DIP	Isocom, Sharp	ISP817D, PC817X4
23	1	U3	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TI	TL431CLP

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7 Transformer Specification

7.1 Electrical Diagram

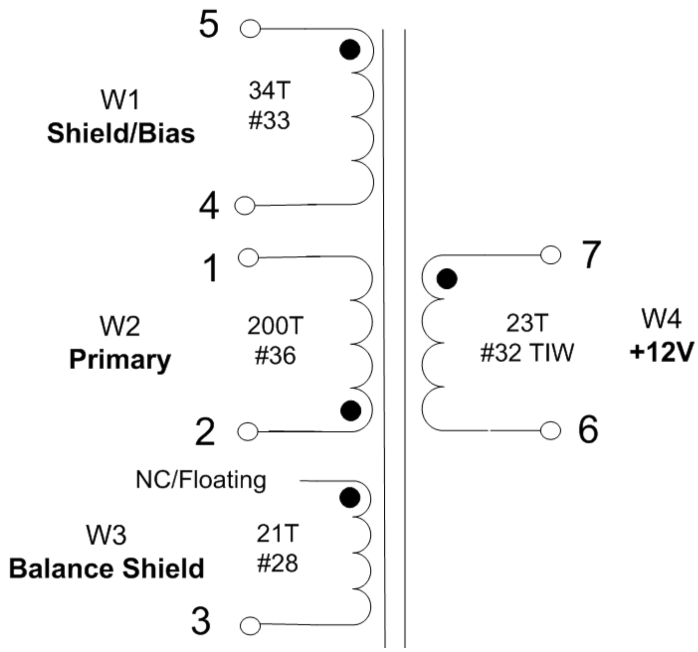

Figure 4 – Transformer Electrical Diagram

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 6-7	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 VRMS	5000µH, -10/+10%
Resonant Frequency	Pins 1-2, all other windings open	500 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with Pins 6-7 shorted, measured at 100 kHz, 0.4 VRMS	250 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: EE16, PC40EE16 TDK – Al = 124nH/T^2
[2]	Bobbin: Horizontal 10 pin
[3]	Magnet Wire: #33 AWG
[4]	Magnet Wire: #36 AWG
[5]	Magnet Wire: #28 AWG
[6]	Triple Insulated Wire: #32 AWG
[7]	Tape: 3M 1298 Polyester Film (white) 2.2mils thick
[8]	Varnish

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7.4 Transformer Build Diagram

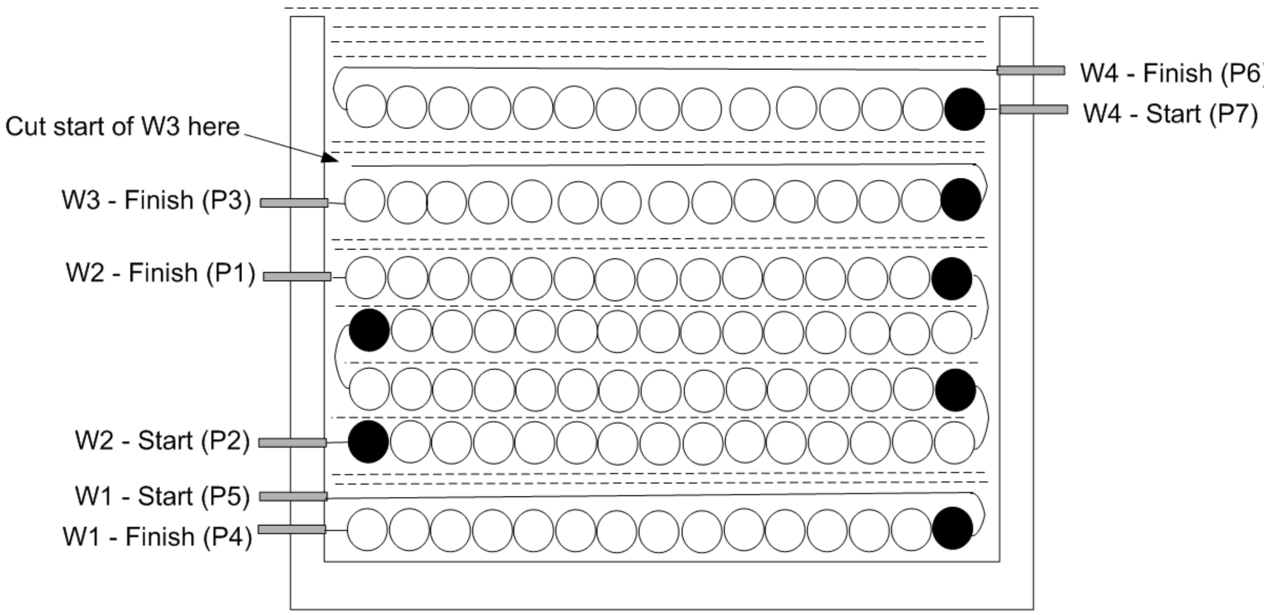

Figure 5 – Transformer Build Diagram

7.5 Transformer Construction

Bobbin Preparation	Pull pins 8-10 on bobbin [2] to provide polarization. Align bobbin on mandrill with pins 1-5 on right hand side.
Core Cancel/Bias	Starting on left hand side of bobbin, wind 34 turns of item [3] uniformly on a single layer from left to right. Finish winding on pin 4. Wrap start of wire to pin 5.
Basic Insulation	Use two layers of item [7] for basic insulation.
Primary	Start at Pin 2. Wind 50 turns of item [4] uniformly on a single layer from right to left. Apply one layer of tape, wind 50 turns on the secondary, third and fourth layer (200T total) adding 1 layer of tape [7] between each layers. Finish winding on pin 1.
Basic Insulation	Use two layers of item [7] for basic insulation.
Balance Shield	Starting on left hand side of bobbin, wind 21 turns of item [5] uniformly on a single layer from left to right. Finish winding on pin 3. Wrap start of wire to right hand side of bobbin and cut close to start of winding leaving it unconnected (as shown in Figure 5).
Basic Insulation	Use two layers of item [7] for basic insulation.
Secondary Winding	Start at Pin 7. Wind 23 of item [6] uniformly on a single layer from left to right. Finish on Pins 6.
Outer Wrap	Wrap windings with 3 layers of tape (item [7]).
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [8]).

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8 Transformer Spreadsheet

A	B	D	F	G	I
LinkSwitch (LNK52X) 032204; Rev.1.8; Copyright Power Integrations 2004	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**LinkSwitch (LNK52X) 032204 Rev.1.8; Copyright Power Integrations 2004**
ENTER APPLICATION VARIABLES					**APC 13.7V/400mA Charger**
VACMIN	108			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	13.7			Volts	Output Voltage
IO	0.4			Amps	Continuous Nominal Output current
VBIAS	20				Bias voltage (recommended default 20V, minimum 16V)
tC	3			msec	Bridge Rectifier Conduction Time Estimate
CIN	16.8			uFarads	Input Filter Capacitor
ESTIMATED LOSSES					
PCORE			266.4	mW	Estimated Core Losses at peak Flux Density (BP)
RCLAMP			200.0	Kohm	Primary clamp resistor (recommended default clamp resistor, RCLAMP)
ESR			0.150	Ohms	Output Capacitor ESR
RSEC			0.2	Ohms	Estimated Resistance of transformer secondary winding.
DC INPUT VOLTAGE PARAMETERS					
VMIN			133	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
ENTER OUTPUT CABLE PARAMETERS					
RCABLE			0.3	Ohms	Resistance of total length of cable from power supply terminals to load and back.
VCABLE			0.120	Volts	Drop along cable connecting power supply to load
ENTER LinkSwitch & OUTPUT DIODE VARIABLES					
LinkSwitch	**LNK520**			*Universal*	*115 Doubled/230*
			Power	*5.5*	*3.5*
I^2 f			2710	A^2 Hz	I^2 f (typical) co-efficient for LinkSwitch
VOR	130		130.00	Volts	Reflected Output Voltage (40<VOR<80 recommended)
VLEAK			2.00	Volts	Error in Feedback voltage as a result of leakage inductance in primary circuit.
VD			1.1	Volts	diode)
VR			100	Volts	Rated Peak Rep Reverse Voltage of secondary diode
ID	3			Amps	Rated Average Forward current for secondary diode
DISCONTINUOUS MODE CHECK					
KDP			1.42		Ensure KDP > 1.15 for discontinuous mode operation.
TON			9.96	us	Linkswitch conduction time
TDON			9.74	us	Secondary Diode conduction time
VOLTAGE STRESS ON LinkSWITCH AND OUTPUT DIODE					
VDRAIN			668	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			56.7	Volts	Output Rectifier Maximum Reverse Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.42		Maximum Operating Duty Cycle
IAVG			0.053	Amps	Average Primary Current
IRMS			0.095	Amps	Primary RMS Current
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**ee16**				
Core		*PC40EE16-Z*			
Bobbin		*BE-16-116CP*			
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
VE			795	mm^3	Effective Core Volume
BW			8.5	mm	Bobbin Physical Winding Width
KCORE			588	kW/m^3	Core losses per unit volume
T(n)	0.9572		0.9572		Estimated transformer efficiency. T(n)=(PSCU+PCORE/2)/POEFF. Re-iterate with n = 0.9572
M			0	mm	Safety Margin Width
NS	23				Number of Secondary Turns
TRANSFORMER PRIMARY DESIGN PARAMETERS					
dLP			1.003		Constant to account for reduction of inductance at higher flux densities. (0.999<dLP<1.05)
LP			4987	uHenries	Primary Inductance
L	4		**4**		Number of Primary Layers
LBIAS	0.9		**0.9**		Number of Bias winding Layers
NP			**200**		Primary Winding Number of Turns
NB			**28**		
ALG			124	nH/T^2	Gapped Core Effective Inductance
BP			**3629**	Gauss	Peak Flux Density (BP<3700)
LG			0.17	mm	Core Gap Length for primary inductance
OD			0.17	mm	Maximum Primary Wire Diameter including insulation to give specified number of layers.
DIA			0.13	mm	Bare conductor diameter
AWG			36	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CMA			**268**	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
AWG_BIAS			30	AWG	

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A	B	D	F	G	I
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			2.21	Amps	Peak Secondary Current
ISRMS			0.82	Amps	Secondary RMS Current
IRIPPLE			0.71	Amps	Output Capacitor RMS Ripple Current
AWGS			31	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.23	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.37	mm	Secondary Maximum Insulated Wire Outside Diameter
INSS			0.07	mm	Maximum Secondary Insulation Wall Thickness
VSEC			0.080	Volts	Voltage Drop across secondary winding
FEEDBACK CIRCUIT COMPONENTS					
RFB			7.07	k-Ohms	Feedback resistor
PRFB			37	mW	Losses in the Feedback resistor
ESTIMATED LOSSES IN POWER SUPPLY AND EFFICIENCY, LOW LINE					
PCABLE			48	mW	Power loss in Output Cable
PSCU			134	mW	Transformer Secondary Copper Losses
PDIODE			440	mW	Output Diode conduction loss
PCAP			100	mW	
PBIAS			51	mW	Power Loss in Feedback circuit
PCONDUCTION			378	mW	Conduction Losses in LinkSwitch calculated at 100C
PCLAMP			85	mW	Primary clamp losses
PCORE			266	mW	Core Losses at peak Flux Density
PBRIDGE			54	mW	Primary bridge rectifier losses
EFFICIENCY ESTIMATE			77.9	%	Estimated Power Supply Efficiency
ADDITIONAL OUTPUT					
VX				Volts	Auxiliary Output Voltage
VDX				Volts	Auxiliary Diode Forward Voltage Drop
NX			0.00		Auxiliary Number of Turns
PIVX			0.00	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency at Full Load (400mA)

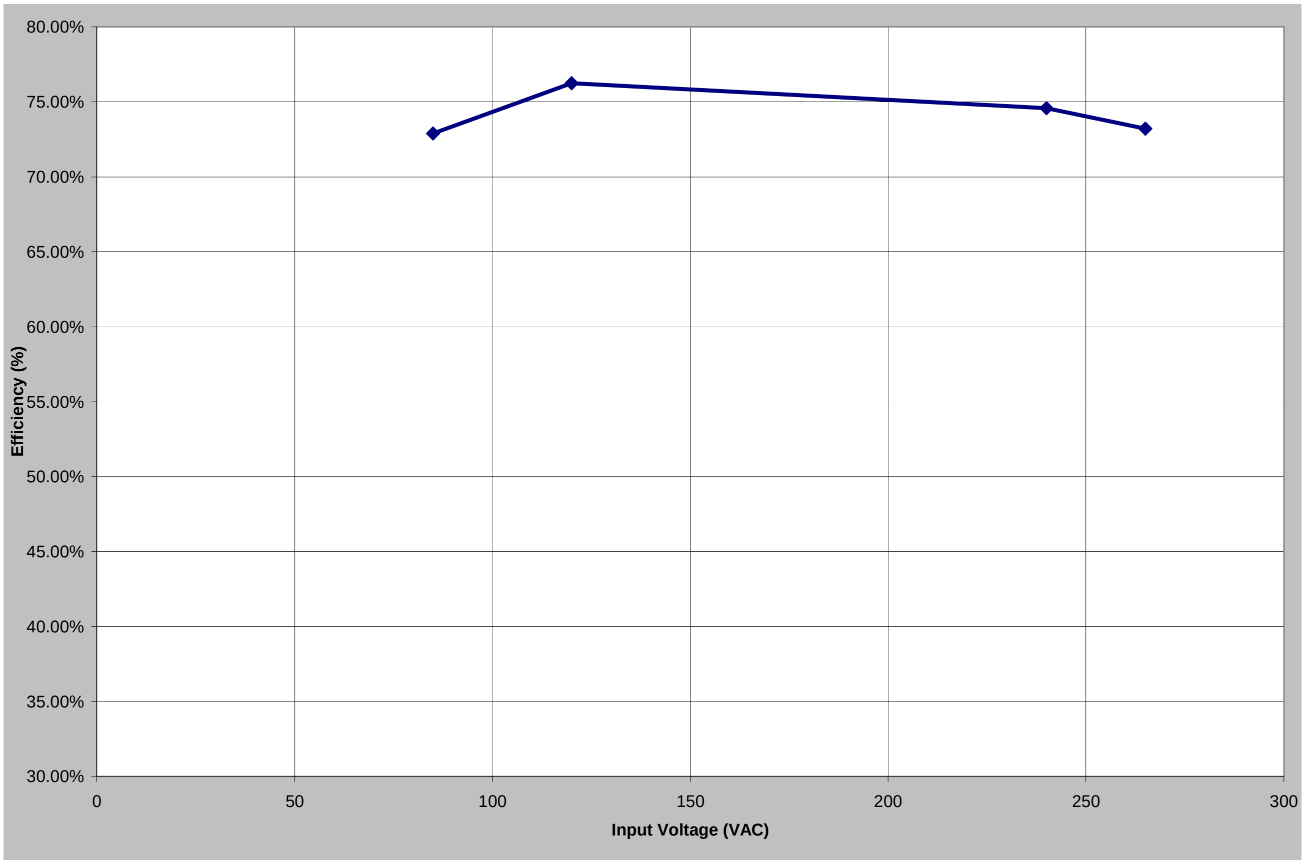

Figure 6 – Efficiency vs. Input Voltage, Room Temperature

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9.2 Efficiency vs. Output Current

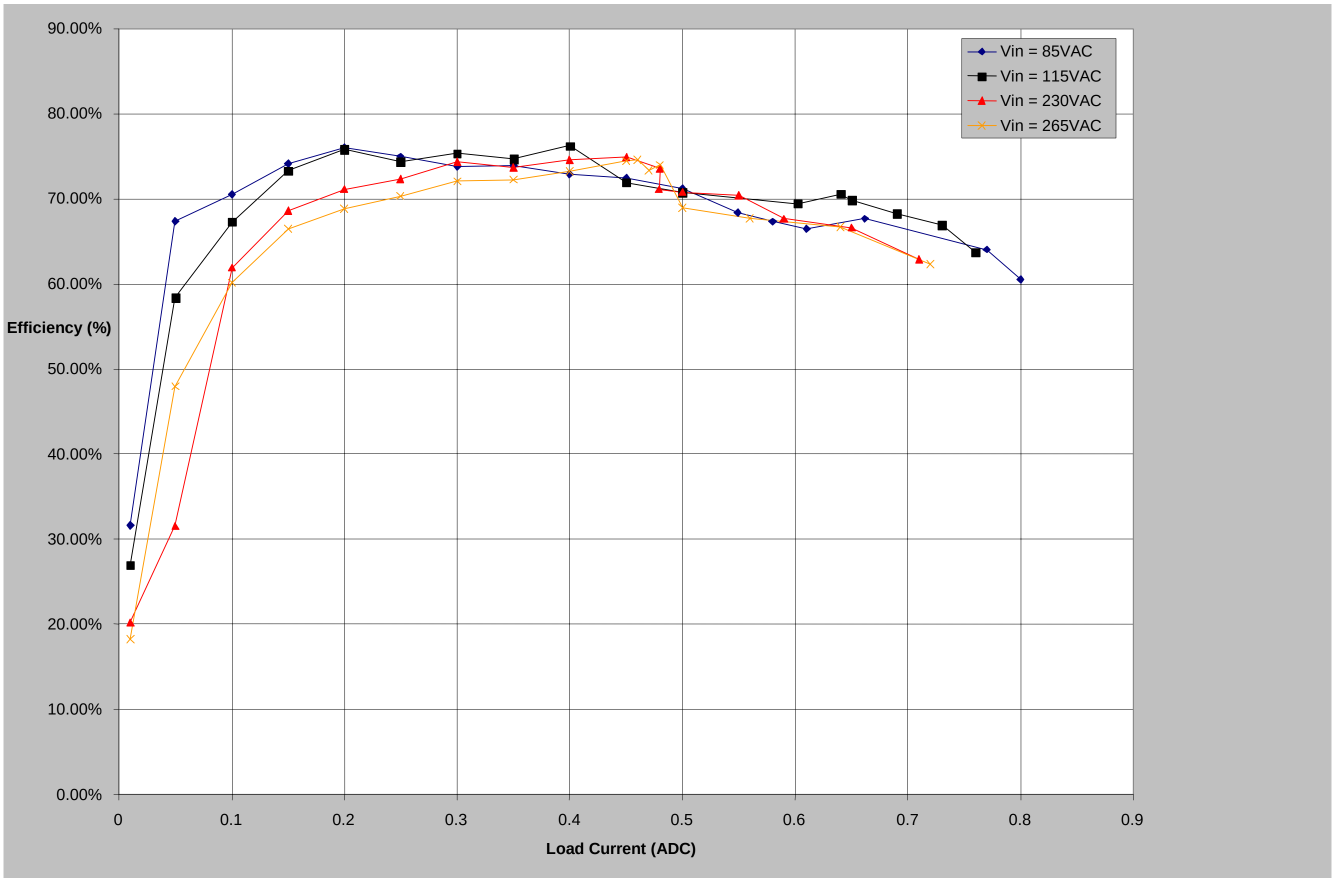

Figure 7 – Efficiency vs. Output Load, Room Temperature

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9.3 Efficiency and Input Power Comparison to Transformer + LDO

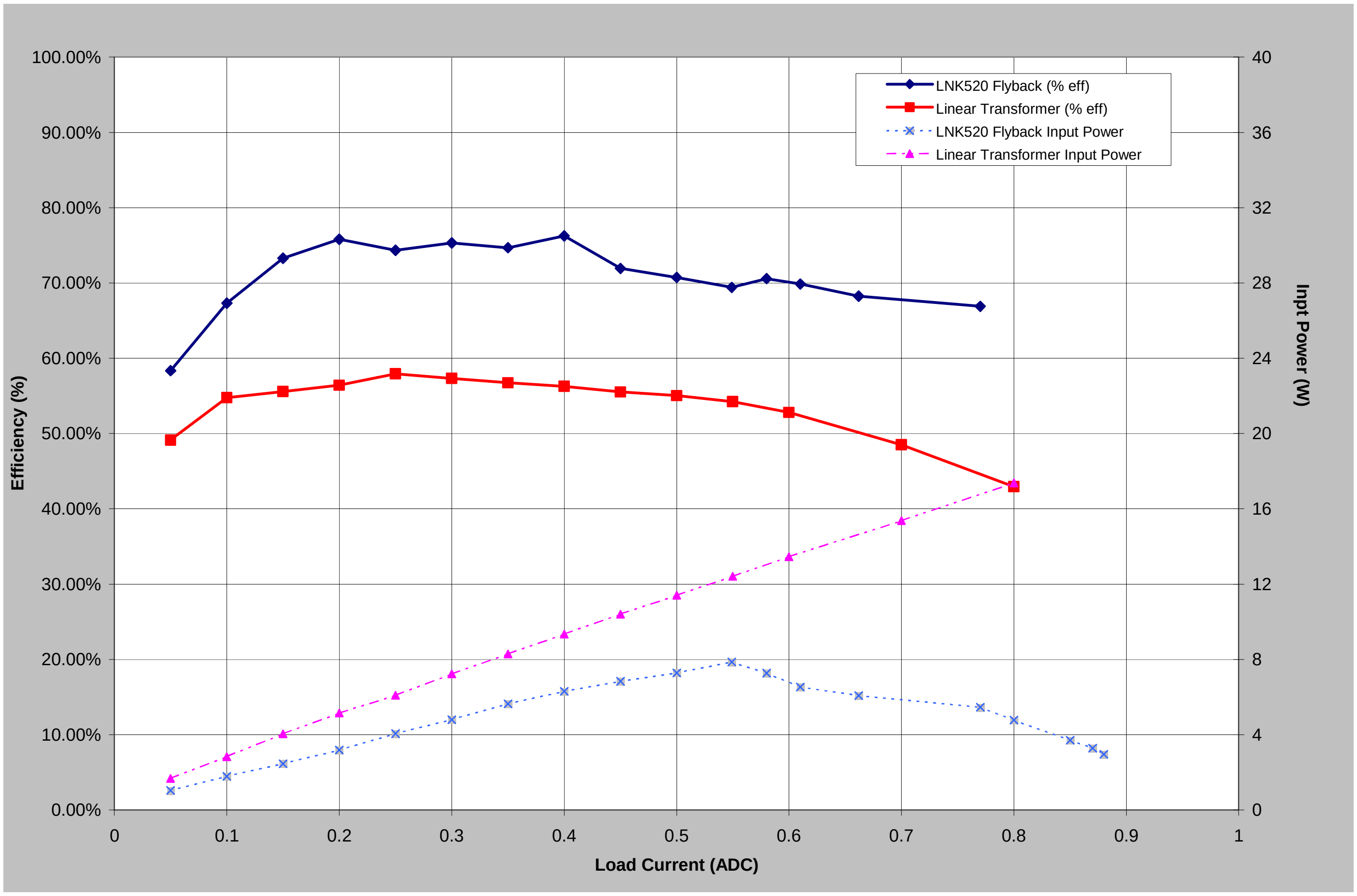

Figure 8 – Efficiency and Input Power at 120VAC Input, Room Temperature, 60 Hz.

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9.4 No-load Input Power

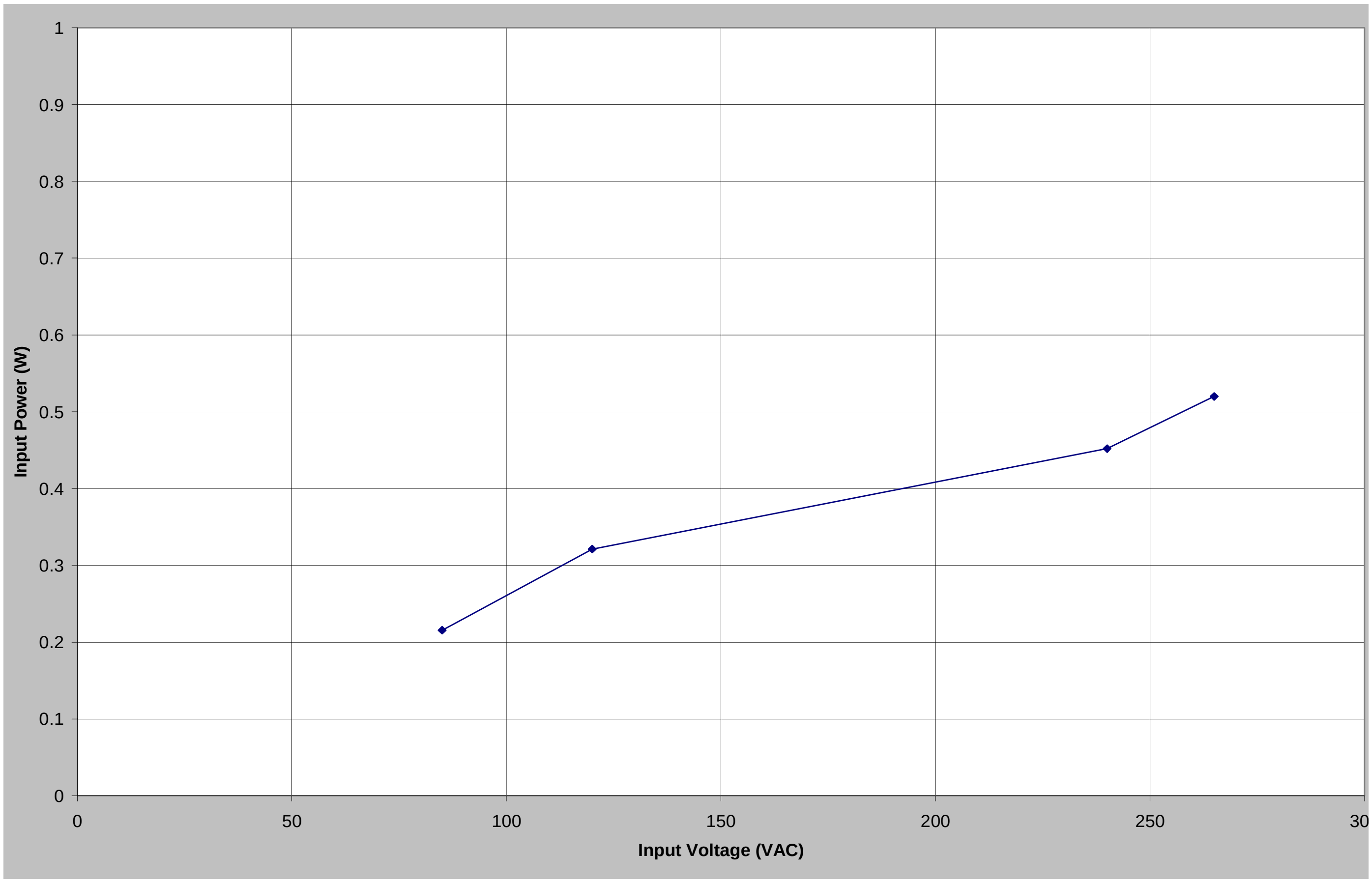

Figure 9 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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9.5 Regulation

9.5.1 Load and Line

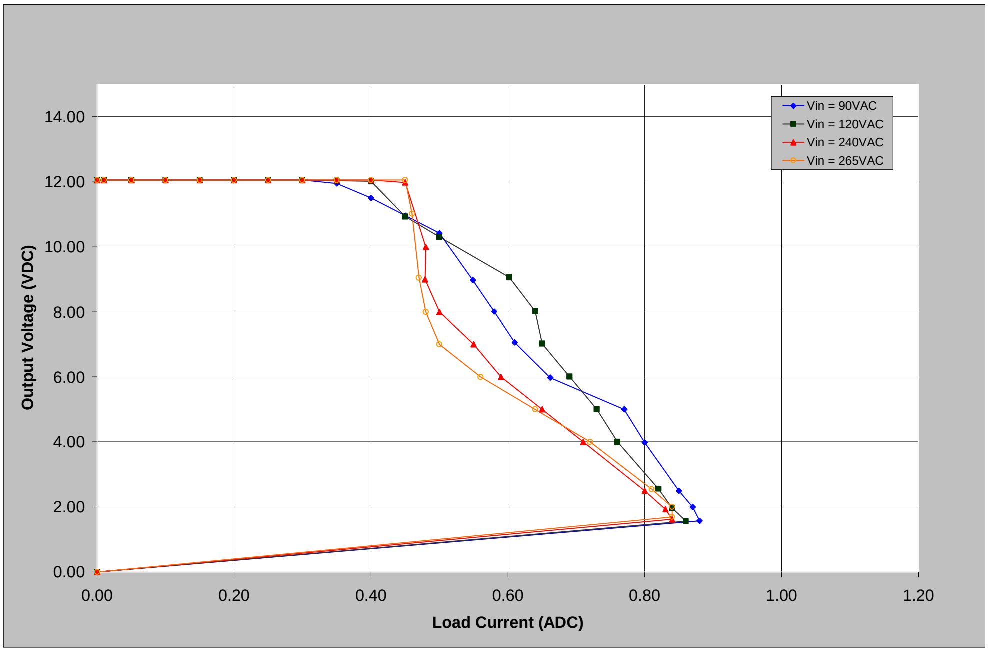

Figure 10 – Load Regulation, Room Temperature.

9.5.2 Battery Load Charge Profile at 120VAC Input

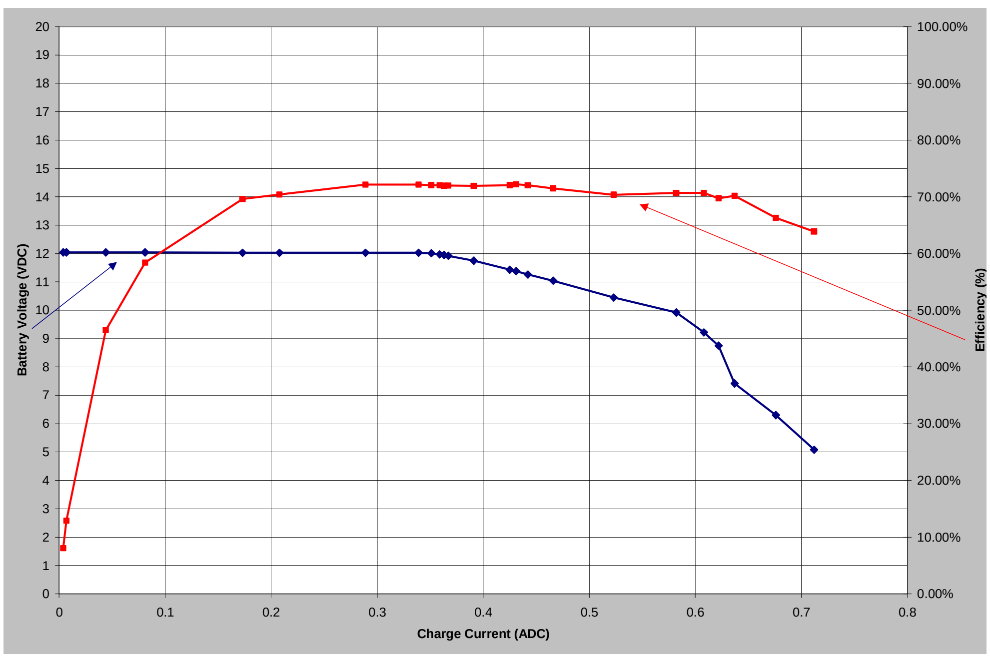

Figure 11 – Battery Charge Profile, Room Temperature.

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10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

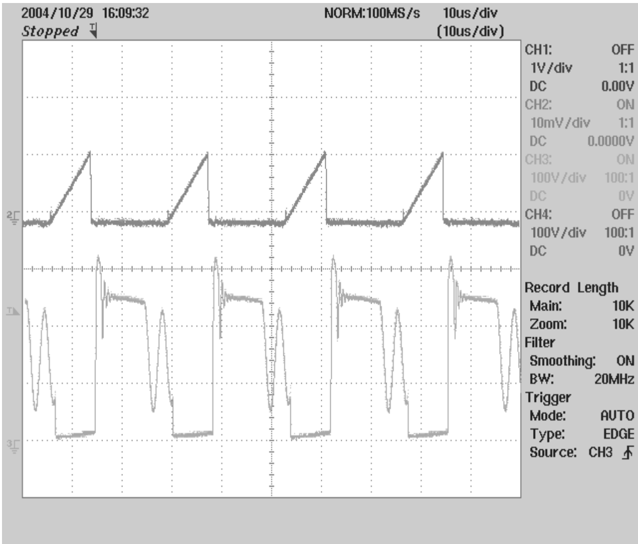

Figure 12 – 85VAC, Full Load
Upper: I_{DRAIN}, 0.2 A / div
Lower: V_{DRAIN}, 100 V, 10 µs / div

Figure 13 – 265VAC, Full Load
Upper: I_{DRAIN}, 0.2 A / div
Lower: V_{DRAIN}, 200 V / div

10.2 Output Voltage Start-up Profile

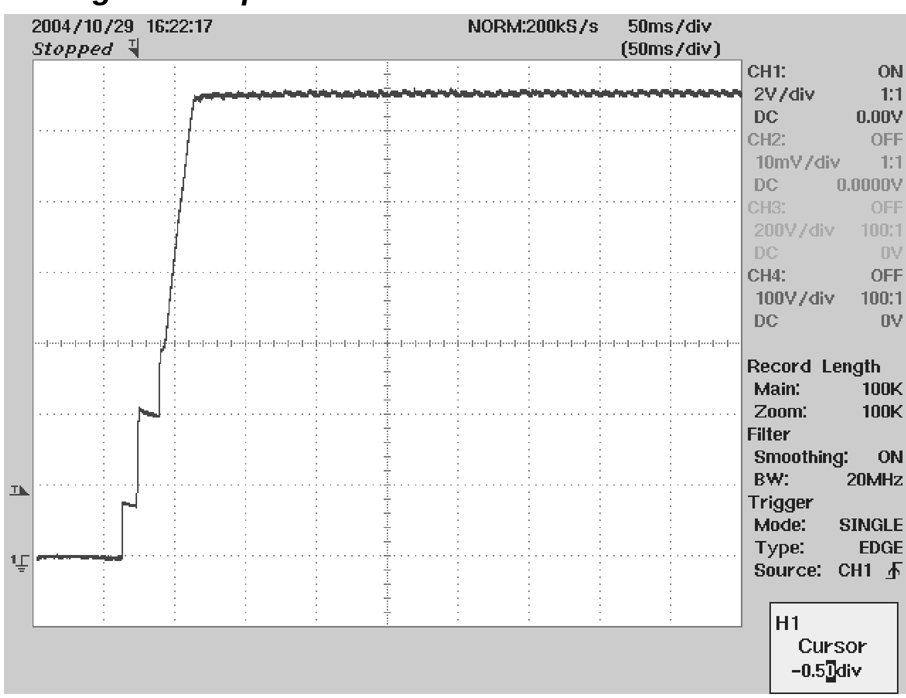

Figure 14 – Start-up Profile Vin = 115VAC; 12V @ 400mA, 2 V, 50 ms / div.

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10.3 Output Ripple Measurements

10.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 15 and Figure 16.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

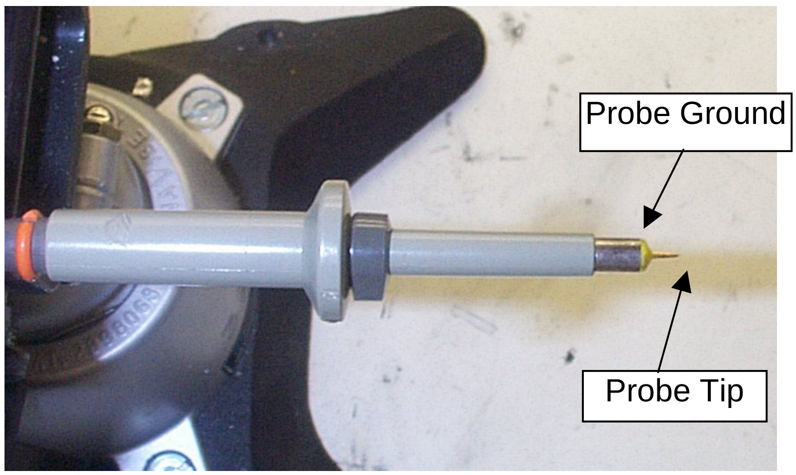

Figure 15 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

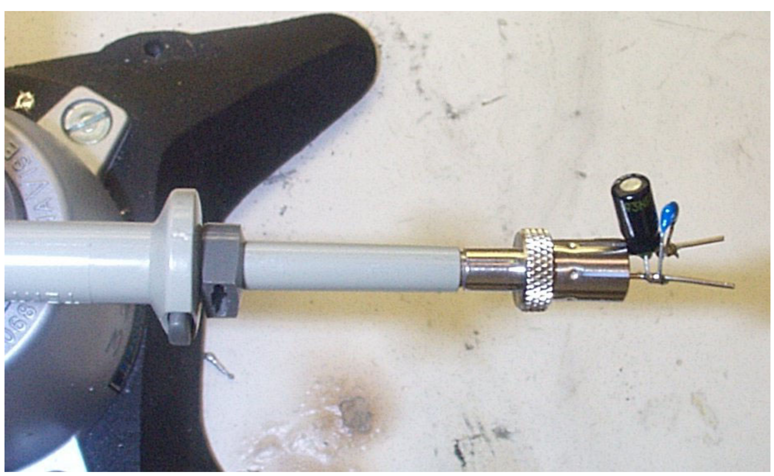

Figure 16 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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10.3.2 Measurement Results

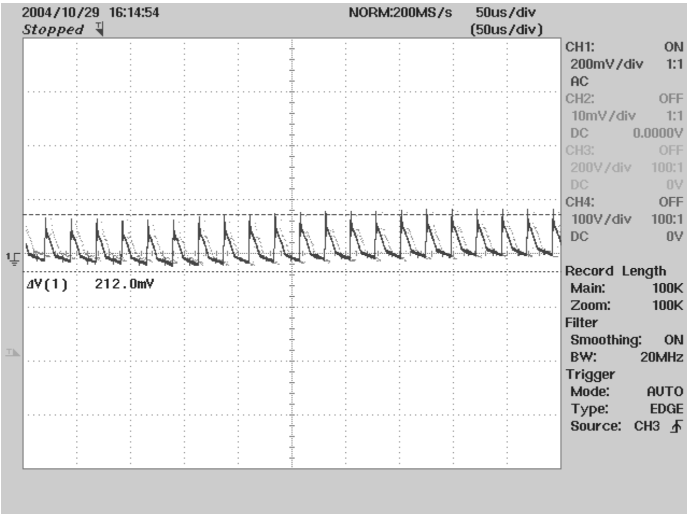

Figure 17 – Ripple, 120VAC, Full Load.
50 µs, 200 mV / div

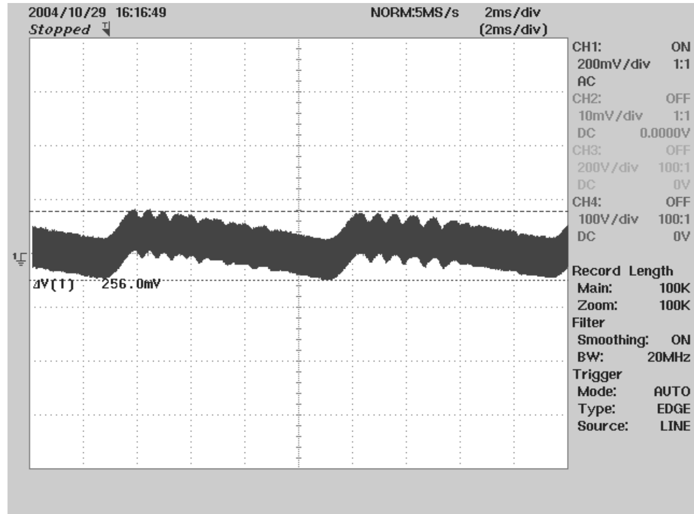

Figure 18 – Ripple, 120VAC, Full Load.
2 ms, 200 mV / div

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11 Conducted EMI

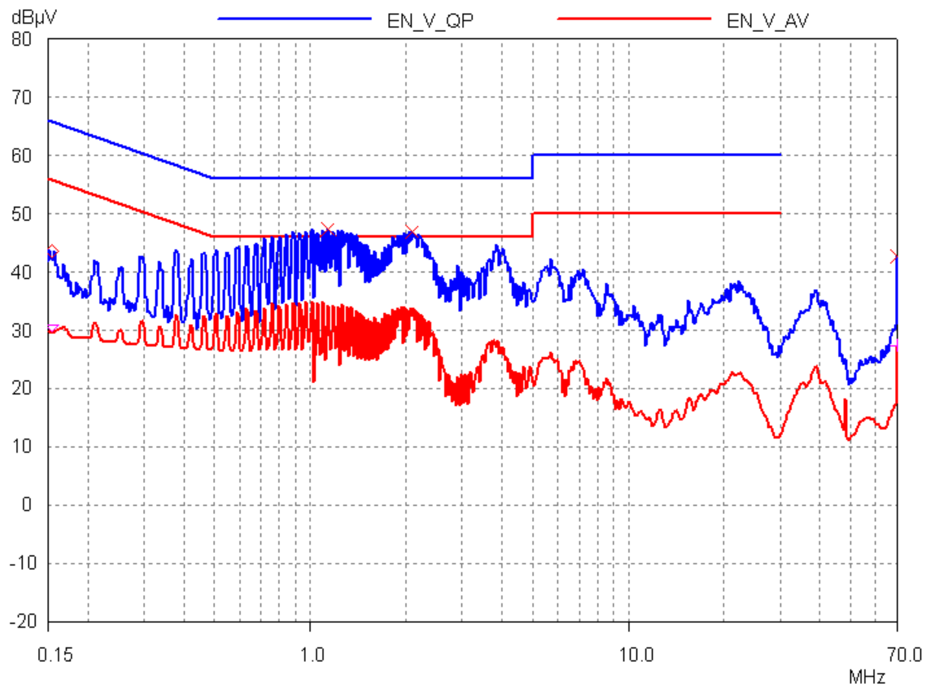

Figure 19 – Conducted EMI, Maximum Steady State Load, 115VAC, 60 Hz, and EN55022 B Limits

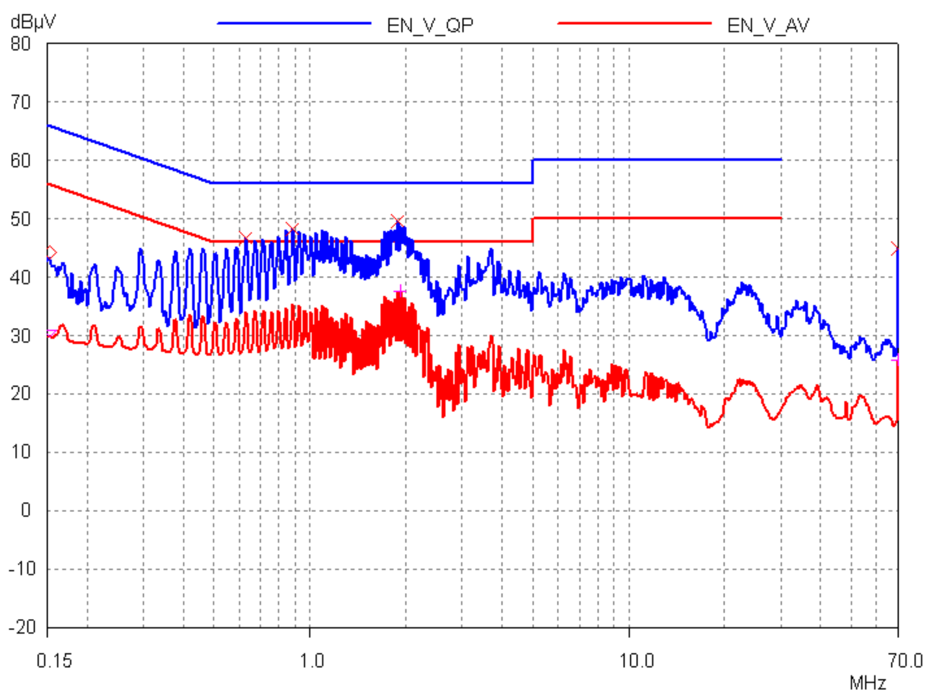

Figure 20 – Conducted EMI, Maximum Steady State Load, 230VAC, 60 Hz, and EN55022 B Limits

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

12 Revision History

Date	Author	Revision	Description & changes	Reviewed
April 20, 2005	RSP/EC	1.0	Initial release	KM / JC / AM

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

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PATENT INFORMATION

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue,
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3,
D-80336, Munich, Germany
Phone: +49-895-527-3910
Fax: +49-895-527-3920
e-mail: eurosales@powerint.com

JAPAN
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama,
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
17F-3, No. 510,
Chung Hsiao E. Rd., Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 807, Pacheer,
Commercial Centre,
555 Nanjing West Road,
Shanghai, 200041, China
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

INDIA (TECHNICAL SUPPORT)
Innovatech
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore, India, 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

KOREA
8th Floor, DongSung Bldg.
17-8 Yoido-dong,
Youngdeungpo-gu,
Seoul, 150-874, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
e-mail: koreasales@powerint.com

UK (EUROPE & AFRICA HEADQUARTERS)
1st Floor, St. James's House
East Street
Farnham, Surrey GU9 7TJ
United Kingdom
Phone: +44-1252-730-140
Fax: +44-1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu,
Shenzhen, Guangdong,
518031, China
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
e-mail: chinasales@powerint.com

ITALY
Via Vittorio Veneto 12, Bresso,
Milano,
20091, Italy
Phone: +39-028-928-6001
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760