Design Example Report

Title	*275 W PFC Front-End Using HiperPFS™-3 PFS7527H*
Specification	90 VAC – 264 VAC Input; 385 VDC Output
Application	PFC Front-End
Author	Applications Engineering Department
Document Number	DER-394
Date	June 24, 2015
Revision	1.0

Summary and Features

- Highly integrated, low component count, low-cost PFC
- Ultra-low reverse recovery loss diode (Qspeed™)
- Power Integrations eSIP-16 low-profile controller package
- "Cool-Pad" package reduces IC mounting hardware
  - Eliminates insulating pad/heat-spreader
- EN61000-3-2 Class-D compliant
- High PFC efficiency enables up to 80+ Platinum PC Main design
- Enhanced light load power factor (PF)
  - PF >0.9 at 20% Load and 230 VAC, 50 Hz input
  - PF >0.95 at 50% Load
- Frequency sliding maintains high efficiency across load range
  - >95% from 10 to 100% load (115 VAC and 230 VAC input)
- Feed forward line sense gain – maintains relatively constant loop gain over entire operating voltage range
- Excellent transient load response
- Frequency adjusted over input line voltage and load
  - Spread-spectrum across >60 kHz window simplifies EMI filtering requirements
- Integrated QSpeed switching diode reduces component count and simplifies assembly

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Important Note:
All testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a PFC power supply utilizing a HiperPFS-3 PFS7527H PFC controller with integrated power MOSFET and switching diode. This power supply is intended as a general purpose platform that operates from universal input line voltage and provides a regulated 385 V DC output voltage and continuous output power of 275 W.

The DER-394 power supply is designed to operate with forced air cooling greater than 200 LFM for all input and load conditions up to the rated maximum ambient temperature of 50 ^{o}C.

This document contains the power supply specification, schematic, bill of materials, inductor documentation, printed circuit layout, and performance data.

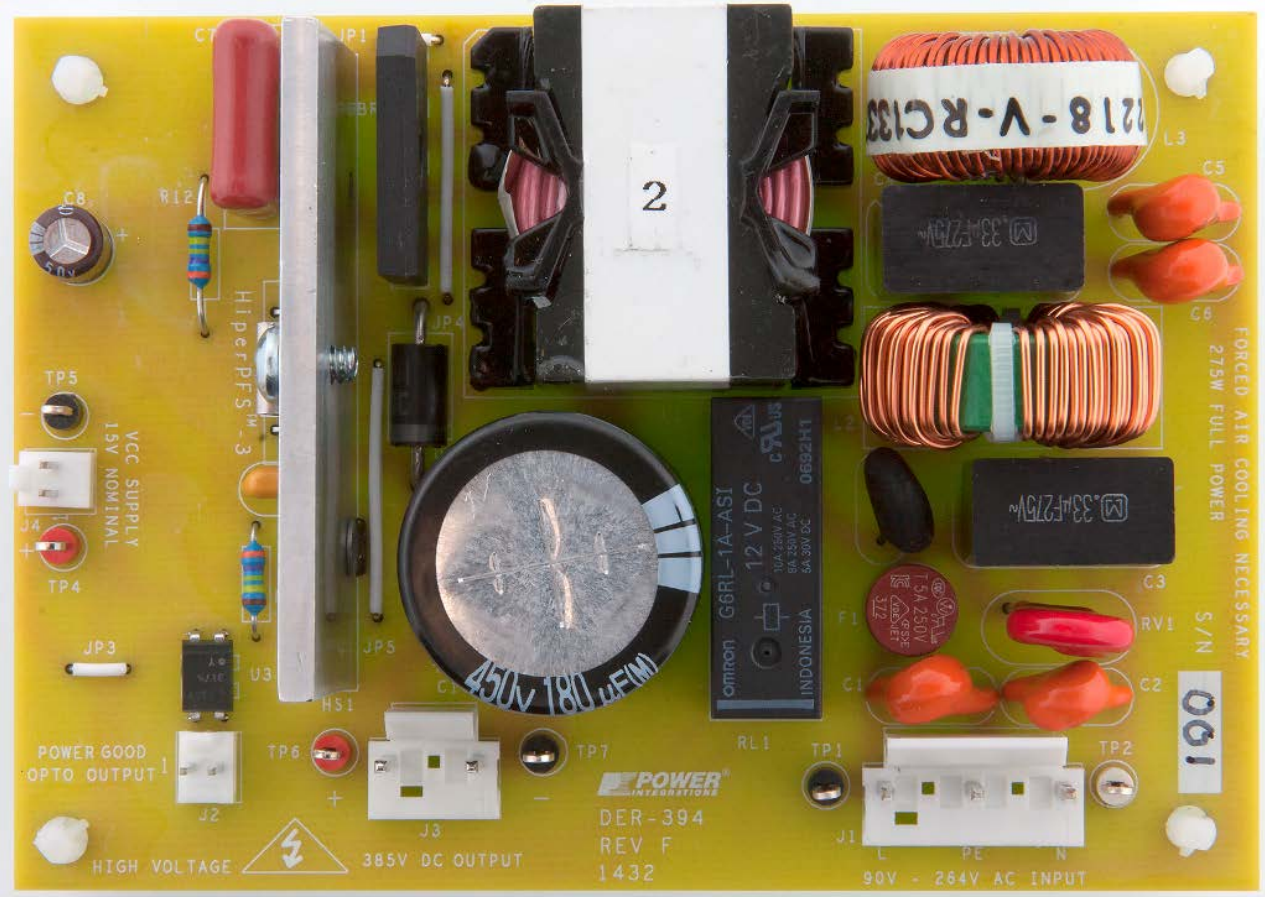

Figure 1 – Populated Circuit Board Photograph (Top View).

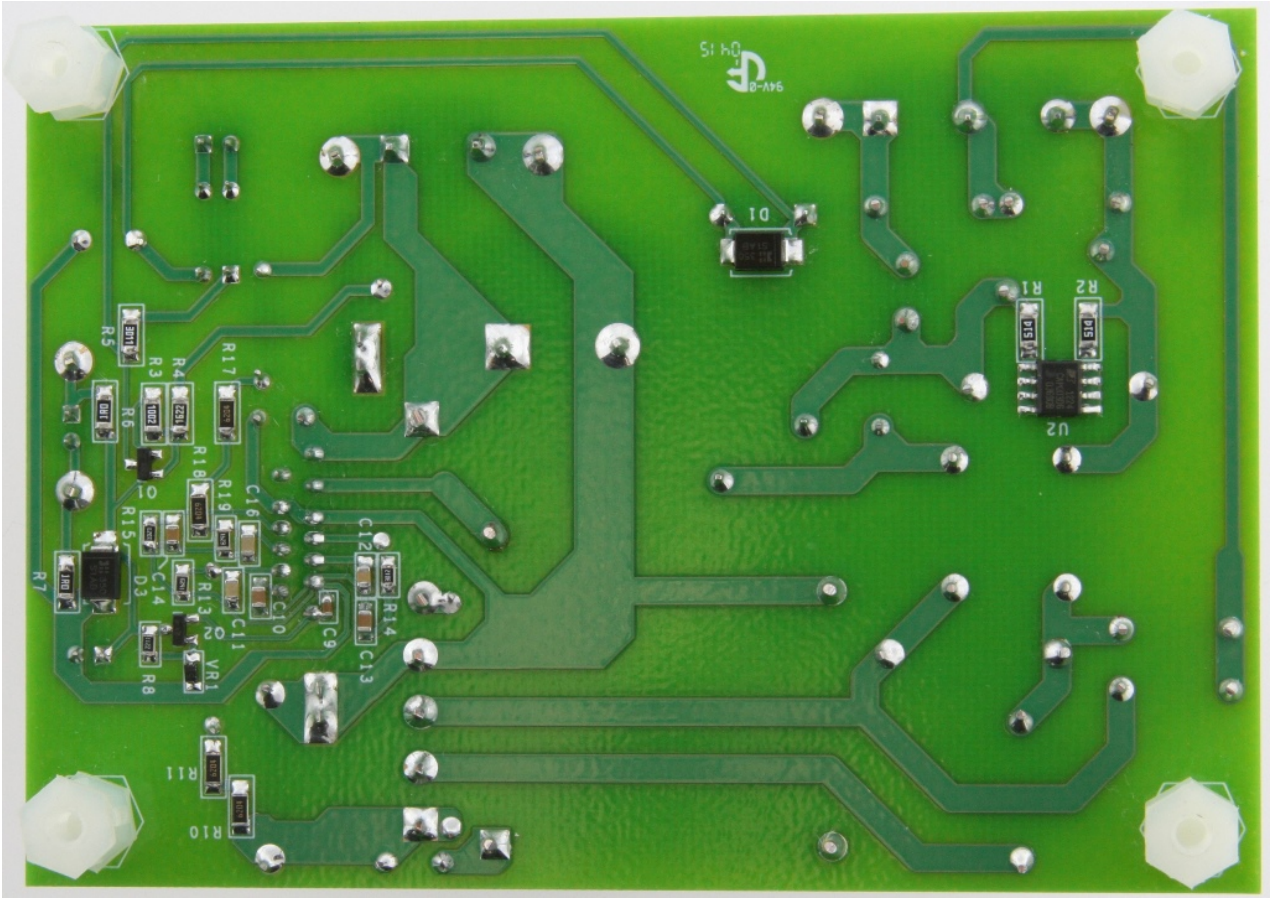

Figure 2 – Populated Circuit Board Photograph (Back View).

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	3 Wire
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	375	385	395	V	
Output Ripple Voltage p-p	V_{RIPPLE}			30	V	20 MHz Bandwidth
Output Current	I_{OUT}		0.71		A	
Total Output Power						
Continuous Output Power	P_{OUT}		275		W	
Efficiency						
Full Load	η	94			%	Measured at P_{OUT} 25 °C
Minimum efficiency at 20, 50 and 100 % of P_{OUT}	η_{80+}	94			%	Measured at 115 VAC Input
Environmental						1.2/50 µs surge, IEC1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Line Surge						
Differential Mode (L1-L2)			2		kV	
Common mode (L1/L2-PE)			3		kV	
Ambient Temperature	T_{AMB}	0		50	°C	Forced convection required 300 LFM Min.
Auxiliary Supply Input Auxiliary Supply	V_{aux}	15		17	V	DC supply

3 Schematic

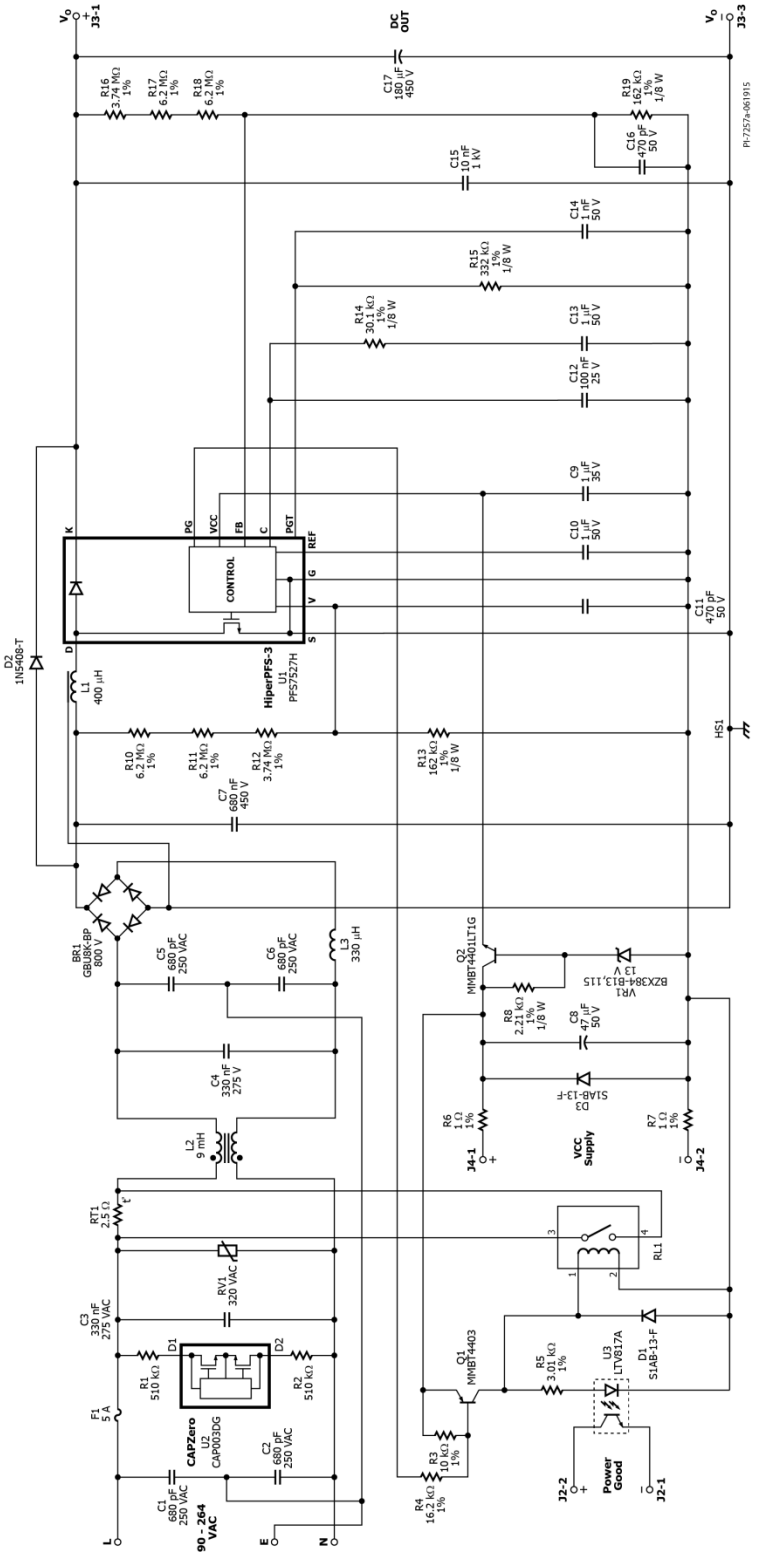

Figure 3 – Schematic.

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4 Circuit Description

This PFC is designed around the Power Integrations PFS7527H integrated PFC controller. This design is rated for a continuous output power of 275 W and provides a regulated output voltage of 385 VDC nominal, maintaining a high input power factor and overall efficiency over line and load, while remaining low in cost.

1.1 *Input EMI Filter and Rectifier*

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, C4, C5 and C6 in conjunction with inductors L2 and L3, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitor C7 provides input decoupling charge storage to reduce input ripple current at the switching frequencies and harmonics.

Resistors R1, R2 and CAPZero™ IC U2 are provided to discharge the EMI filter capacitors after line voltage has been removed from the circuit, while dissipating zero power during operation.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

1.2 *PFS7527H Boost Converter*

The boost converter stage consists of the boost inductor L1 and the PFS7527H IC U1. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

During start-up, diode D2 provides an inrush current path to the output capacitor C17, bypassing the switching inductor L1 and switch U1 in order to prevent a resonant interaction between the switching inductor and output capacitor.

NTC thermistor RT1 limits inrush current of the supply when line voltage is first applied. Thermistor RT1 is bypassed by the electro-mechanical relay RL1 after the output voltage is in regulation and a power good signal from U1 is asserted low. Resistor R3, R4, and Q1 drive relay RL1 and optocoupler U3. Diode D1 clamps the relay coil reverse voltage during de-assertion transitions Resistor R5 limits the current to the diode in the optocoupler. IC U3 provides optocoupler isolation through connector J2 for a POWER GOOD output signal if required.

Capacitor C15 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U1 MOSFET drain voltage overshoot during turn-off. Capacitor C9 decouples and bypasses the U1 VCC pin.

Resistor R15 programs the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD (PG) pin will go into a high-impedance state.

Capacitor C10 on the REF pin of U1 is a noise decoupler for the internal reference and also programs the output power for either full mode, 100% of rated power [C10 = 1 μF] or efficiency mode, 80% [C10 = 0.1 μF] of rated power.

1.3 *Input Feed Forward Sense Circuit*

The input voltage of the power supply is sensed by the IC U1 using resistors R10, R11, R12 and R13. The capacitor C11 bypasses the V pin on IC U1.

1.4 *Output Feedback*

An output voltage resistive divider network consisting of resistors R16, R17, R18, and R20 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U11 setting the PFC output at 385 V. Capacitor C16 decouples the U1 FB pin.

Resistor R14 and capacitor C13 provide the control loop dominant pole. C12, attenuates high-frequency noise.

1.5 *Bias Supply Series Regulator*

The PFS7527H IC requires a regulated V_{CC} supply of 12 V nominal for operation, with an absolute maximum voltage rating of 15 V. V_{CC} levels in excess of this maximum could result in failure of the IC. Resistor R8, Zener diode VR1, and transistor Q2 form a series regulator that regulates the supply voltage to IC U1 to 12.4 V nominal. Capacitor C9 decouples the input auxiliary supply voltage to ensure reliable operation of IC U1.

Resistors R6, R7 and capacitor C8 provide filtering of the external V_{CC} voltage source. Reverse polarity protection of this source is achieved with diode D3.

The +15 V auxiliary supply is applied on connector J4.

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5 PCB Layout

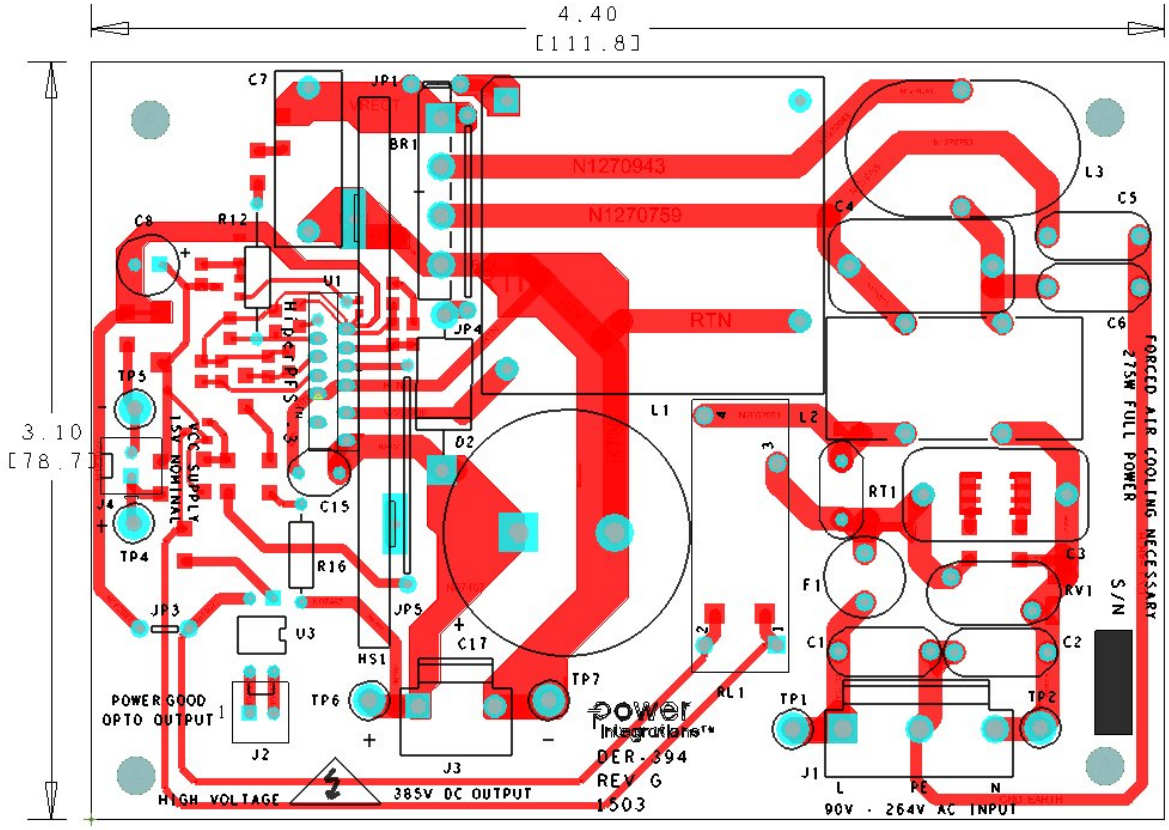

Figure 4 – Printed Circuit Layout, Top.

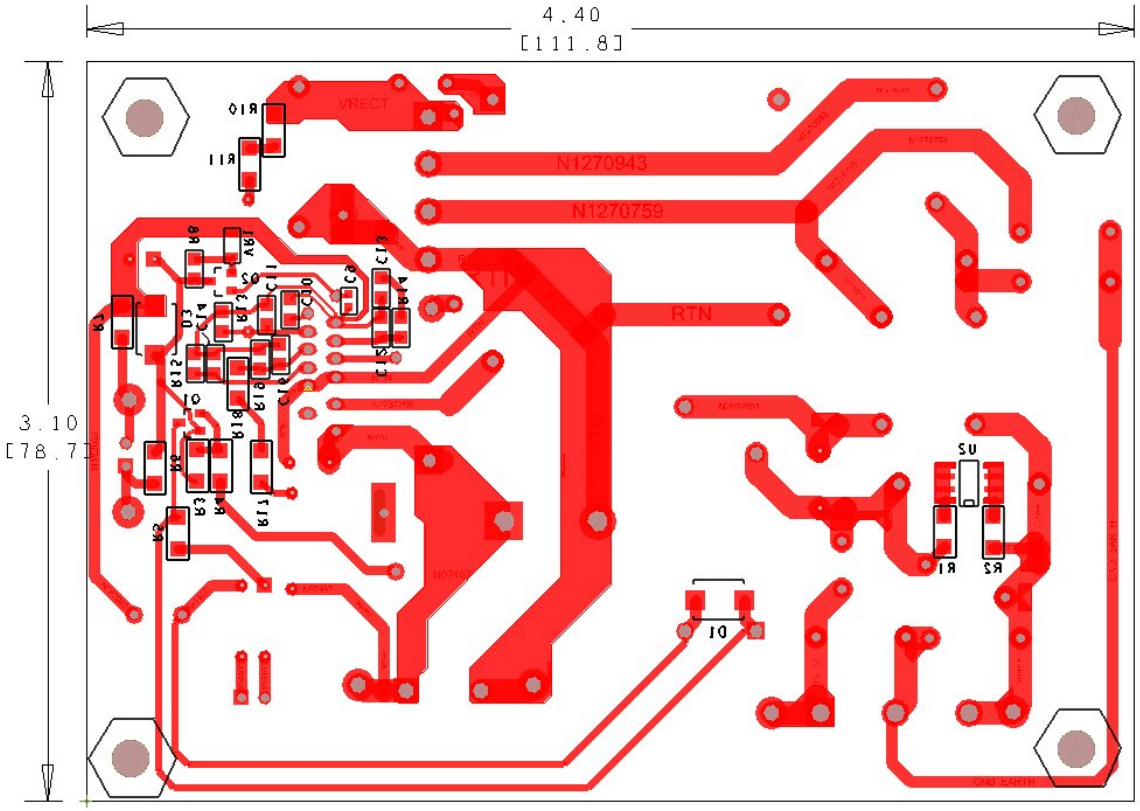

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	4	C1 C2 C5 C6	680 pF, Ceramic, Y1	440LT68-R	Vishay
3	2	C3 C4	330 nF, 275 VAC, Film, X2	ECQ-U2A334ML	Panasonic
4	1	C7	680 nF, 450 VDC, Disc Ceramic	ECQ-E2W684KH	Panasonic
5	1	C8	47 µF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG500ELL470MF11D	Nippon Chemi-Con
6	1	C9	1 µf 35 V, Ceramic, X7R, 0603	C1608X7R1V105M	TDK
7	2	C10 C13	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
8	2	C11 C16	470 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB471	Yageo
9	1	C12	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
10	1	C14	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
11	1	C15	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
12	1	C17	180 µF, 450 V, Electrolytic, Snap In, (25 x 30)	ESMQ451VSN181MQ30S	United Chemi-con
13	2	D1 D3	50 V, 1 A, Standard Recovery, GPP, SMB	S1AB-13-F	Diodes, Inc.
14	1	D2	1000 V, 3 A, Recitifier, DO-201AD	1N5408-T	Diodes, Inc.
15	1	ESIPCLIP_M4_METAL1	Heat sink Hardware, Edge Clip, 20.76 mm L x 8 mm W x 0.015 mm Thk	NP975864	Aavid Thermalloy
16	1	F1	5 A, 250 V, Slow, TR5	37215000411	Wickman
17	1	HS1	FAB, HEAT SINK, DER394		Custom
18	1	J1	5 Position (1 x 5) header, 0.156 pitch, Vertical	0026604050	Molex
19	2	J2 J4	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
20	1	J3	CONN HEADER 3POS (1x3).156 VERT TIN	0026604030	Molex
21	1	JP1	Wire Jumper, Non insulated, #22 AWG, 0.2 in	298	Alpha
22	1	JP3	Wire Jumper, Insulated, #24 AWG, 0.2 in	C2003A-12-02	Gen Cable
23	1	JP4	Wire Jumper, Insulated, #24 AWG, 0.8 in	C2003A-12-02	Gen Cable
24	1	JP5	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable
25	1	L1	Custom, PFC Inductor, 400 uH, PQ32/20, Vertical	BQ32/30-1112CPFR	TDK
26	1	L2	9 mH, 5A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
27	1	L3	330 µH, 3.3 A, Vertical Toroidal	2218-V-RC	Bourns
28	4	POST-CRKT_BRD_6-32_HEX1 POST-CRKT_BRD_6-32_HEX2 POST-CRKT_BRD_6-32_HEX3 POST-CRKT_BRD_6-32_HEX4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
29	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
30	1	Q2	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
31	2	R1 R2	510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
32	1	R3	10.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1002V	Panasonic
33	1	R4	16.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1622V	Panasonic
34	1	R5	3.01 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3011V	Panasonic
35	2	R6 R7	1 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF1R0V	Panasonic
36	1	R8	2.21 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2211V	Panasonic
37	4	R10 R11 R17 R18	6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
38	2	R12 R16	3.74 MΩ, 1%, 1/4 W, Metal Film	MFR-25FBF52-3M74	Yageo
39	2	R13 R19	162 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1623V	Panasonic

40	1	R14	30.1 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3012V	Panasonic
41	1	R15	332 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3323V	Panasonic
42	1	RL1	RELAY GEN PURPOSE SPST 8 A 12 V	G6RL-1A-ASI-DC12	OMRON
43	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SL10 2R505	Ametherm
44	1	RTV	Thermally conductive Silicone Grease	120-SA	Wakefield
45	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
46	1	SCREW	SCREW MACHINE PHIL 6-32 X 1/4 SS	PMSSS 632 0025 PH	Building Fasteners
47	3	TP1 TP5 TP7	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
48	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
49	2	TP4 TP6	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
50	1	U1	HiperPFS-3, eSIP16/13	PFS7527H	Power Integrations
51	1	U2	CAPZero, SO-8C	CAP003DG	Power Integrations
52	1	U3	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
53	1	VR1	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP Semi
54	1	WASHER	Washer Flat #6, SS, Zinc Plate, 0.267 OD x 0.143 ID x 0.032 Thk	620-6Z	Olander

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7 Inductor Design Spreadsheet

Note: If current density is higher than 6 A / mm^2 on forced air cooling case, a “warning” will be generated. Need for a higher cross section of the wire should be made based on the thermal test result. With sufficient cooling, higher current densities can be used safely.

Hiper_PFS-3_Boost_012815; Rev.0.6; Copyright Power Integrations 2015	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Hiper_PFS-3_Boost_012815_Rev0-6.xls; Continuous Mode Boost Converter Design Spreadsheet**
Enter Application Variables					
Input Voltage Range	**Universal**		**Universal**		Input voltage range
VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
VACMAX			265	VAC	Maximum AC input voltage
VBROWNIN			76	VAC	Expected Minimum Brown-in Voltage
VBROWNOUT			72	VAC	Specify brownout voltage.
VO			385	VDC	Nominal load voltage
PO	275		275	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	°C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
VO_MIN			366	VDC	Minimum Output voltage
VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
tHOLDUP	17		17	ms	Holdup time
VHOLDUP_MIN			310	VDC	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**Yes**		**Yes**		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
KP and INDUCTANCE					
KP_TARGET	0.395		0.395		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
LPFC_TARGET (0 bias)			399	uH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
LPFC_DESIRED (0 bias)			399	uH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
KP_ACTUAL			0.380		Actual KP calculated from LPFC_ACTUAL
LPFC_PEAK			399	uH	Inductance at VACMIN, 90°. For Ferrite, same as LPFC_DESIRED (0 bias)
Basic current parameters					
IAC_RMS			3.29	A	AC input RMS current at VACMIN and Full Power load
IO_DC			0.71	A	Output average current/Average diode current
PFS Parameters					
PFS Part Number	**Auto**		**PFS7527H**		If examining brownout operation, over-ride autopick with desired device size
Operating Mode	**Full Power**		**Full Power**		Mode of operation of PFS. For Full Power mode

					enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
IOCP min			8.0	A	Minimum Current limit
IOCP typ			8.4	A	Typical current limit
IOCP max			8.8	A	Maximum current limit
IP			5.47	A	MOSFET peak current
IRMS			2.68	A	PFS MOSFET RMS current
RDSON			0.52	Ohms	Typical RDSon at 100 'C
FS_PK			93	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			67	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
PCOND_LOSS_PFS			3.7	W	Estimated PFS conduction losses
PSW_LOSS_PFS			2.7	W	Estimated PFS switching losses
PFS_TOTAL			6.4	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			4.91	°C/W	Maximum thermal resistance of heatsink
INDUCTOR DESIGN					
Basic Inductor Parameters					
LPFC (0 Bias)			399	uH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
LP_TOL			10.0	%	Tolerance of PFC Inductor Value (ferrite only)
IL_RMS			3.14	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
Material and Dimensions					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	**Auto**		**PC44/PC95**		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
Core Geometry	**Auto**		**PQ**		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
Core	**PQ32/20**		**PQ32/20**		Core part number
Ae			170.00	mm^2	Core cross sectional area
Le			55.50	mm	Core mean path length
AL			6530.00	nH/t^2	Core AL value
Ve			9.44	cm^3	Core volume
HT (EE/PQ) / ID (toroid)			5.12	mm	Core height/Height of window; ID if toroid
MLT			67.1	mm	Mean length per turn
BW			8.98	mm	Bobbin width
LG			1.36	mm	Gap length (Ferrite cores only)
Flux and MMF calculations					
BP_TARGET (ferrite only)	4100	*Info*	4100	Gauss	Info: Peak flux density is too high. Check for Inductor saturation during line transient operation
B_OCP (or BP)			4061	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
B_MAX			2429	Gauss	peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance
µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
µ_MAX (powder only)			N/A	%	mu_max greater than 75% indicates a very large core. Please verify
µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
I_TEST			8.4	A	Current at which B_TEST and H_TEST are

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					calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
B_TEST			3876	Gauss	Flux density at I_TEST and maximum tolerance inductance
µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
Wire					
TURNS			56		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
ILRMS			3.14	A	Inductor RMS current
Wire type	**Litz**		**Litz**		Select between "Litz" or "Magnet" for double coated magnet wire
AWG	38		38	AWG	Inductor wire gauge
Filar	40		40		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
OD (per strand)			0.102	mm	Outer diameter of single strand of wire
OD bundle (Litz only)			0.90	mm	Will be different than OD if Litz
DCR			0.27	ohm	Choke DC Resistance
P AC Resistance Ratio			1.22		Ratio of total Cu loss including HF ACR loss vs. assuming only DCR (uses Dowell equations)
J		*Warning*[1]	9.69	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
FIT			99%	%	Percentage fill of winding window for EE/PQ core. Full window approx. 90%
Layers			5.1		Estimated layers in winding
Loss calculations					
BAC-p-p			959	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
LPFC_CORE_LOSS			0.20	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			3.20	W	Estimated Inductor copper losses
LPFC_TOTAL_LOSS			3.40	W	Total estimated Inductor Losses
Built-in PFC Diode					
PFC Diode Part Number			INTERNAL		PFC Diode Part Number
Type			SPECIAL		PFD Diode Type
Manufacturer			PI		Diode Manufacturer
VRRM			530	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
Qrr					high temperature
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			1.05	W	Estimated Diode conduction losses
PSW_DIODE			0.28	W	Estimated Diode switching losses
P_DIODE			1.33	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			4.91	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
Output Capacitor	**Auto**		180	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			13.6	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			17.1	ms	Expected holdup time with selected Output capacitor
ESR_LF			0.92	ohms	Low Frequency Capacitor ESR
ESR_HF			0.37	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.48	A	Low Frequency Capacitor RMS current
IC_RMS_HF			1.19	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.21	W	Estimated Low Frequency ESR loss in Output

					capacitor
CO_HF_LOSS			0.52	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.74	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
I^2t Rating			12.64	A^2*s	Minimum I^2t rating for fuse
Fuse Current rating			4.88	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			3.03	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			5.32	W	Estimated Bridge Diode conduction loss
CIN			0.8	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT			9.37	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
PFS3 small signal components					
C_REF			1.0	uF	REF pin capacitor value
RV1			4.0	MOhms	Line sense resistor 1
RV2			6.0	MOhms	Line sense resistor 2
RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
C_VCC			1.0	uF	Supply decoupling capacitor
C_C			100	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
PGT set resistor			333.0	kohm	Power good threshold setting resistor
Feedback Components					
R1			4.0	Mohms	Feedback network, first high voltage divider resistor
R2			6.0	Mohms	Feedback network, second high voltage divider resistor
R3			6.0	Mohms	Feedback network, third high voltage divider resistor
R4			161.6	kohms	Feedback network, lower divider resistor
C1			0.495	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
R5			25.5	kohms	Feedback network: zero setting resistor
C2			1000	nF	Feedback component- noise suppression capacitor
Loss Budget (Estimated at VACMIN)					
PFS Losses			6.45	W	Total estimated losses in PFS
Boost diode Losses			1.33	W	Total estimated losses in Output Diode
Input Bridge losses			5.32	W	Total estimated losses in input bridge module
Inductor losses			3.40	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.74	W	Total estimated losses in Output capacitor
EMI choke copper loss			0.50	W	Total estimated losses in EMI choke copper
Total losses			17.24	W	Overall loss estimate
Efficiency			0.94		Estimated efficiency at VACMIN, full load.
CAPZero component selection recommendation					
CAPZero Device			CAP005DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second

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Total Series Resistance (R1+R2)			0.48	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN_RECOMMENDED			680	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2[2]			680	nF	X capacitor after differencial mode choke and before bridge, ratio with Po
LDM_calc			186	uH	estimated minimum differencial inductance to avoid <10kHz resonance in input current
CX1			470	nF	X capacitor before common mode choke, ratio with Po
LCM			10	mH	typical common mode choke value
LCM_leakage			30	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
LDM_Actual			156	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
DCR_LCM	0.10		0.10	Ohms	total DCR of CM choke for estimating copper loss
DCR_LDM	0.10		0.10	Ohms	total DCR of DM choke(or CM #2) for estimating copper loss

Notes:

1) This design is intended for forced air cooling only. By using less strands in the Litz wire (ie. overall smaller O.D.) and running at a higher current density a smaller core size can be used.
2) CX2 can be placed between CM chock and DM choke depending on EMI design requirement.

8 Switching Inductor Specification

8.1 Electrical Diagram

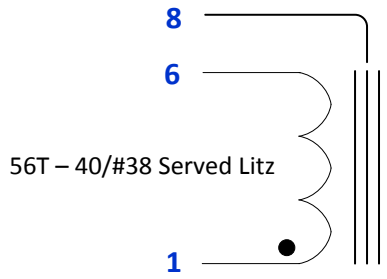

Figure 6 – Inductor Electrical Diagram.

8.2 Electrical Specifications

Inductance	Pins 1-6, measured at 100 kHz, 0.4 $V_{RMS.}$	400 µH ±5%
Resonant Frequency	Pins 1-6.	1300 kHz (Min.)

8.3 Materials

Item	Description
[1]	Core: TDK Core: PC44PQ32/20Z-12, and gapped ALG 137 nH/T^2.
[2]	Bobbin: BPQ32/20-112CPFR - TDK.
[3]	Magnet wire: 40 x #38_Served Litz.
[4]	Bus wire: #24 AWG, connects to pin 8.
[5]	Tape: 3M 1298 Polyester Film, 17.5 mm wide, 2.0 mils thick, or equivalent.
[6]	Varnish: Dolph BC-359, or equivalent.

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8.4 Inductor Build Diagram

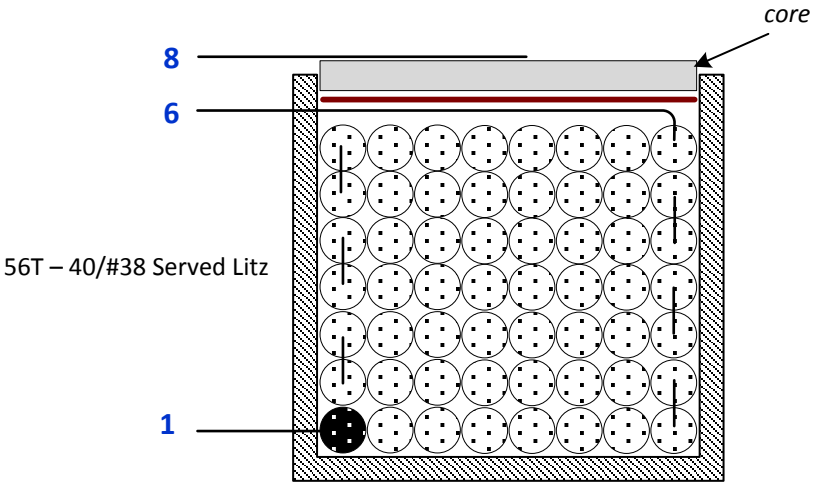
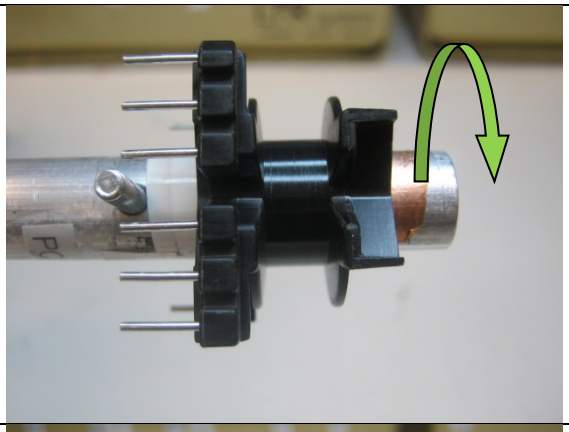
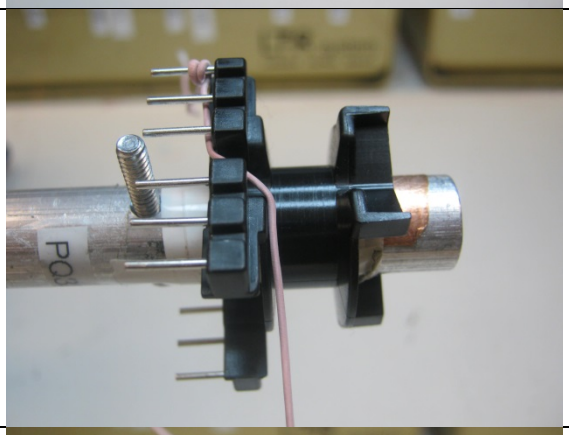
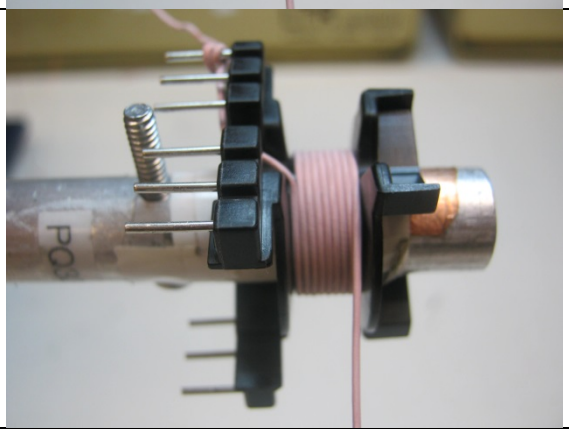


Figure 7 – Inductor Build Diagram.

8.5 Inductor Construction

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding	Start at pin 1, wind 56 turns of wire item [3] in 7 layers (8T/layer). At the last turn, terminate at pin 6. Apply tape item [5] to secure the winding.
Final Assembly	Grind both core center legs equally to get 400 μH. Remove pins 2, 3, 4, 5, 7, 9, 10 and 11. Attach a bare-wire item [4] to the bottom core's surface and wrap tape to secure the wire and core halves. Terminate the bare-wire at pin 8. Varnish with item [6].

8.6 Winding Illustrations

Winding Preparation		Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding		Start at pin 1,
		Wind 56 turns of wire item [3] in 7 layers (8T/layer). At the last turn, terminate at pin 6.

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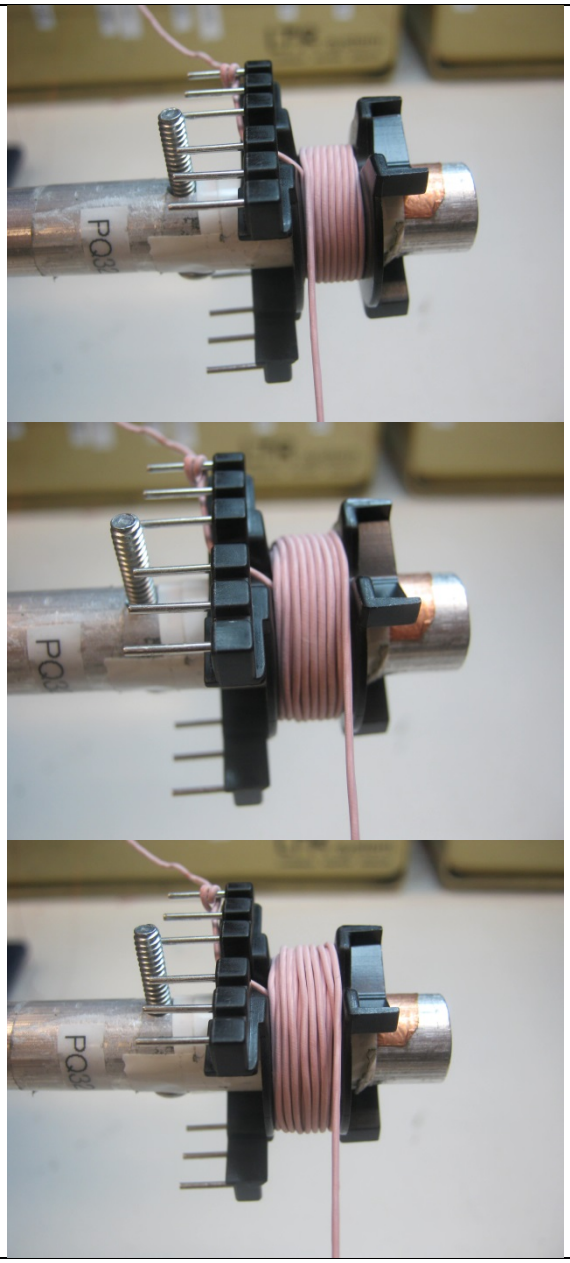
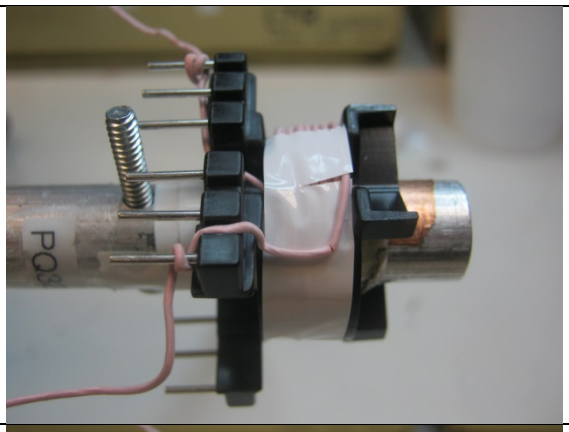
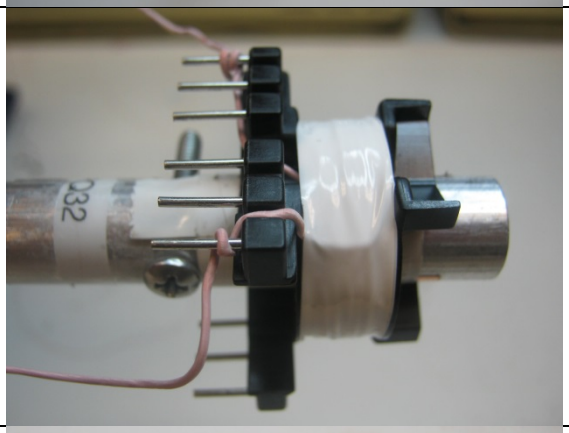
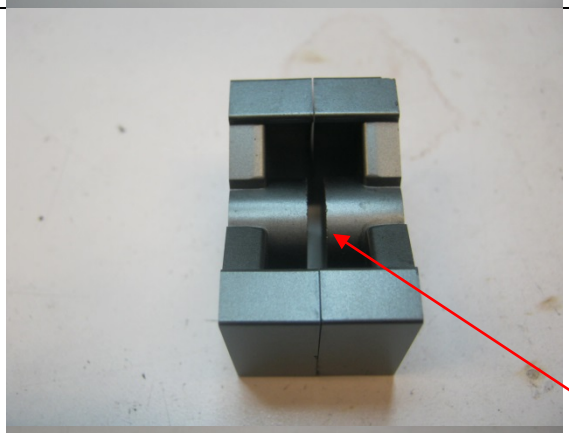
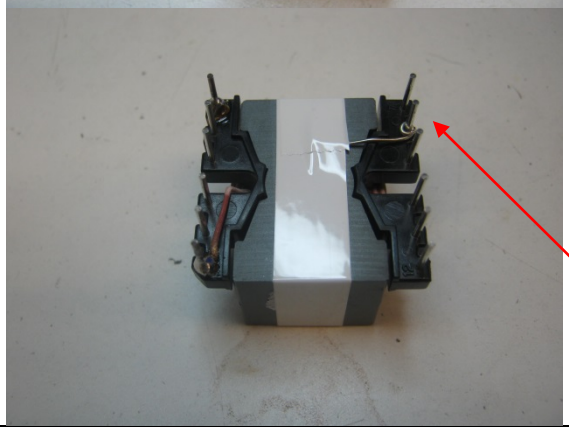


		
		Apply tape item [5] to secure the winding.)
Final Assembly	 	Grind both core center legs equally to get 400 µH. Attach a bare-wire item [4] to the bottom core's surface and wrap tape to secure the wire and core halves. Terminate the bare-wire at pin 8. Remove pins 2, 3, 4, 5, 7, 9, 10 and 11. Varnish with item [6].

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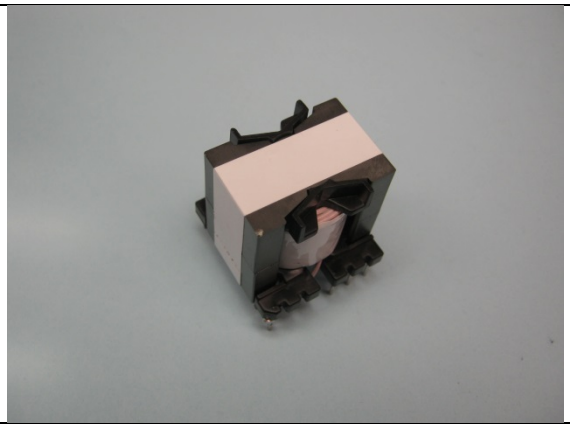
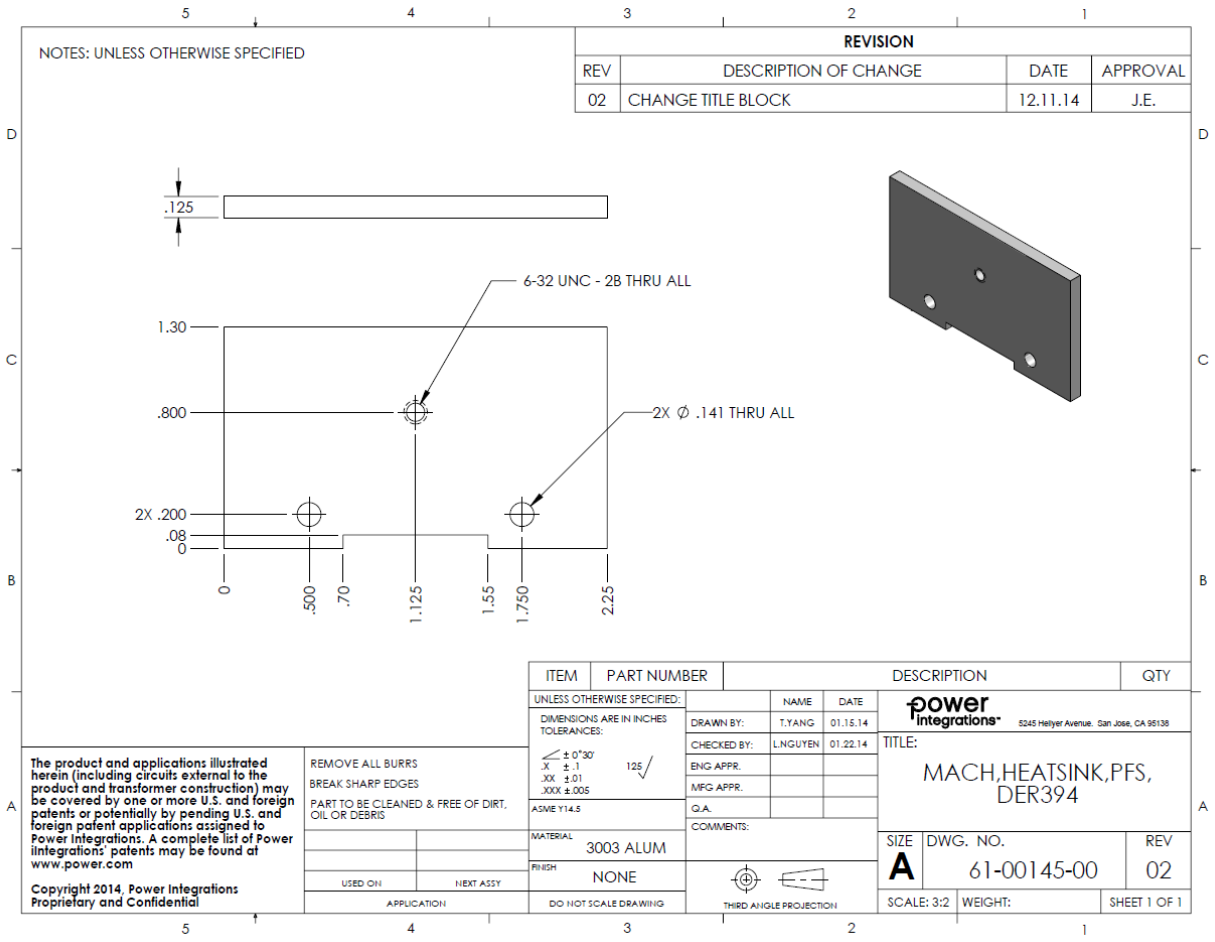


9 eSIP U1 Heat Sink

(Note: The heat sink was designed for operation with forced air cooling for all operation conditions.)

9.1 eSIP U1 Heat Sink Machining Drawing



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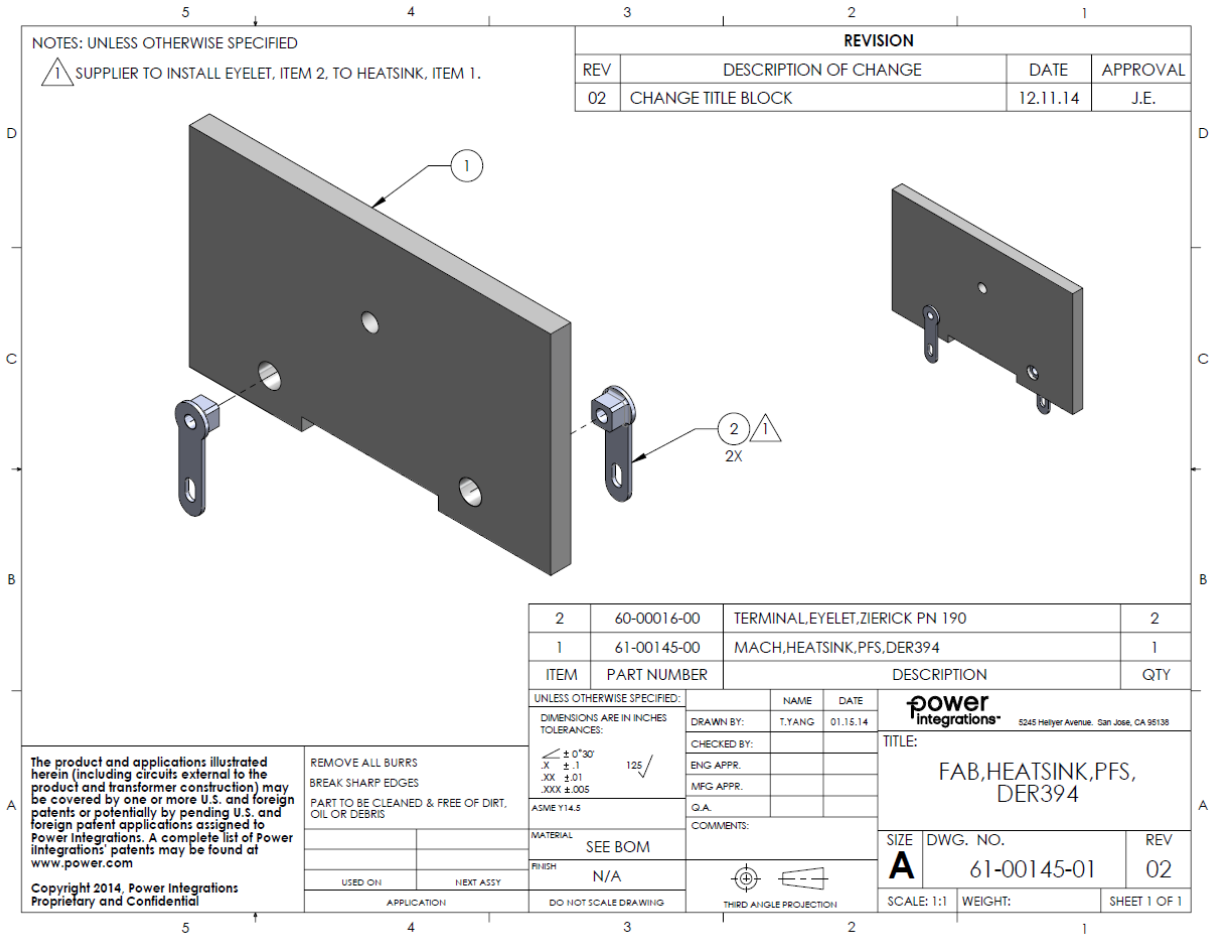
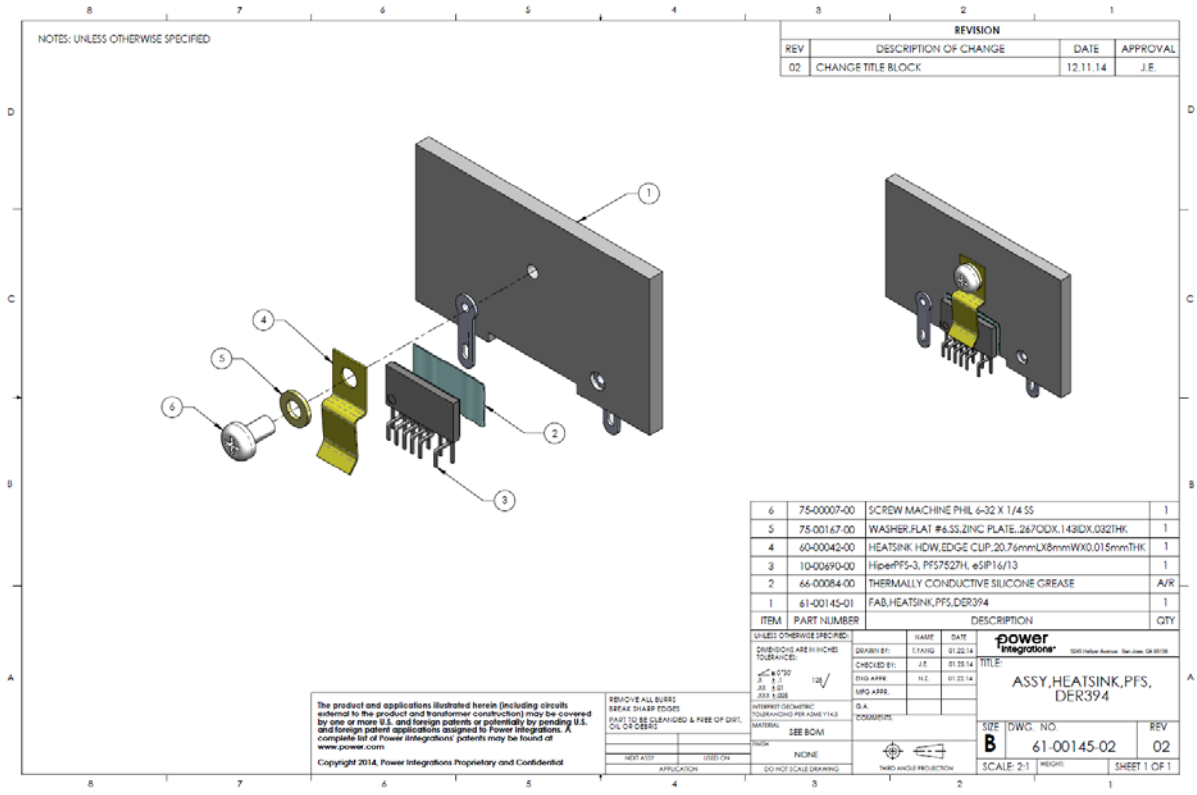
9.2 eSIP U1 Heat Sink Fabrication Drawing



9.3 eSIP U1 Assembly to Heat Sink Drawing



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10 Performance Data

All measurements performed at room temperature, 60 Hz input frequency for voltages below 150 VAC and input frequency of 50 Hz for 150 VAC and higher.

During operation, an 80 mm fan was placed next to the board. Picture of measurement set up can be found in Figures in appendix.

10.1 No-Load/Light Load Input Power

To measure no-load/light load input power, the UUT was operated with the relay and power good disabled by removing Q1 and R4. The contacts of relay RL1 were shorted with a wire jumper to bypass inrush thermistor RT1. Input power was measured using a Yokogawa WT210 set for integration mode, with an integration time of 20 minutes.

The UUT was operated with an auxiliary V_{CC} of 12 V. V_{CC} voltage and current were measured as 12 V and 0.4 mA, resulting in a V_{CC} power consumption of 4.8 mW.

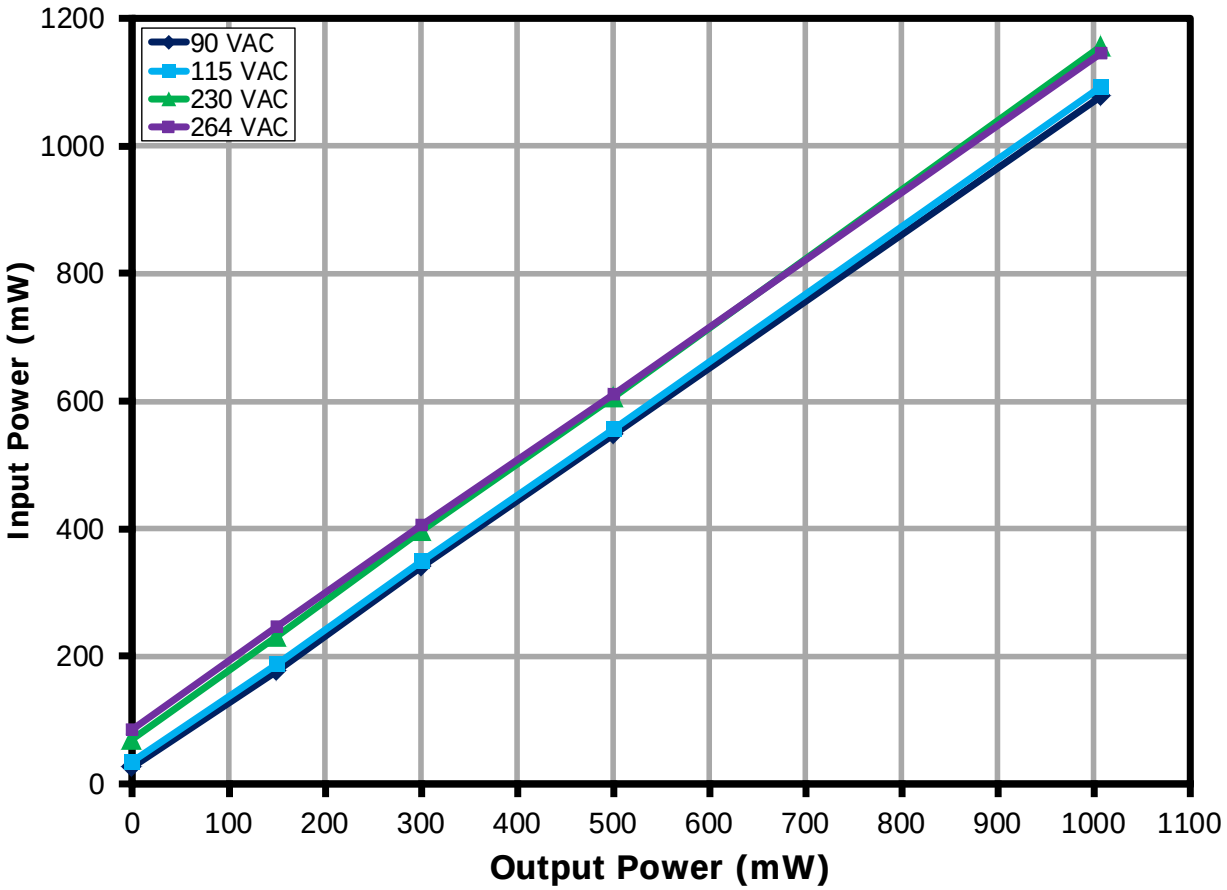

Figure 8 – No-Load/Light Load Input Power (with Vcc Consumption).

90 VAC		115 VAC		230 VAC		264 VAC	
P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)
0	26	0	34	0	69	0	86
151	177	151	188	151	232	151	246
301	341	301	349	301	396	301	405
500	547	500	556	500	607	500	611
1008	1079	1008	1092	1008	1157	1008	1146

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10.2 PFC Efficiency

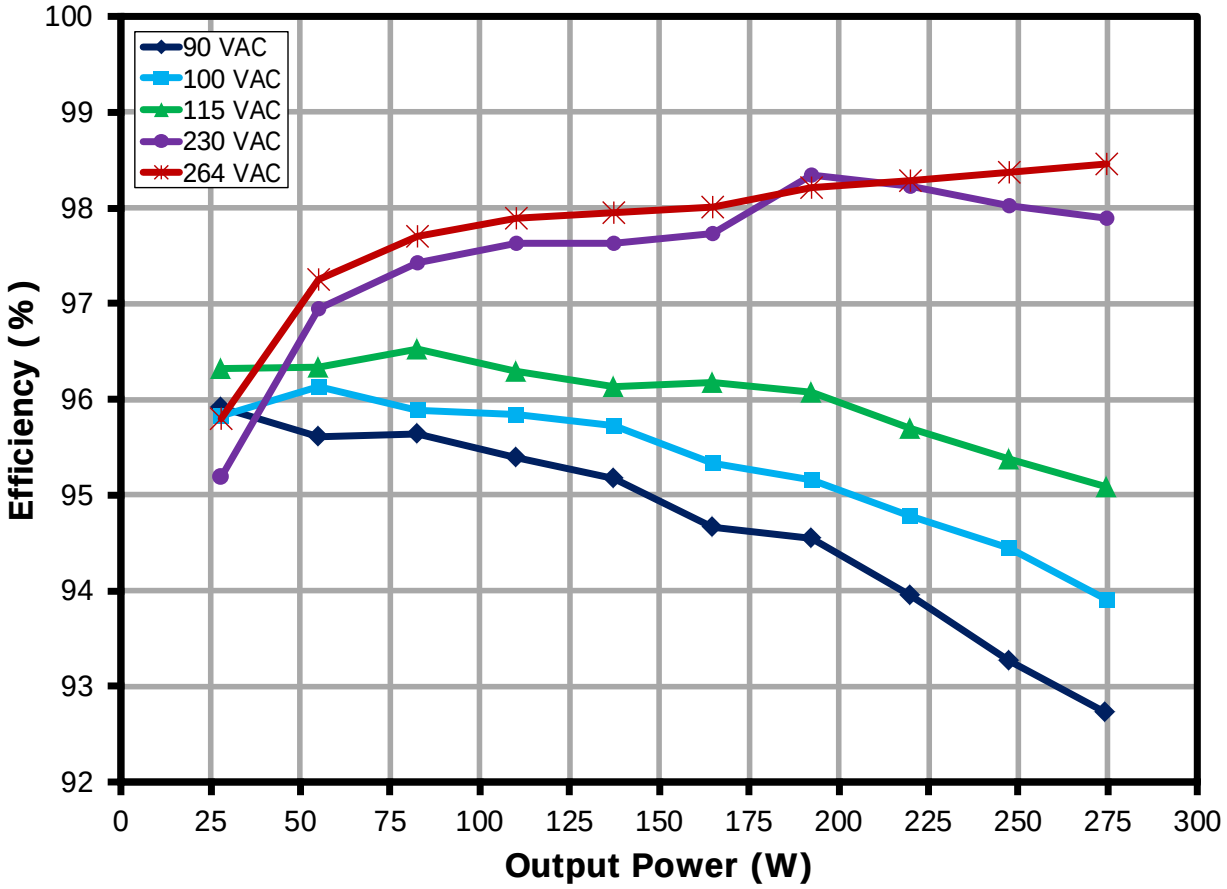

Figure 9 – Efficiency vs. Output Power.

10.3 Input Power Factor

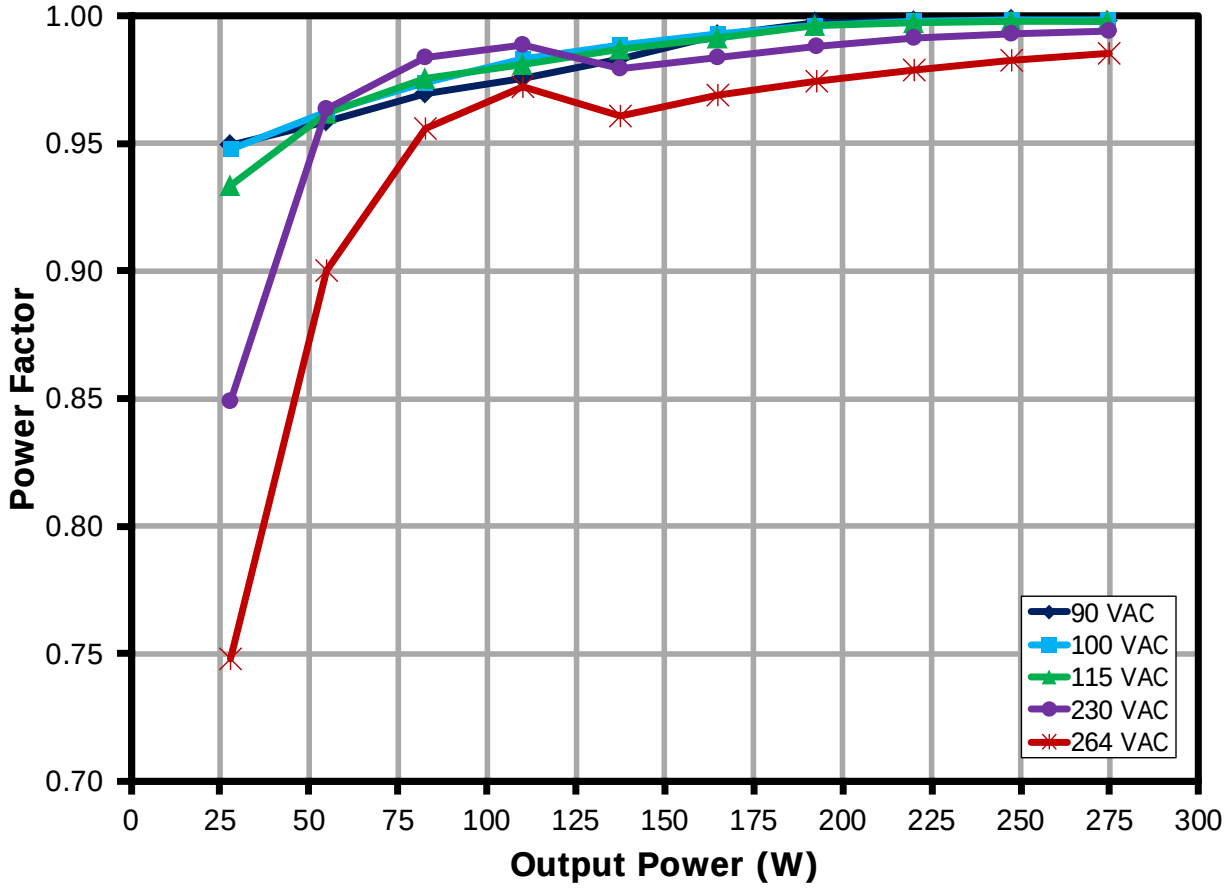

Figure 10 – Input Power Factor vs. Output Power.

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10.4 Regulation

10.4.1 Load Regulation

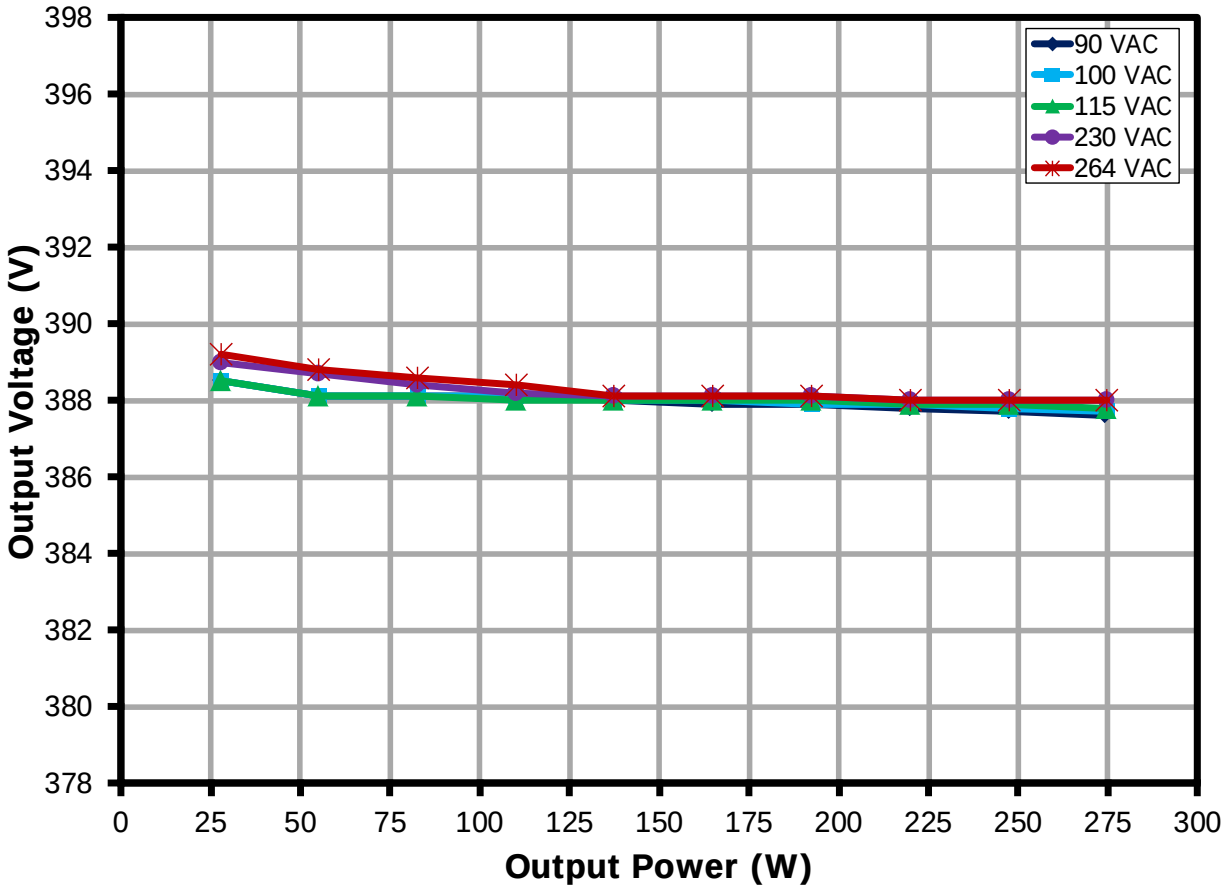

Figure 11 – Load Regulation.

10.4.2 Line Regulation

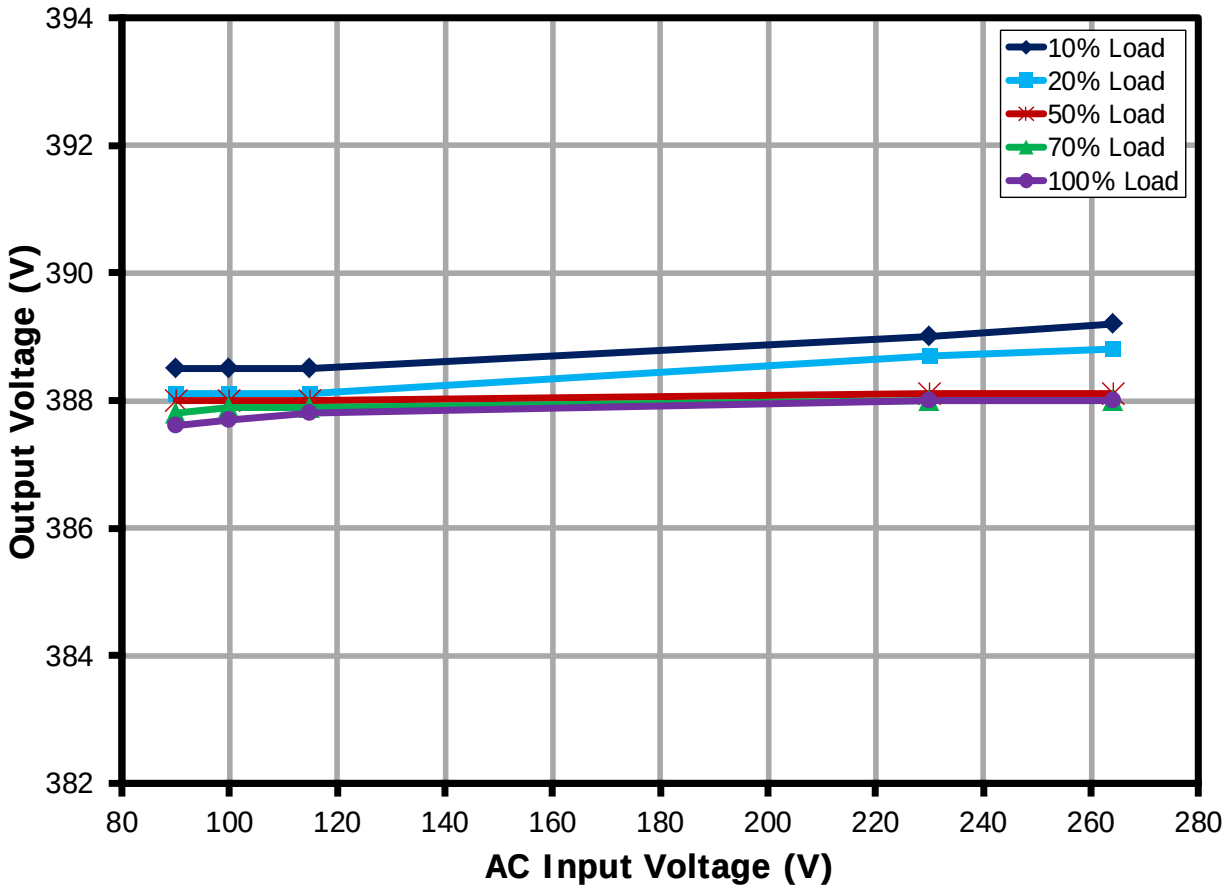

Figure 12 – Line Regulation.

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10.5 Overload

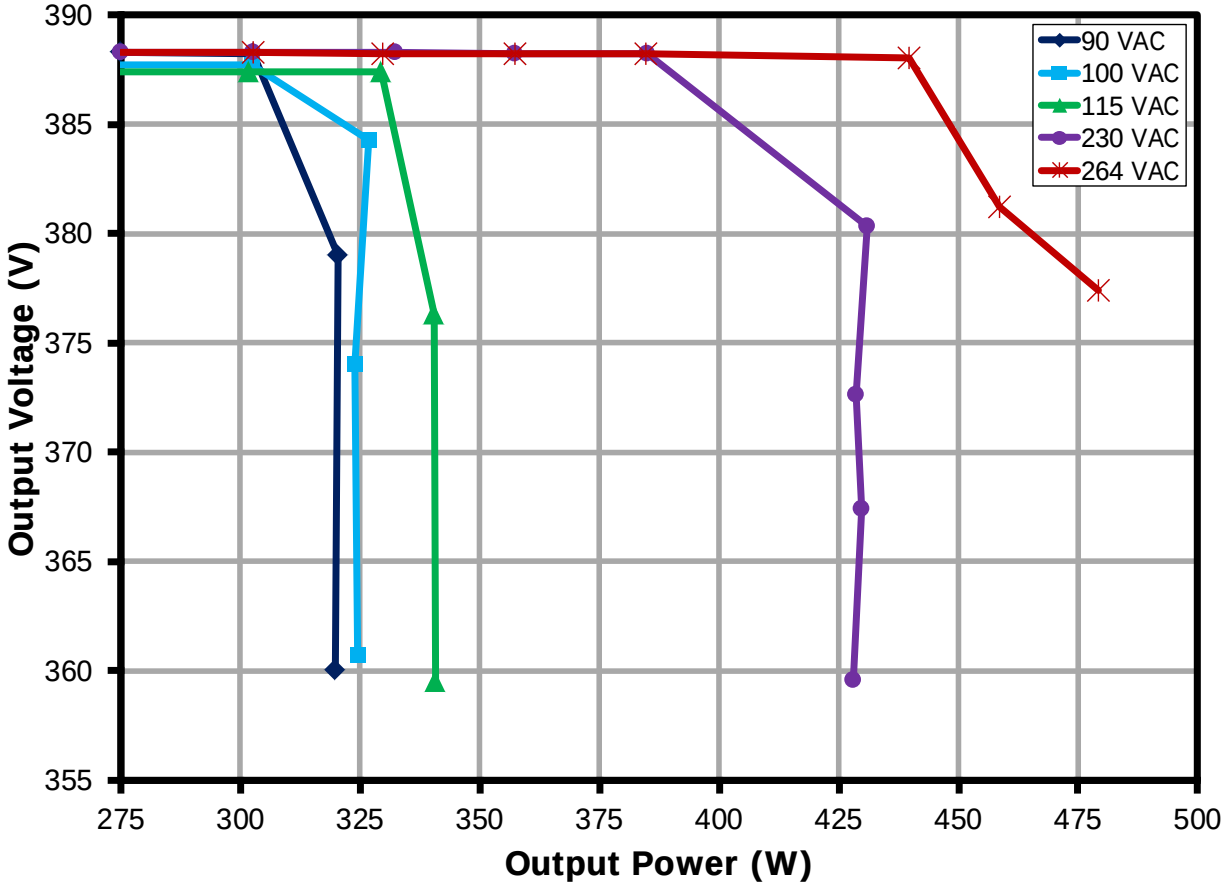

Figure 13 – Overload Regulation.

Note: 275 W is rated full load for this board design.

10.6 THD

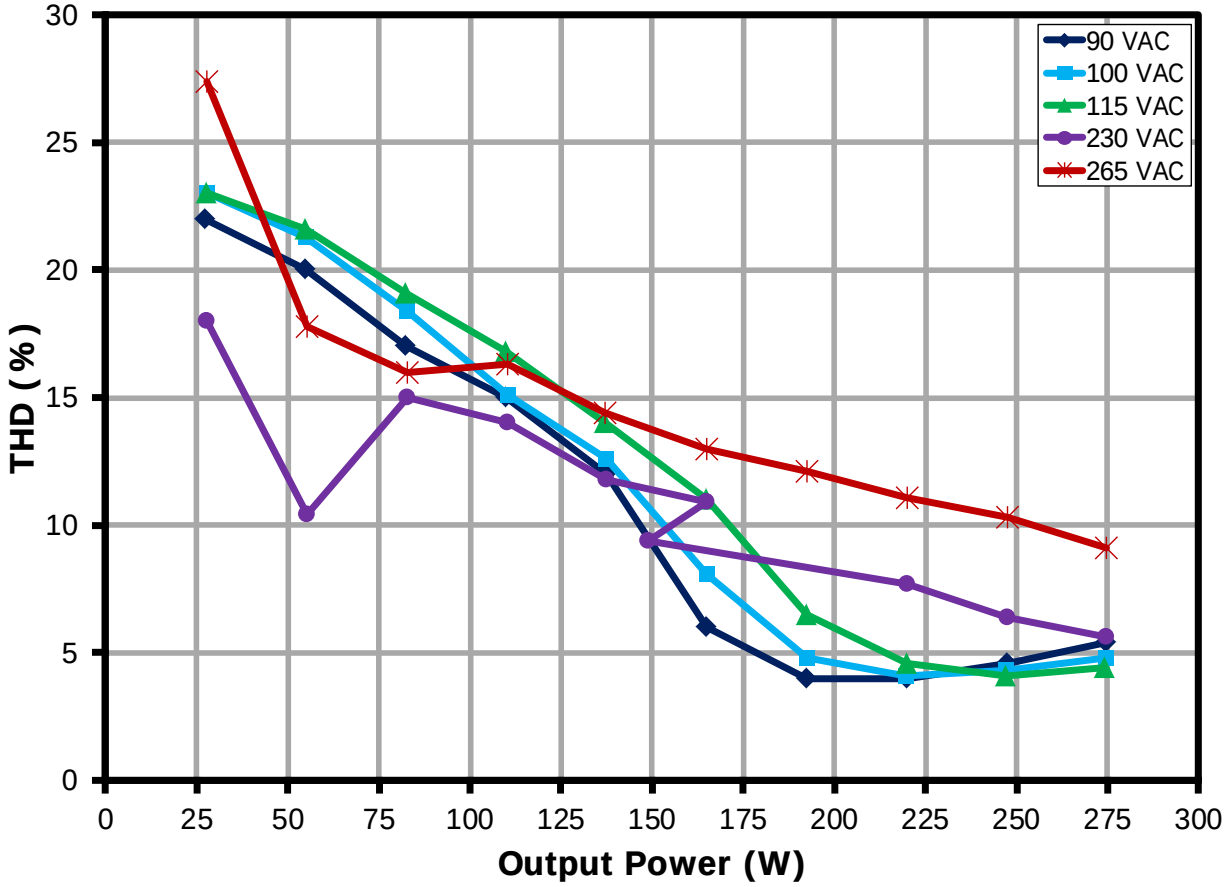

Figure 14 – Input Current THD vs. Load.

Note: When on highline (230 VAC and 264 VAC) and 10% load the unit is bursting making the THD reading very high. To get an accurate reading the light load THD value should be integrated over several minutes.

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10.7 Input Current Harmonic Distortion (IEC 61000-3-2 Class-D)

Measured at 230 VAC Input 50 Hz.

10.7.1 50% Load at Output

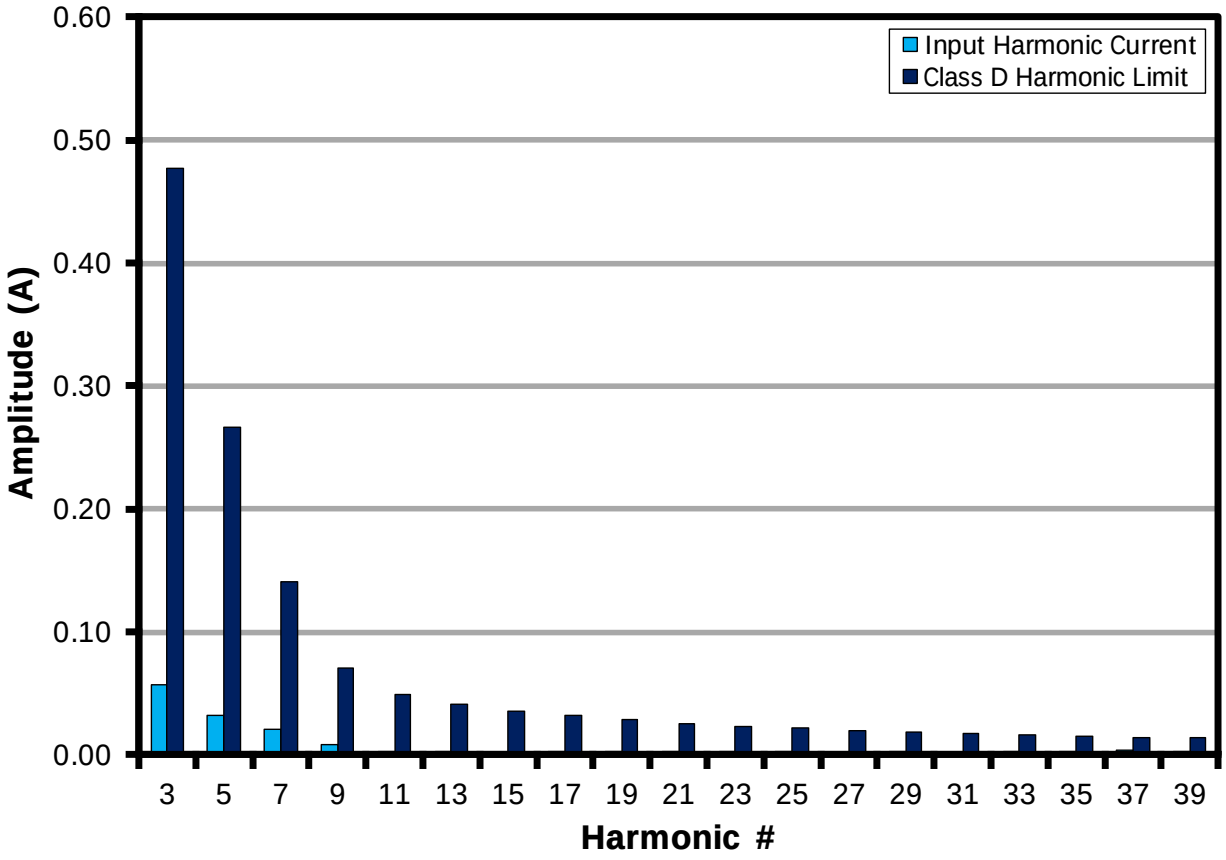

Figure 15 – Amplitude of Input Current Harmonics for 50% Load at 230 VAC Input.

10.7.2 100% Load at Output

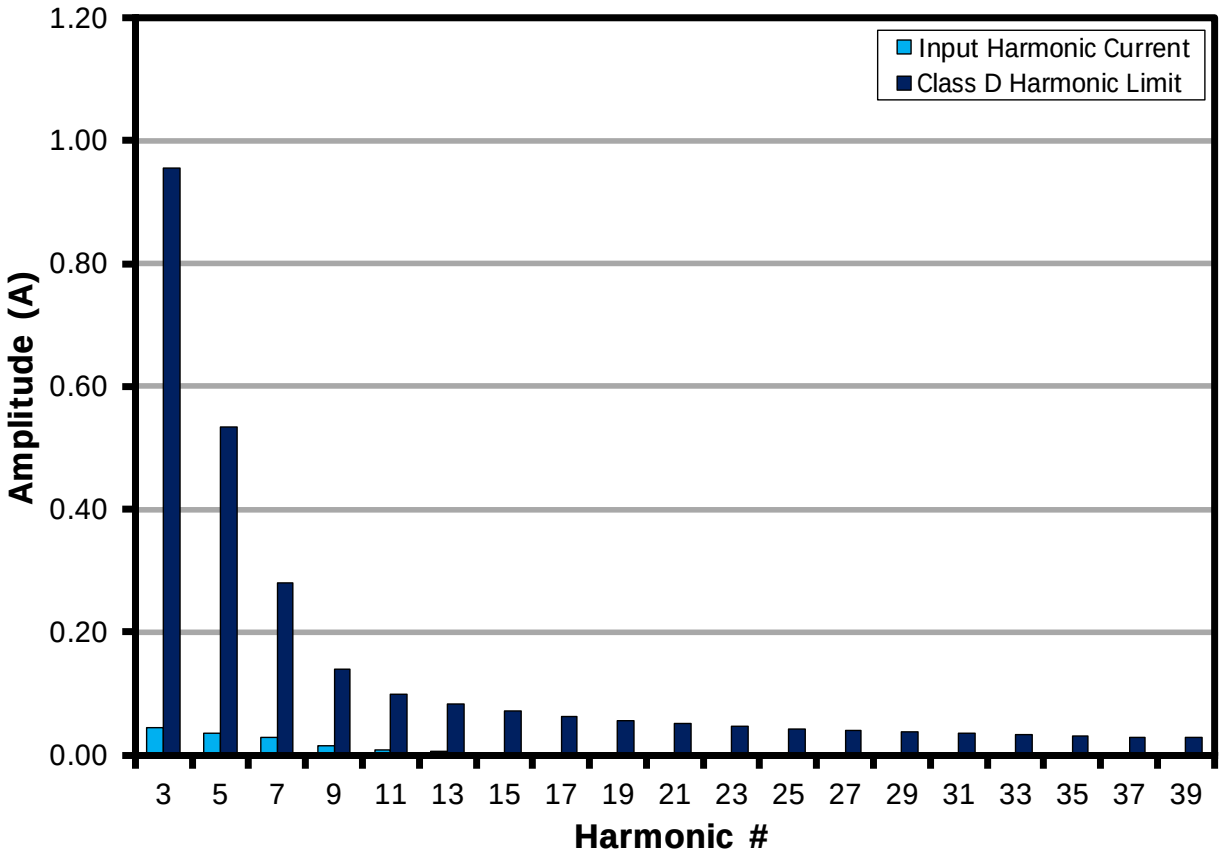

Figure 16 – Amplitude of Input Current Harmonics for 100% Load at 230 VAC Input.

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11 Thermal Performance

A 80 mm 12 VDC fan powered by 10 VDC supply to create a 200 LFM air flow was placed as shown in Appendix 1 with the UUT running at full load. The unit was allowed to reach thermal equilibrium [~2 hrs.] prior to thermal measurement with a FLIR camera. Table 1 shows full load temperature of key components measured at equilibrium, room temperature and with forced air cooling. See Appendix 1 for set-up.

Temperature (ºC) 278 W Load			
Component		**115 VAC**	**230 VAC**
Ambient (measured by FLIR)		21.4	21.1
CM Inductor	L2	29	24,5
DM Inductor	L3	29.1	23.4
Main Inductor	L1 Wire	47.8	31.9
	L1 Core	40.8	29.1
X1 Capacitor	C3	25.7	23.8
X2 Capacitor	C4	26	23.2
Bridge Capacitor	C5	28.4	26.7
Bride Rectifier	BR1	73.6	47.4
Output Capacitor	C13	37.6	29.6
Heat Sink Top (Close to PFS7327H)		52.2	35
PFS7327H	U1 MOSFET	66	39.4
	U1 Diode	56.2	36.6

Table 1 – Steady State Thermal Performance.

11.1 115 VAC Thermal Measurements

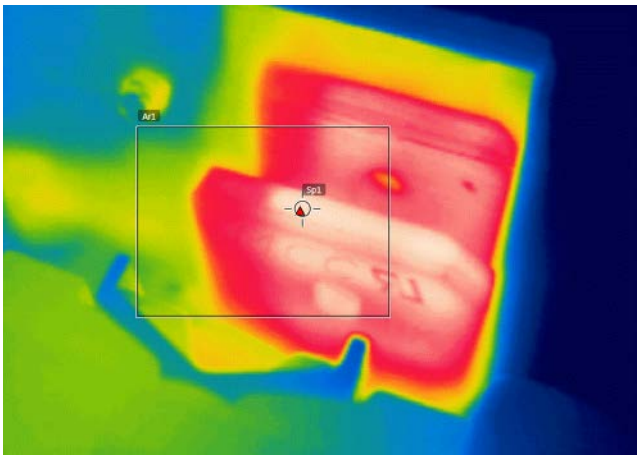

Figure 17 – Infra-Red Images of HiperPFS-3 MOSFET and Diode at Thermal Equilibrium, 115 VAC, Full Load, with Forced-Air Flow.
AR1/SP2: HiperPFS-3 MOSFET Hot Spot = 66 °C.
SP1: HiperPFS-3 Output Diode = 56.2 °C.
SP3: Heat Sink Temperature Near HiperPFS-3 = 52.2 °C.

Figure 18 – Infra-Red Images of Bridge at Thermal Equilibrium, 115 VAC, Full Load, with Forced-Air Flow.
SP1/AR1: BR1 Hot Spot Temperature = 73.6 °C.

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11.2 230 VAC Thermal Measurements

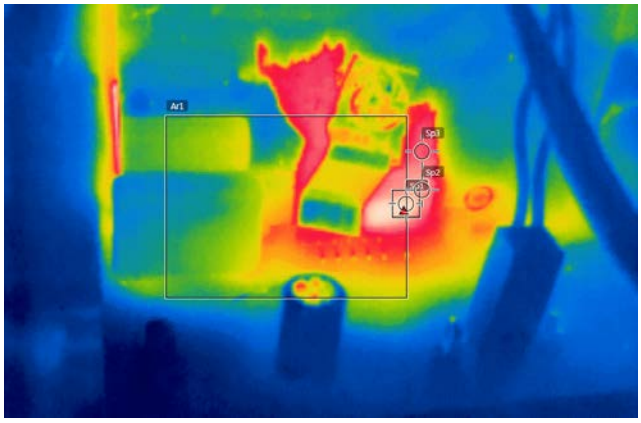

Figure 19 – Infra-Red Images of HiperPFS-3 MOSFET and Diode at Thermal Equilibrium, 230 VAC, Full Load, with Forced-Air Flow.
SP1: HiperPFS-3 MOSFET Hot Spot = 39.4 °C.
SP1: HiperPFS-3 Output Diode = 36.6 °C.
SP3: Heat Sink Temperature Near HiperPFS-3 = 35 °C.

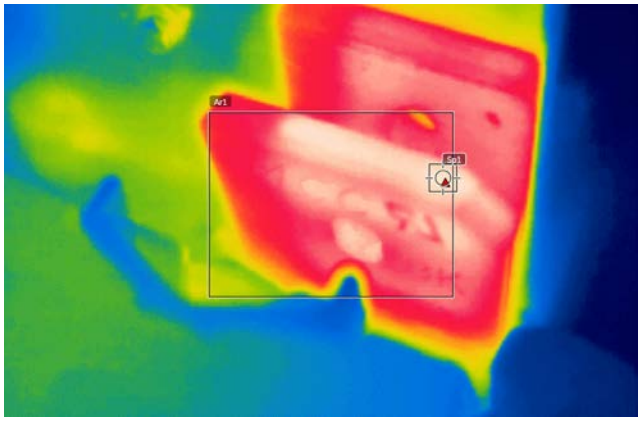

Figure 20 – Infra-Red Images of Bridge at Thermal Equilibrium, 230 VAC, Full Load, with Forced-Air Flow.
SP1/AR1: BR1 Hot Spot Temperature = 47.4 °C.

12 Input Waveforms

12.1 Input Current at 115 VAC and 60 Hz

Figure 21 – 115 VAC, 50% Load.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 1 A / div., 5 ms / div.

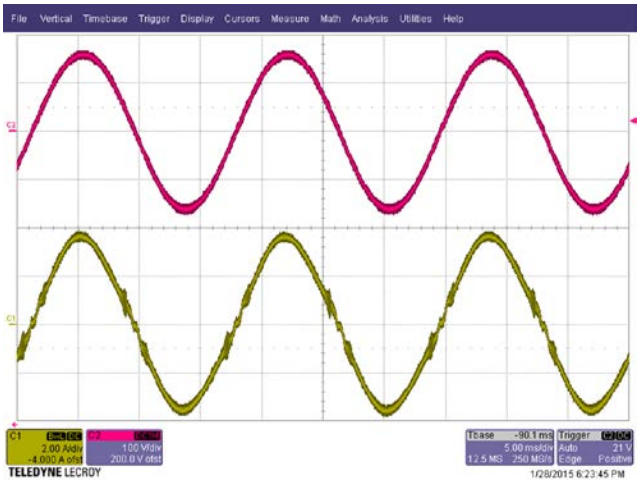

Figure 22 – 115 VAC, 100% Load.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 2A / div., 5 ms / div.

12.2 Input Current at 230 VAC and 50 Hz

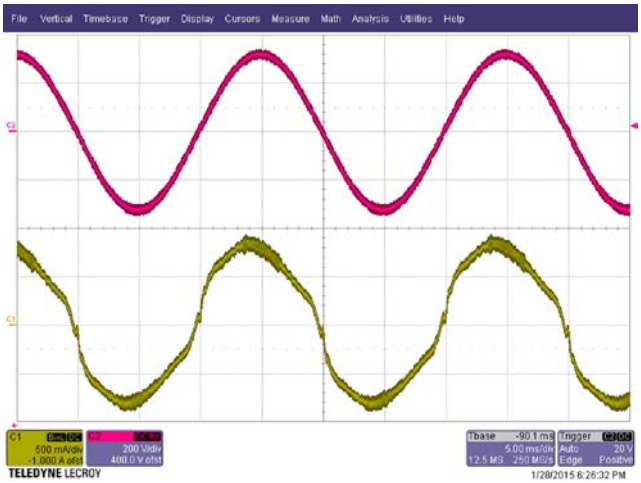

Figure 23 – 230 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 0.5 A / div., 5 ms / div.

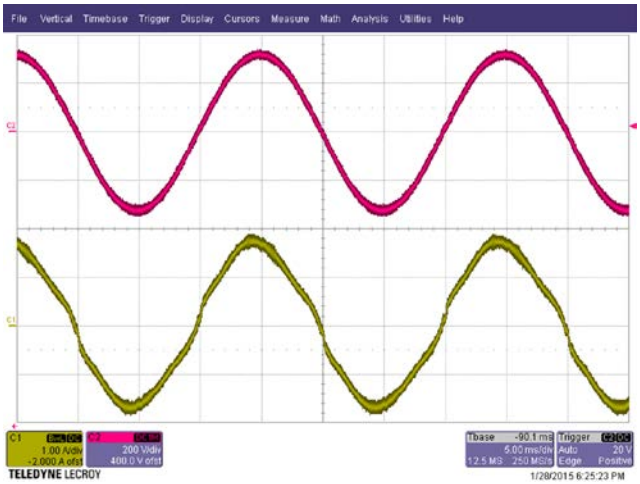

Figure 24 – 230 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 1 A / div., 5 ms / div.

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12.3 Start-up Waveforms

12.3.1 90 VAC and 60 Hz

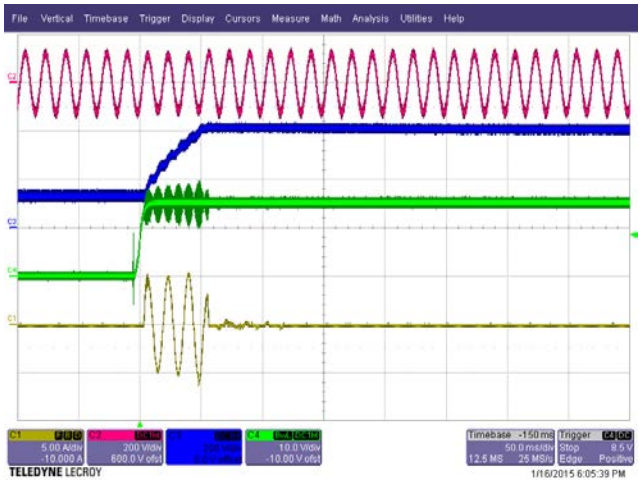

Figure 25 – 90 VAC, No-Load.
Upper: V_{IN}, 200 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

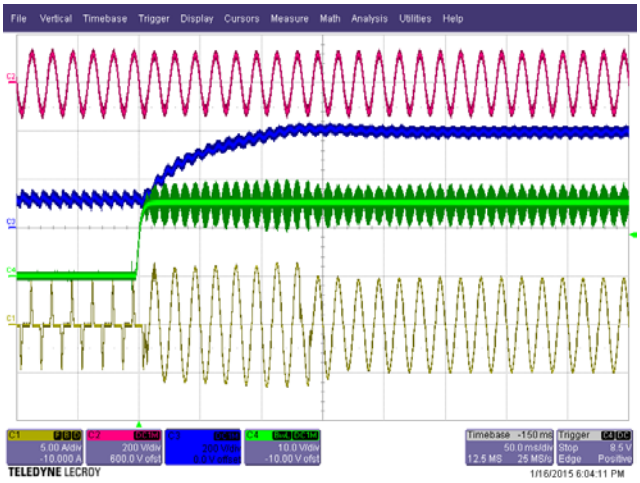

Figure 26 – 90 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

12.3.2 115 VAC and 60 Hz

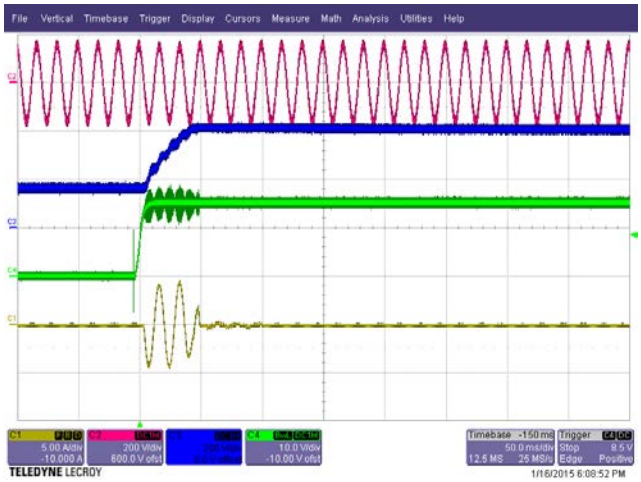

Figure 27 – 115 VAC, No-Load.
Upper: V_{IN}, 200 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

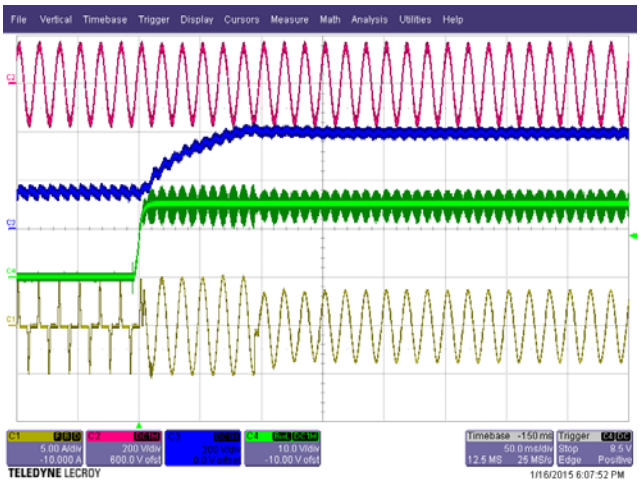

Figure 28 – 115 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

12.3.3 230 VAC and 50 Hz

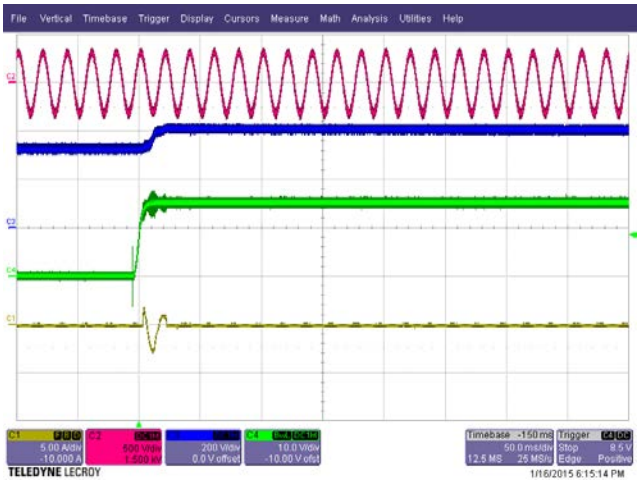

Figure 29 – 230 VAC, No-Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

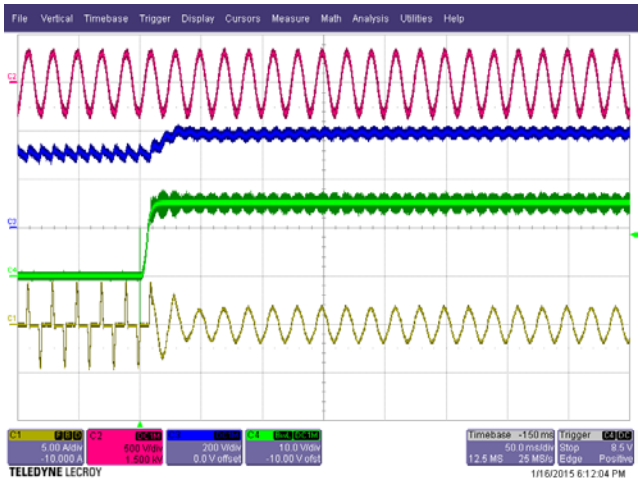

Figure 30 – 230 VAC, Full Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

12.3.4 264 VAC and 50 Hz

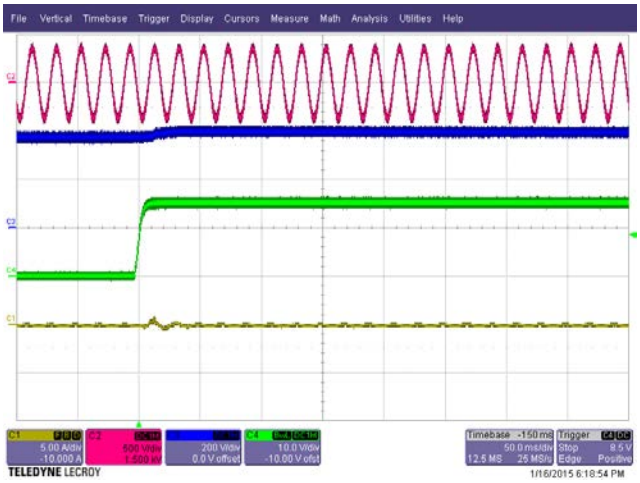

Figure 31 – 264 VAC, No-Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

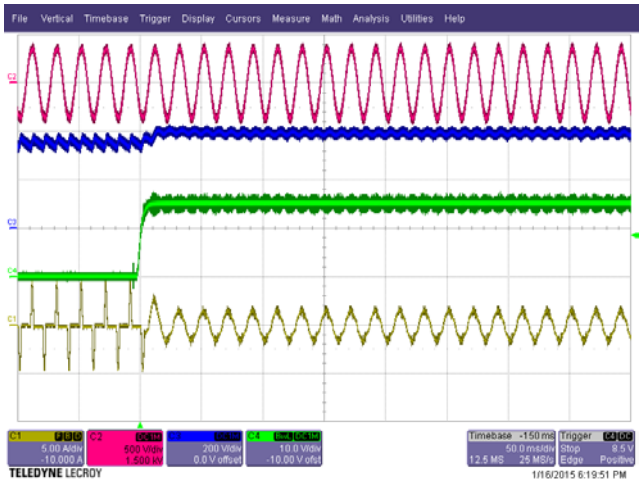

Figure 32 – 264 VAC, Full Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: V_{aux}, 10 V / div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

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12.4 Load Transient Response

12.4.1 90 VAC, 60 Hz

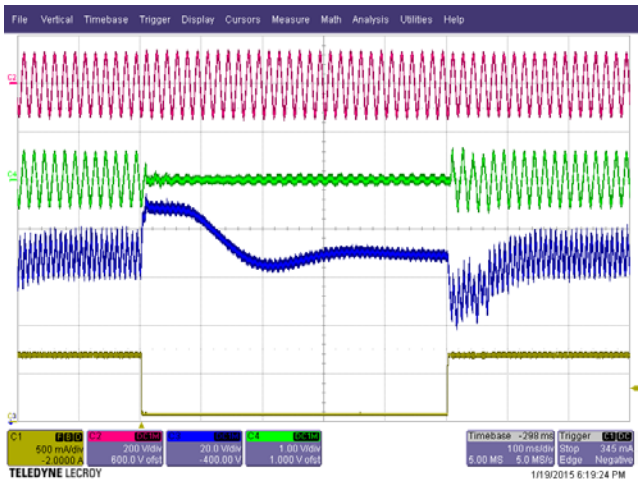

Figure 33 – Transient Response, 90 VAC,
10-100-10% Load Step.
Upper: V_{IN}, 200 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

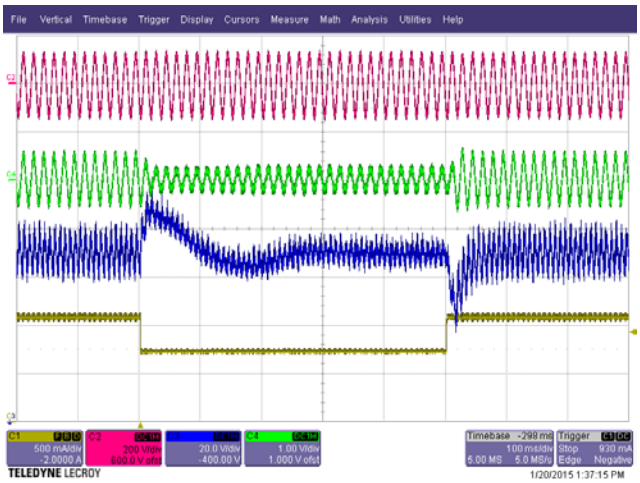

Figure 34 – Transient Response, 90 VAC,
50-100-50% Load Step.
Upper: V_{IN}, 200 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

12.4.2 115 VAC, 60 Hz

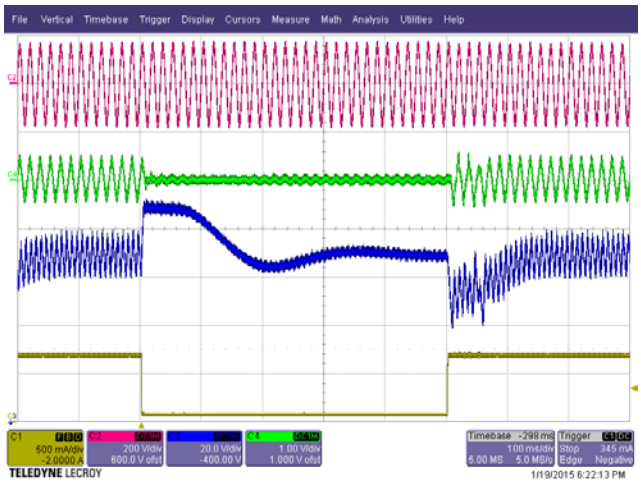

Figure 35 – Transient Response, 115 VAC,
10-100-10% Load Step.
Upper: V_{IN}, 200 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

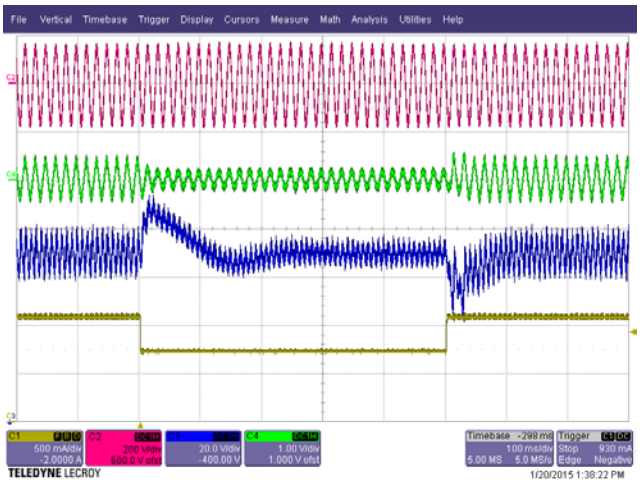

Figure 36 – Transient Response, 115 VAC,
50-100-50% Load Step.
Upper: V_{IN}, 200 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

12.4.3 230 VAC, 50 Hz

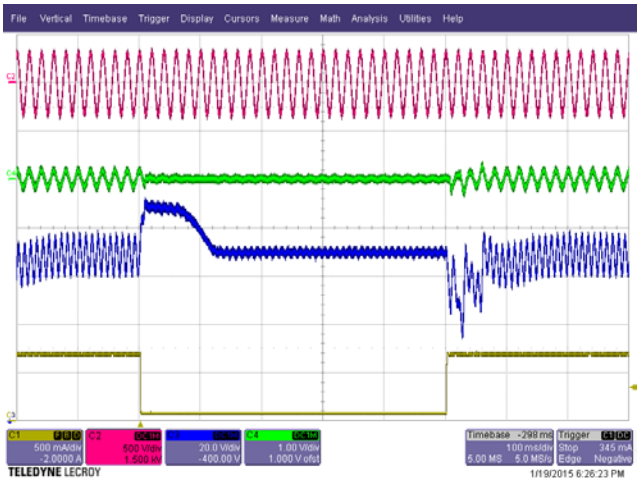

Figure 37 – Transient Response, 230 VAC, 10-100-10% Load Step.
Upper: V_{IN}, 500 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

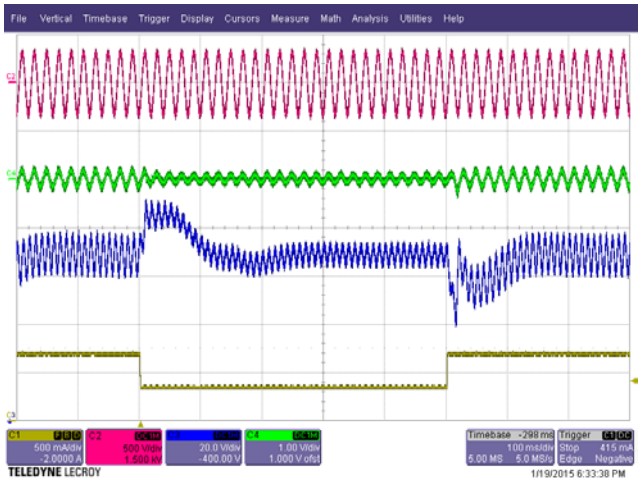

Figure 38 – Transient Response, 230 VAC, 50-100-50% Load Step.
Upper: V_{IN}, 500 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

12.4.4 264 VAC, 50 Hz

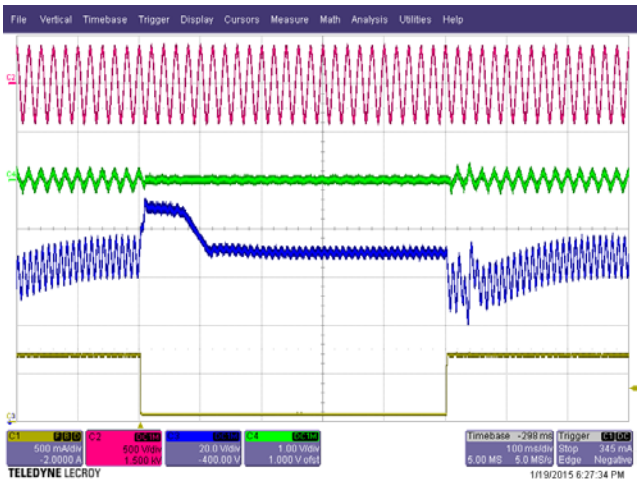

Figure 39 – Transient Response, 264 VAC, 10-100-10% Load Step.
Upper: V_{IN}, 500 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

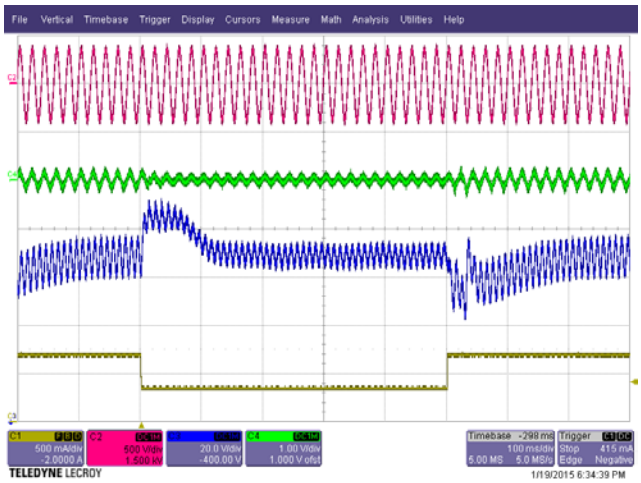

Figure 40 – Transient Response, 264 VAC, 50-100-50% Load Step.
Upper: V_{IN}, 500 V / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (DC Coupled), 20 V / div.
Lower: I_{OUT}, 0.5 A / div., 100 ms / div.

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12.5 Line Dropout

12.5.1 1000 ms Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

12.5.1.1 50% Load at Output

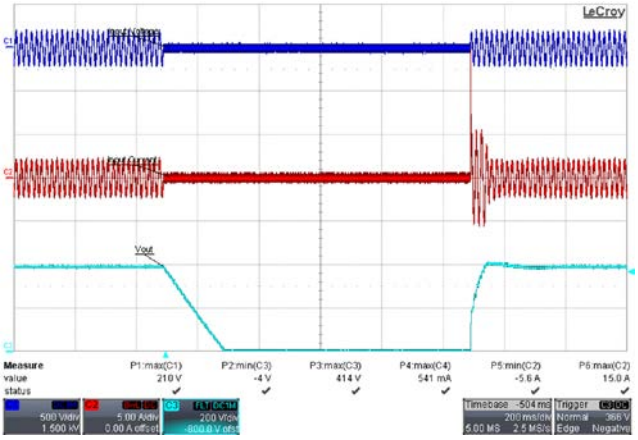

Figure 41 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

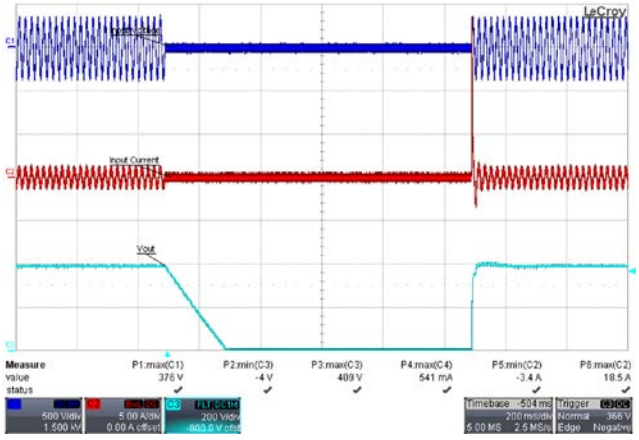

Figure 42 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

12.5.1.2 Full Load at Output

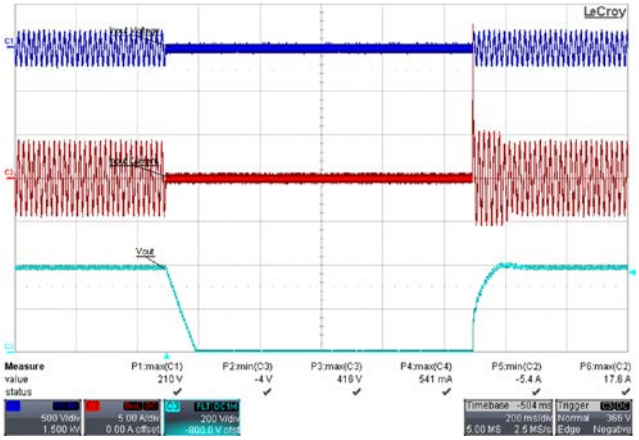

Figure 43 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

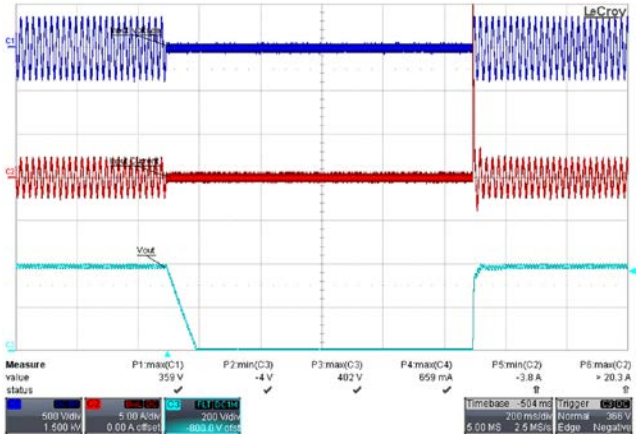

Figure 44 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

12.5.2 One Cycle Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

12.5.2.1 Full Load at Output

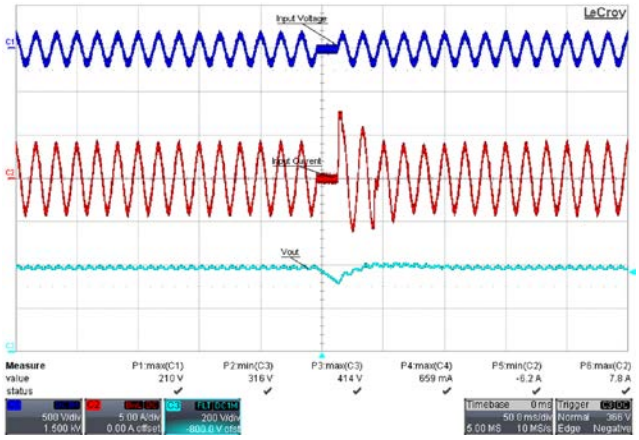

Figure 45 – Line Dropout 115 VAC, 60 Hz.
Upper: V_{IN}, 500 V / div.
Middle:. I_{IN}, 5 A /div.
Lower:, V_{OUT}, 200 V / div., 50 ms / div.

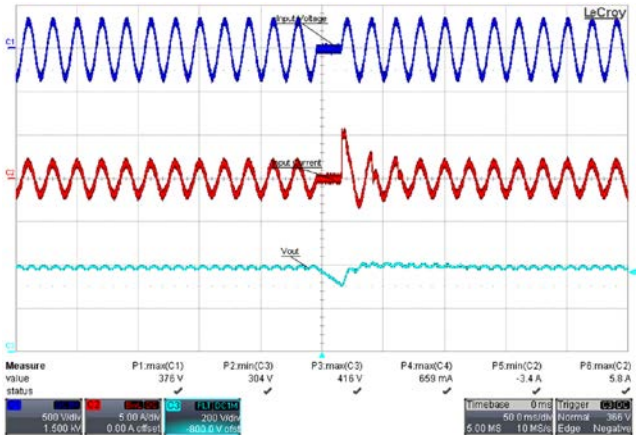

Figure 46 – Line Dropout 230 VAC, 50 Hz.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A /div.
Lower: V_{OUT}, 200 V / div., 50 ms /div.

12.6 Input Line Step

12.6.1 Line Sag (115 VAC ~ 85 VAC ~ 115 VAC, 60 Hz)

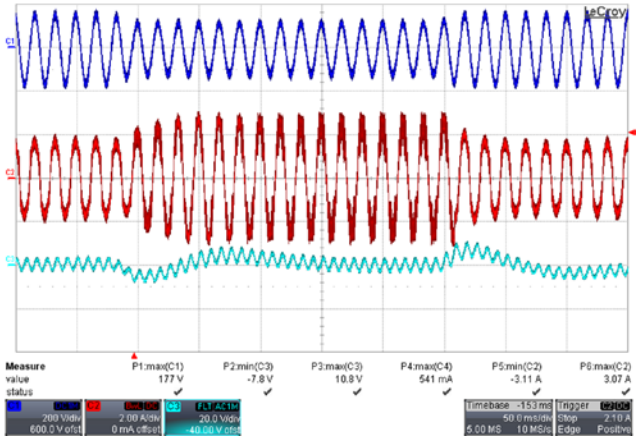

Figure 47 – Line Sag 115 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 2 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

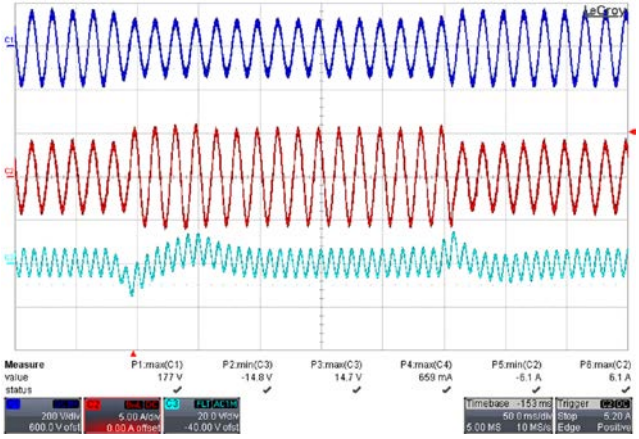

Figure 48 – Line Sag 115 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

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12.6.2 Line Swell (132 VAC ~ 147 VAC ~ 132 VAC, 60 Hz)

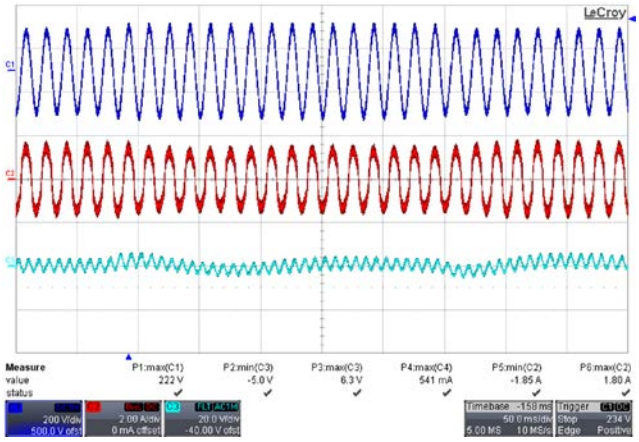

Figure 49 – Line Surge 132 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 2 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

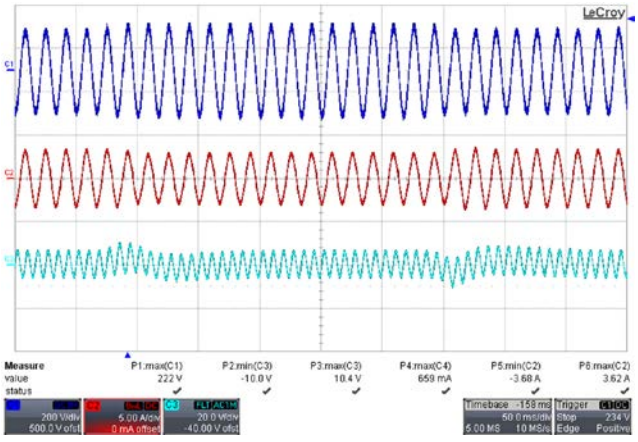

Figure 50 – Line Surge 132 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

12.6.3 Line Sag (230 VAC ~ 170 VAC ~ 230 VAC, 50 Hz)

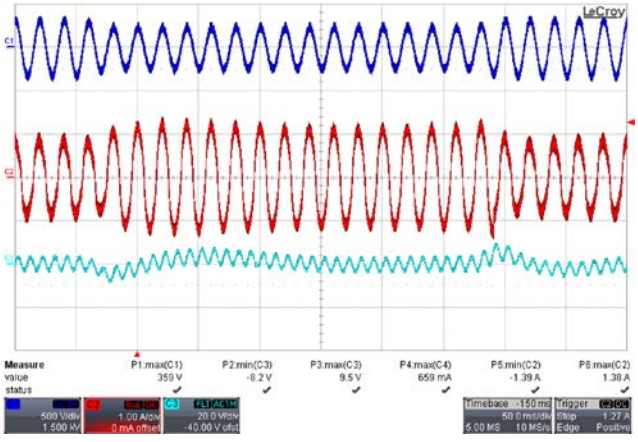

Figure 51 – Line Sag 230 VAC, 50% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 1 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

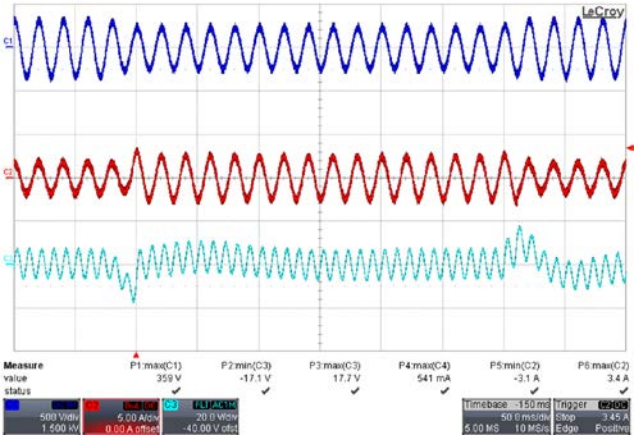

Figure 52 – Line Sag 230 VAC, 100% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

12.6.4 Line Swell (264 VAC ~ 293 VAC ~ 264 VAC, 50 Hz)

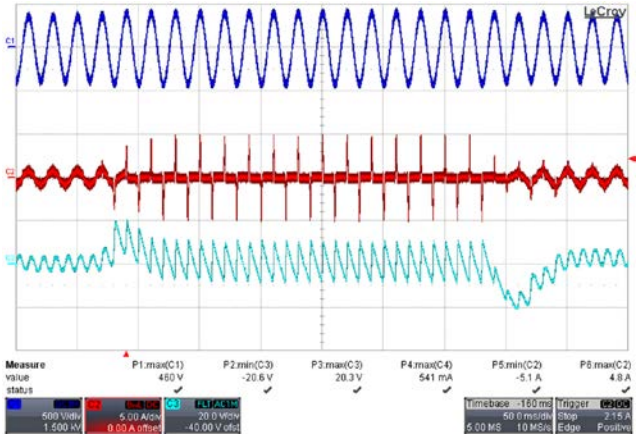

Figure 53 – Line Surge 264 VAC, 50% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

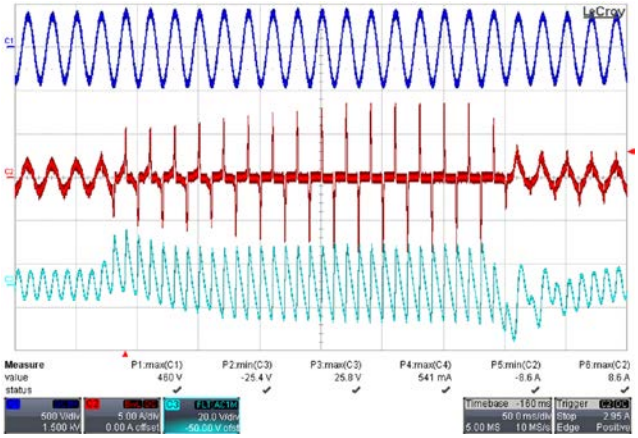

Figure 54 – Line Surge 264 VAC, 100% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50 ms / div.

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12.7 Power Good (PG)

Power Good (PG) waveforms were measured at startup and shutdown with the PG output optocoupler collector (J2-2) tied to the VCC (J4-1) via a 10 kΩ resistor. The PG optocoupler emitter was tied to the VCC return (J4-2).

12.7.1 115 VAC and 60 Hz

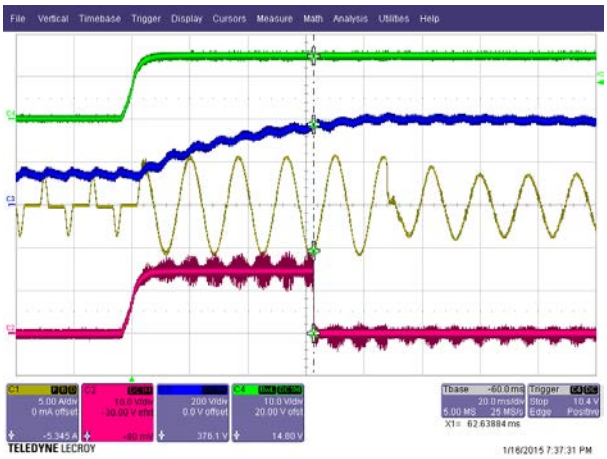

Figure 55 – 115 VAC, Full Load, V_{OUT} Rising Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 5 A / div.
4th: PG, 10 V / div, 20 ms / div.

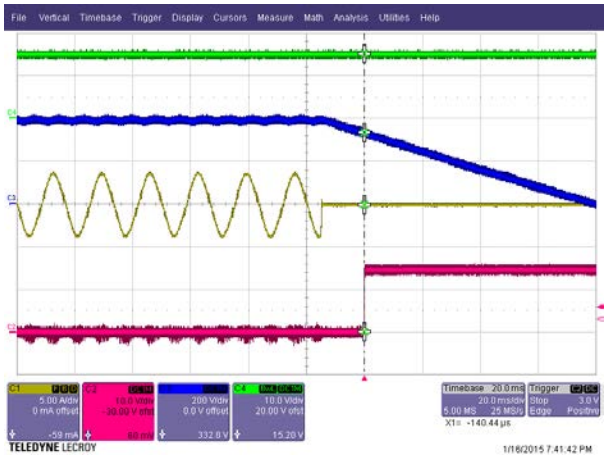

Figure 56 – 115 VAC, Full Load, V_{OUT} Falling Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 5 A / div.
4th: PG, 10 V / div, 20 ms / div.

12.7.2 230 VAC and 50 Hz

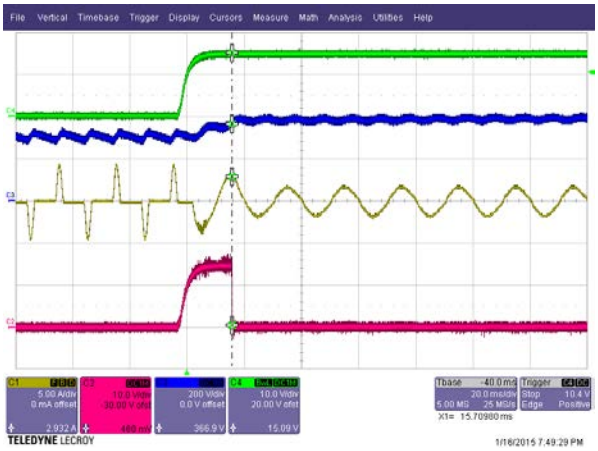

Figure 57 – 230 VAC, Full-load, Vout Rising Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 5 A / div.
4th: PG, 10 V / div, 20 ms / div.

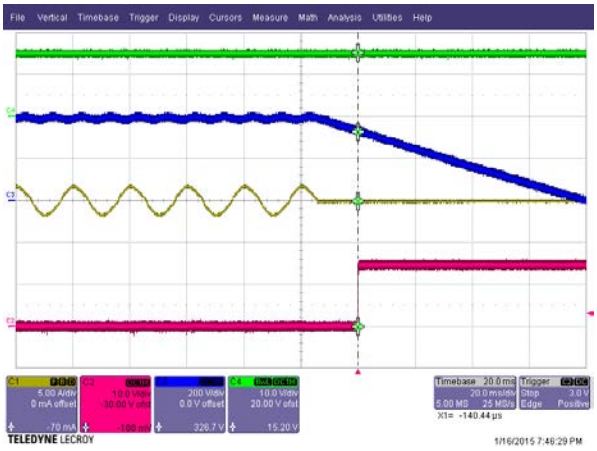

Figure 58 – 230 VAC, Full Load, Vout Falling Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 5 A / div.
4th: PG, 10 V / div, 20 ms / div.

Note: For Figures 54 and 56, input AC voltage was turned off to verify PG transition threshold.

12.8 Brown-In and Brown-Out at 6 V / Minute Rate

Test conducted by first reducing, followed by increasing input AC voltage source at a rate of 6 V / min. The PFC converter DC output was loaded to 100% of rated load (electronic load), which was programmed to release the load when the DC output of the PFC dropped below 310 V [at brown-out]. After the load switches off it continues to draw about 1.5mA and discharges the output capacitor of the PFC after the dynamic load is released at brown-out.

12.8.1 Thresholds

Measured PFC Brown-Out Threshold	71.7 VAC
Measured PFC Brown-In Threshold	80.0 VAC

12.8.2 Waveforms

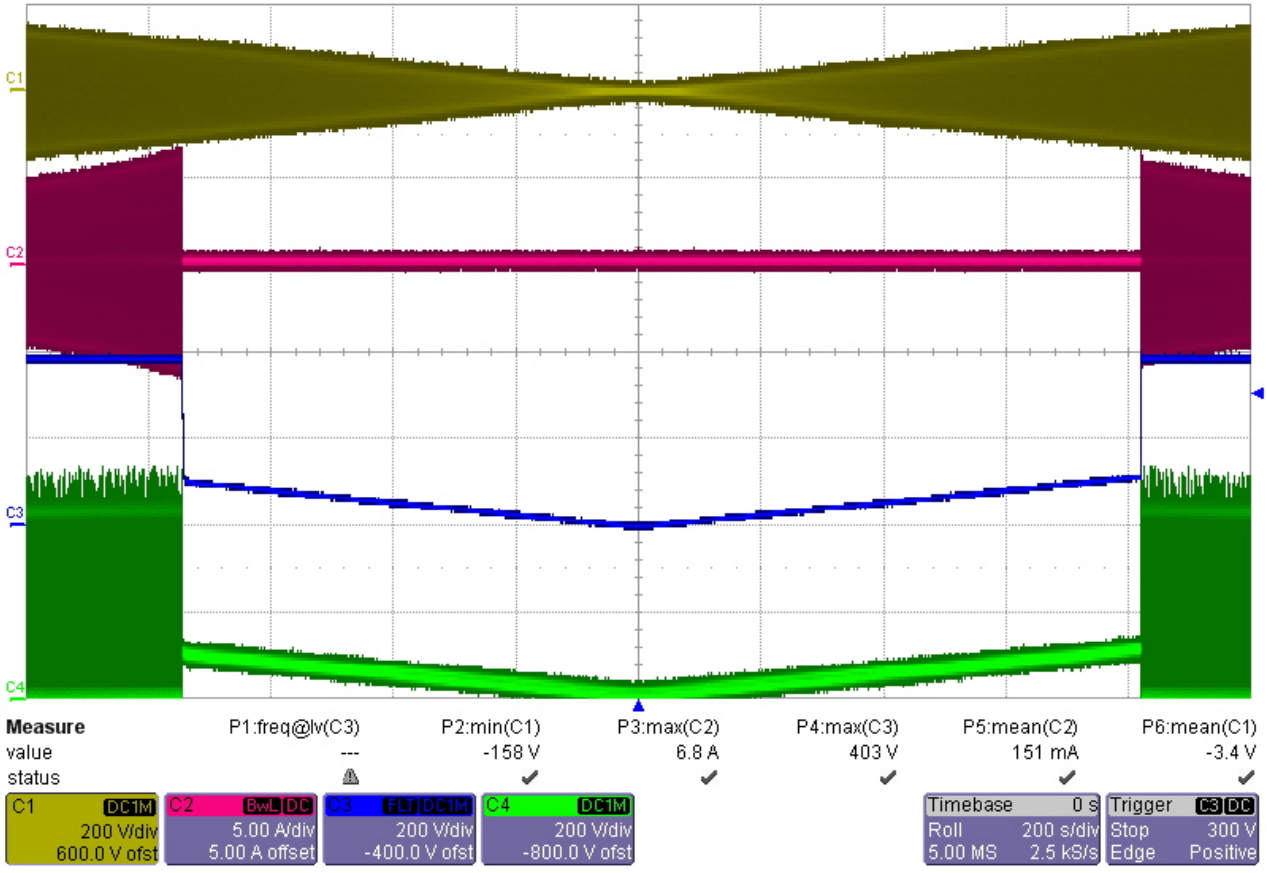

Figure 59 – Brown-Out Followed by Brown-In at 100% Load.
Top: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Third: V_{OUT}, 200 V / div
Lower: V_{ds}, 200 V / div., 200 s / div.

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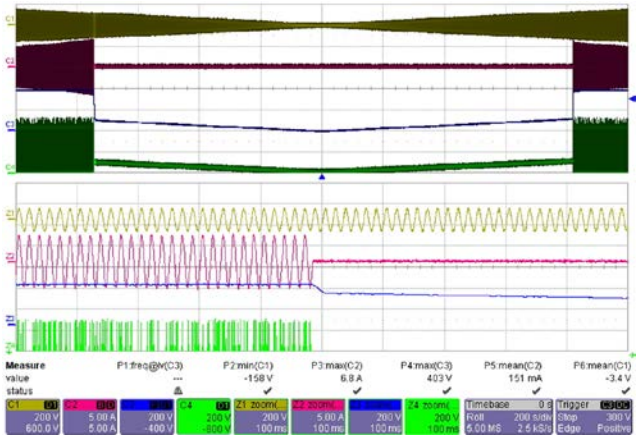

Figure 60 – Brown-out with 100% Load, Zoom-in
Upper (Yellow): V_{IN}, 200 V / div.
Middle (Red): I_{IN}, 5 A / div.
Third (Blue): V_{OUT}, 200 V / div.
Lower (Green): V_{DS}, 200 V / div. Zoom in 100 ms / div.

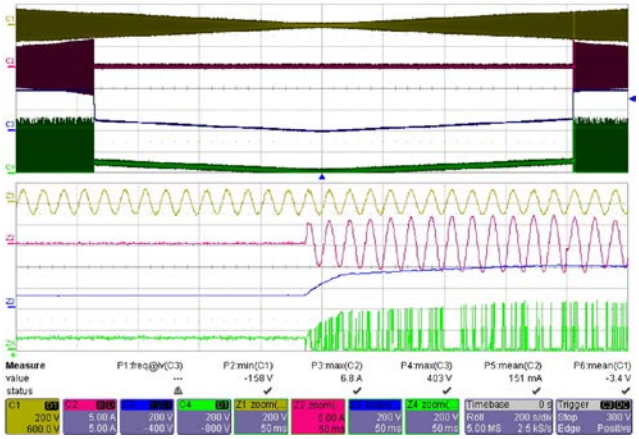

Figure 61 – Brown-in with 100% Load, Zoom-in
Upper (Yellow): V_{IN}, 200 V / div.
Middle (Red): I_{IN}, 5 A / div.
Third (Blue): V_{OUT}, 200 V / div.
Lower (Blue): V_{DS}, 200 V / div, 50 ms / div.

12.8.3 Drain Voltage and Inductor Current

Since PFC output diode is integrated into the package, there is no direct access of the MOSFET drain current. Therefore inductor current was measured at jumper JP1 location by replacing JP1 with a short wire loop in order to insert the current probe. The Drain voltage was measured at the DRAIN and SOURCE pins of IC U1.

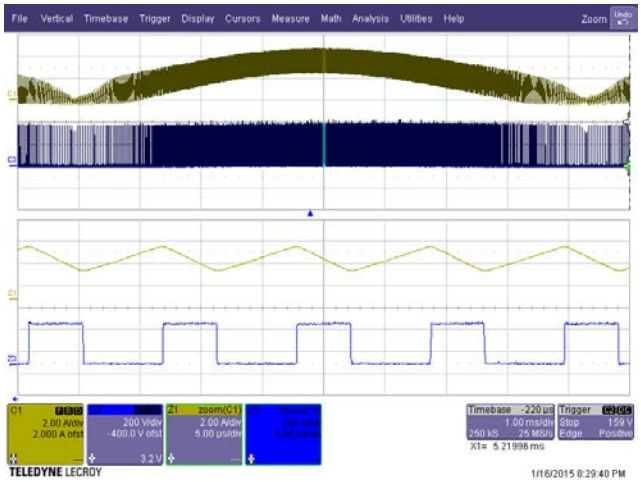

Figure 62 – Input Voltage 115 VAC, 100% Load.
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN}, 200 V / div., 1 ms / div.
Zoom Upper: $I_{INDUCTOR}$, 2 A / div.
Zoom Lower: V_{DRAIN}, 200 V / div., 5 μs / div.

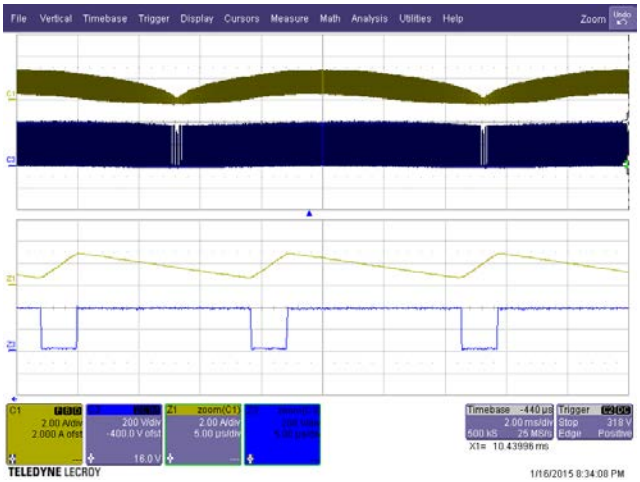

Figure 63 – Input Voltage 230 VAC, 100% Load.
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN}, 200 V / div., 2 ms / div.
Zoom Upper: $I_{INDUCTOR}$, 2 A / div.
Zoom Lower: V_{DRAIN}, 200 V / div., 5 μs / div.

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12.9 Output Ripple Measurements

12.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with one capacitor 0.02 μF/1 kV ceramic disc type tied in parallel across the probe tip.

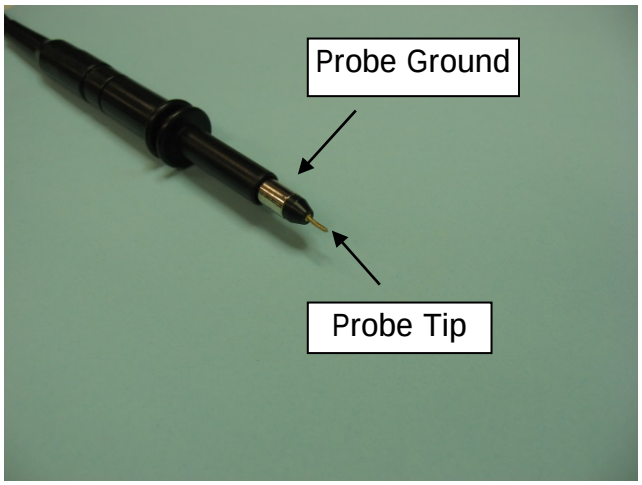

Figure 64 – Oscilloscope Probe Prepared for Ripple Measurement (End cap and ground lead removed.)

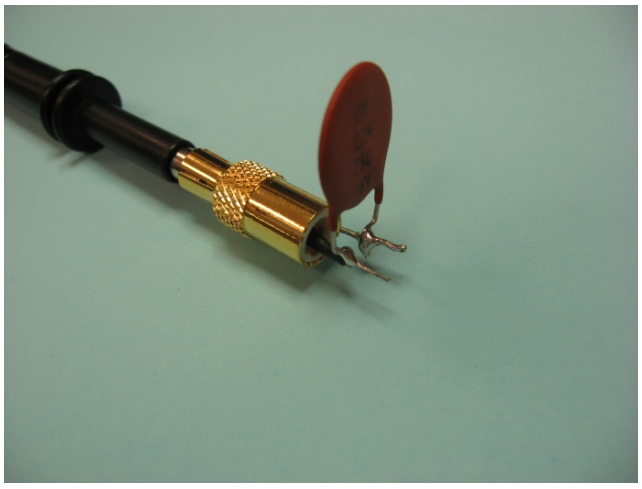

Figure 65 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter (Modified with wires for ripple measurement, and one parallel decoupling capacitor added.)

12.9.2 Measurement Results

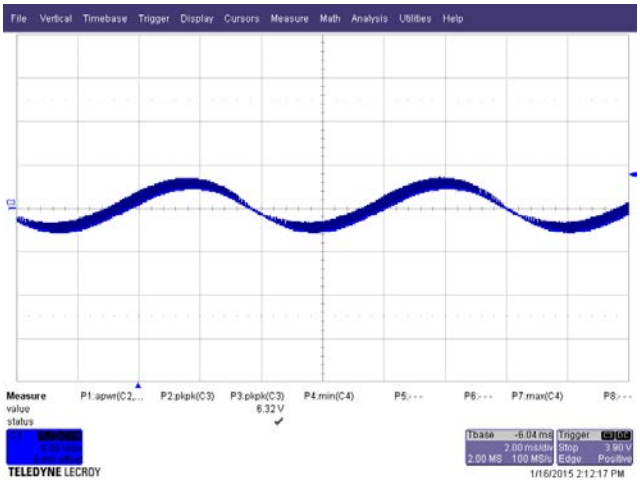

Figure 66 – Ripple, 90 VAC, 50% Load.
5 V / div., 2 ms / div.

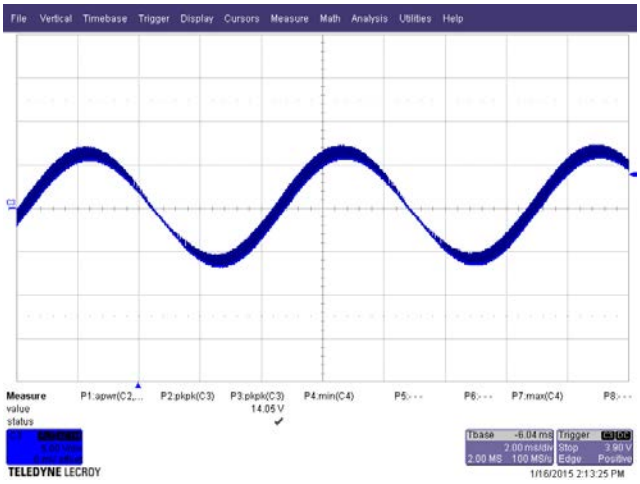

Figure 67 – Ripple, 90 VAC, 100% Load.
5 V / div., 2 ms / div.

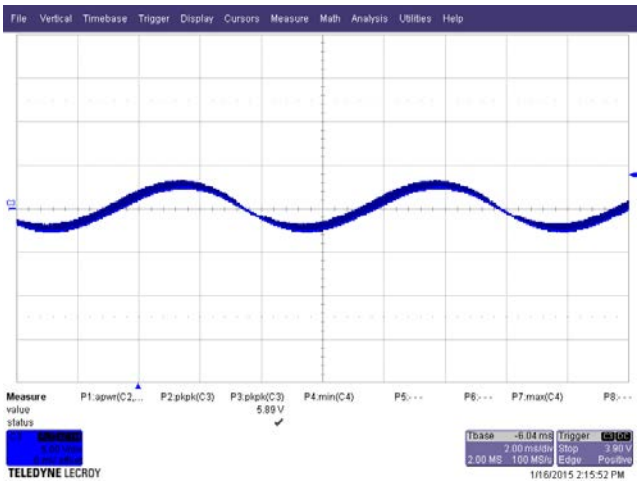

Figure 68 – Ripple, 115 VAC, 50% Load.
5 V / div., 2 ms / div.

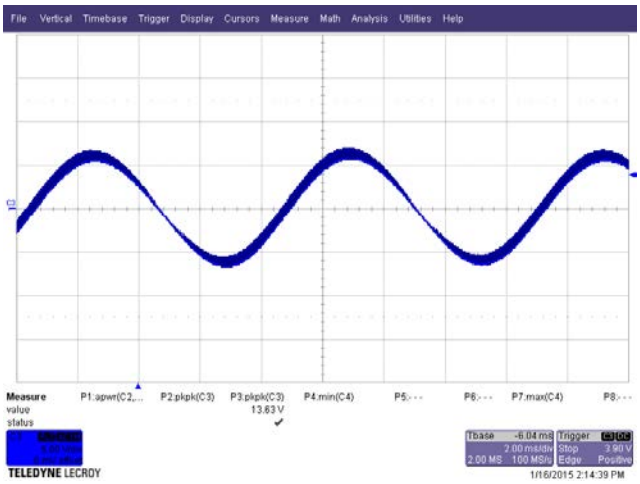

Figure 69 – Ripple, 115 VAC, 100% Load.
5 V / div., 2 ms / div.

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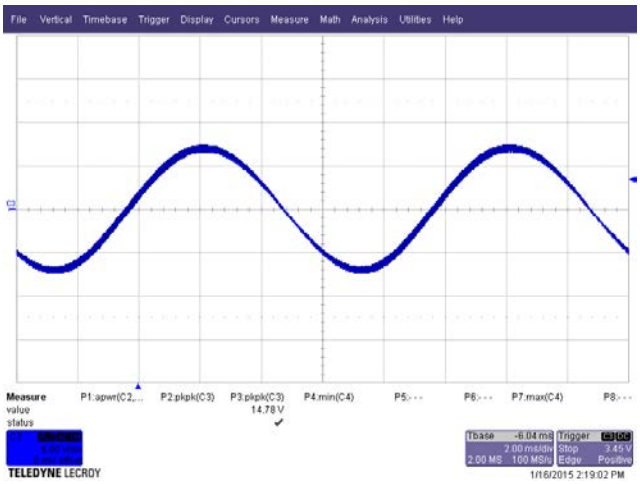

Figure 70 – Ripple, 230 VAC, 50% Load.
5 V / div., 2 ms / div.

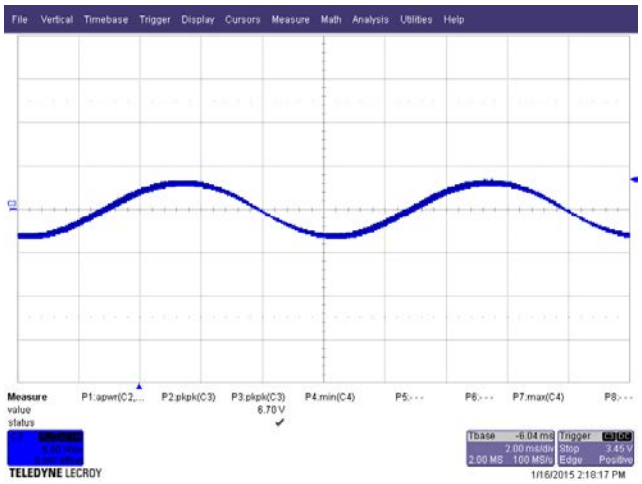

Figure 71 – Ripple, 230 VAC, 100% Load.
5 V / div., 2 ms / div.

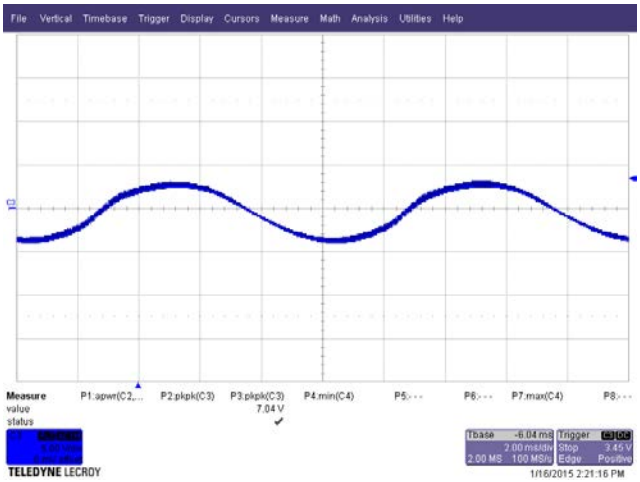

Figure 72 – Ripple, 264 VAC, 50% Load.
5 V / div., 2 ms / div.

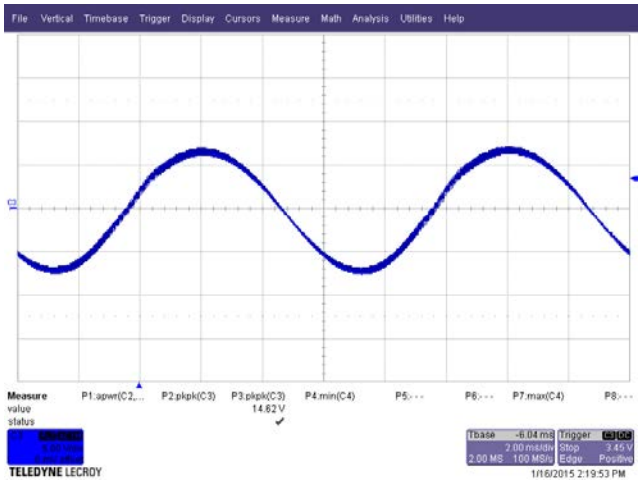

Figure 73 – Ripple, 264 VAC, 100% Load.
5 V / div., 2 ms / div.

12.10 Gain-Phase Measurement Procedure and Results

- The PFC stage is supplied from an adjustable DC source for this test. Connect the circuit as shown in figure below. Open the top end of the feedback divider network and insert a 100 Ω–2 W resistor in series as shown. The signal injected in the loop for gain–phase measurement will be injected across this resistor.
- Nodes A and B (two ends of the injection resistor) are connected to Channel 1 and Channel 2 of the frequency response analyzer using high voltage x100 attenuator probes. GND leads of both probes are connected to output return as shown.
- The signal to be injected is isolated using the Bode–Box injection transformer model – 200–000 from Venable Industries.

Test Procedure:

- Adjust the input voltage to 150 VDC and confirm that the PFC output voltage is within regulation limits.
- Inject a signal from the frequency response analyzer.
- The injected signal can be seen in the output voltage ripple of the PFC.
- Plot the gain phase by sweeping the injected signal frequency from 2 Hz to 1000 Hz.

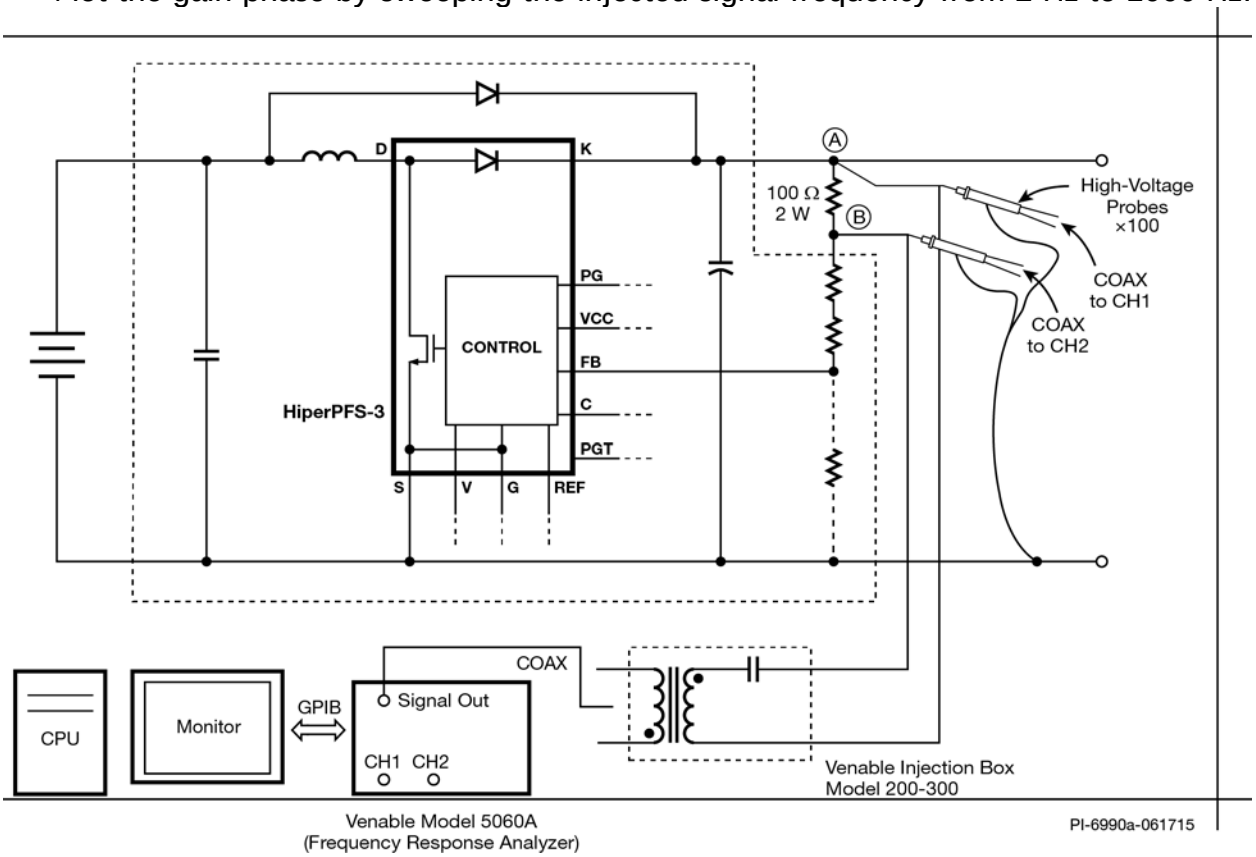

Figure 74 – System Test Set-up for Loop Gain-Phase Measurement.

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12.10.1 Measured Bode Plots

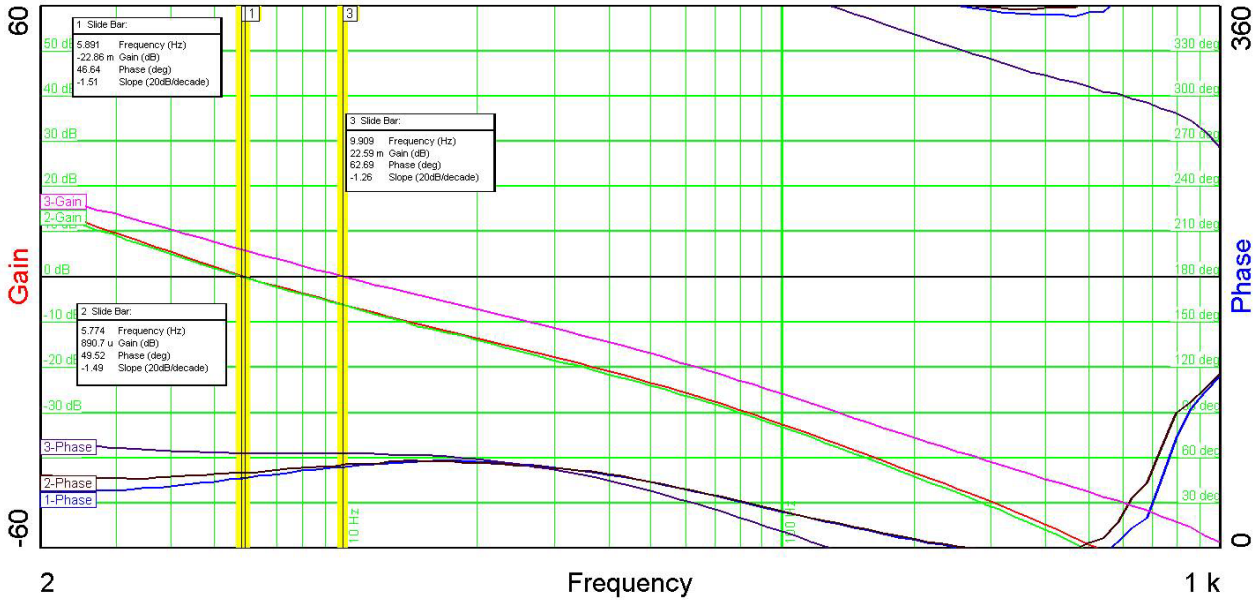

Figure 75 – Bode Plot with V_{IN} = 150 VDC at 100%, 50% and 20% Load.
20% Load (Red/Blu) – Slide Bar #1 Gain Crossover, 5.89 Hz, Phase Margin 46.6°.
50% Load (Grn/Brn) – Slide Bar #2, Gain Crossover 5.77 Hz, Phase Margin 49.5°.
100% Load (Pnk/Pur) – Slide Bar #3, Gain Crossover 9.91 Hz, Phase Margin 62.7°.

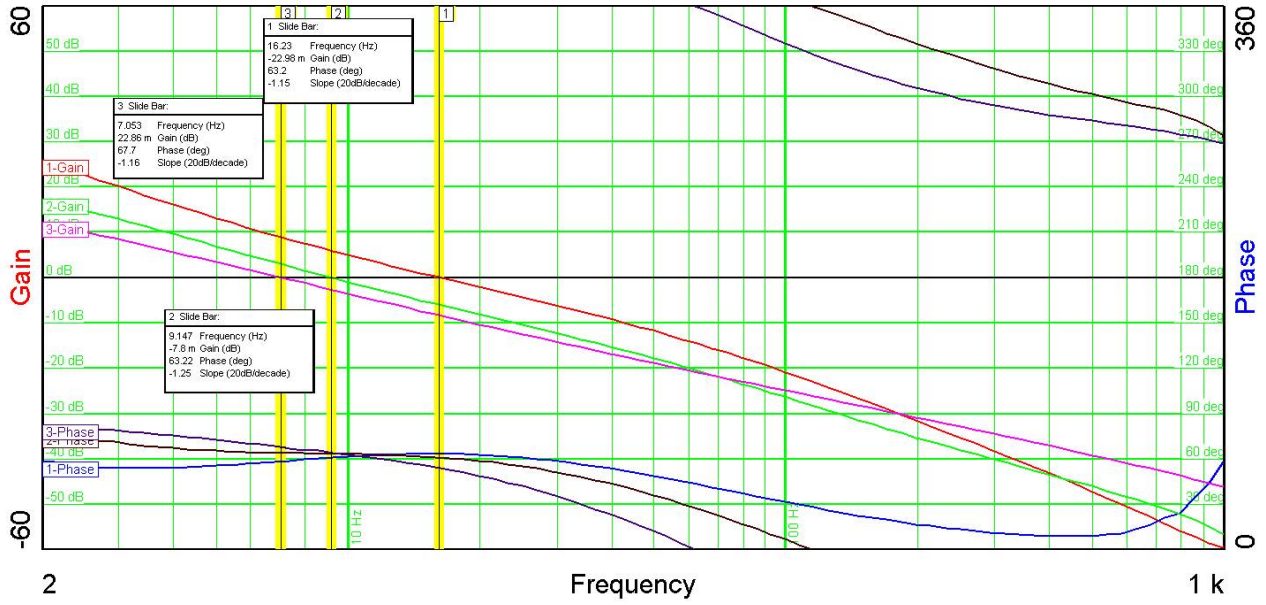

Figure 76 – Bode Plot with V_{IN} = 300 VDC at 100%, 50% and 20% Load.
20% Load (Red/Blu) – Slide Bar #1, Gain Crossover 16.2 Hz, Phase Margin 63.2°.
50% Load (Grn/Brn) – Slide Bar #2, Gain Crossover 9.15 Hz, Phase Margin 63.2°.
100% Load (Pnk/Pur) – Slide Bar #3, Gain Crossover 7.05 Hz, Phase Margin 67.7°.

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13 Line Surge Test

Differential input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 50 Hz. The UUT output was resistively loaded at full load and operation was verified following each surge event. The UUT was powered with a RDR-91 supply powered from the PFC output voltage. A single-sided 0.062” thick copper-clad FR4 material was placed under the UUT, insulation side up, and with the copper side of the board connected to earth ground at the AC input connector.

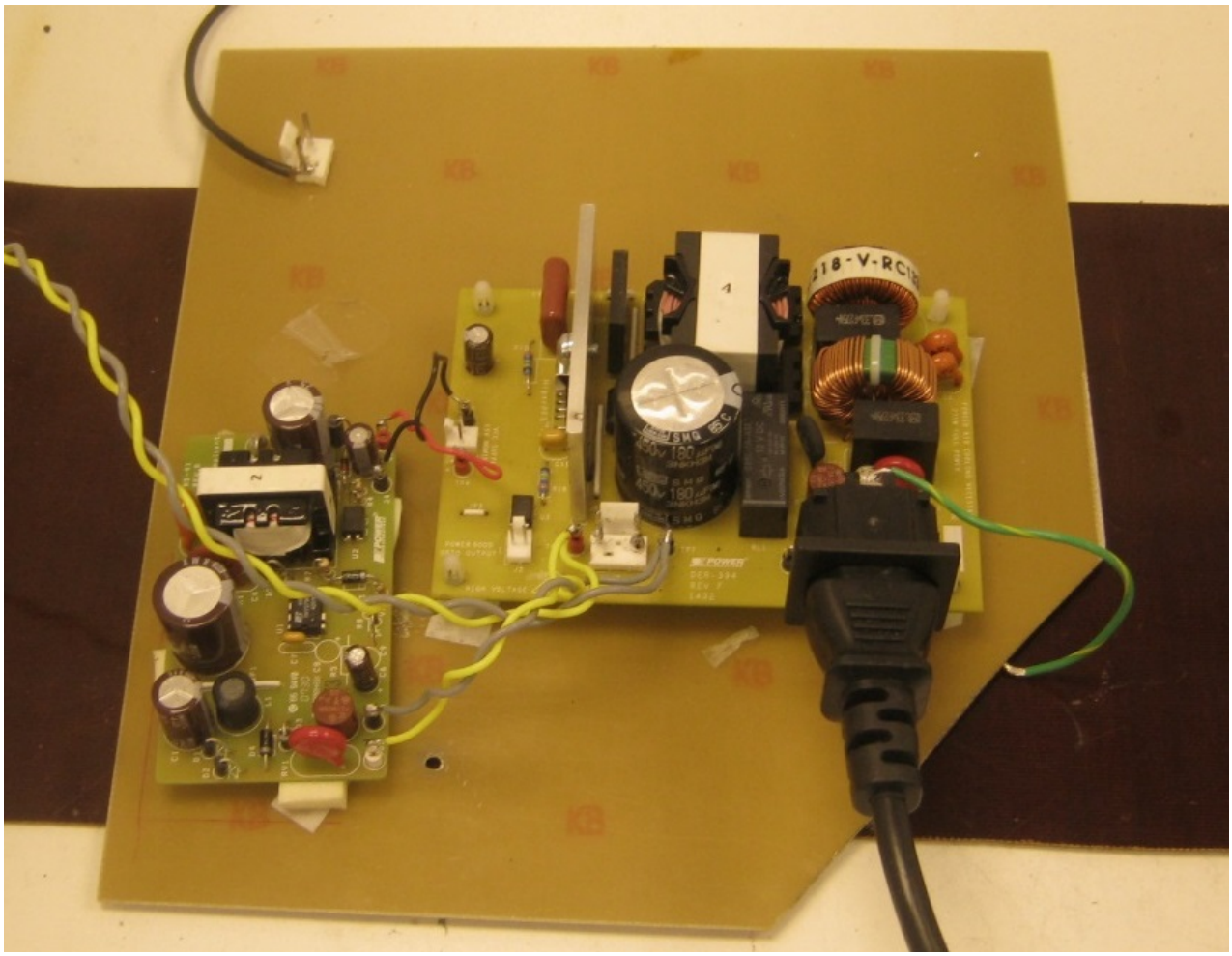

Figure 77 – Line Surge UUT Set-up.

13.1 Differential Mode Surge

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	2	10	PASS
230	-2	0	2	10	PASS
230	+2	90	2	10	PASS
230	-2	90	2	10	PASS
230	+2	180	2	10	PASS
230	-2	180	2	10	PASS
230	+2	270	2	10	PASS
230	-2	270	2	10	PASS

13.2 Common Mode Surge

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+3	0	12	10	PASS
230	-3	0	12	10	PASS
230	+3	90	12	10	PASS
230	-3	90	12	10	PASS
230	+3	180	12	10	PASS
230	-3	180	12	10	PASS
230	+3	270	12	10	PASS
230	-3	270	12	10	PASS

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14 EMI Scans

14.1 EMI Test Set-up

A single-sided 0.062” thick copper-clad FR4 material was placed under the UUT, insulation side up, and with the copper side of the board connected to earth ground at the AC input connector. The evaluation board is placed on top of the ground plane board. Output connector J4 is connected to a high-voltage resistive DC load (550 Ω) via a 3.3 mH common-mode choke to avoid the high frequency noise introduced by load wire connections. Auxiliary power to PFS board J3 is supplied by a RDR-91 supply powered from the PFC output voltage. All interconnections were made as short as possible. See below figure for set-up details.

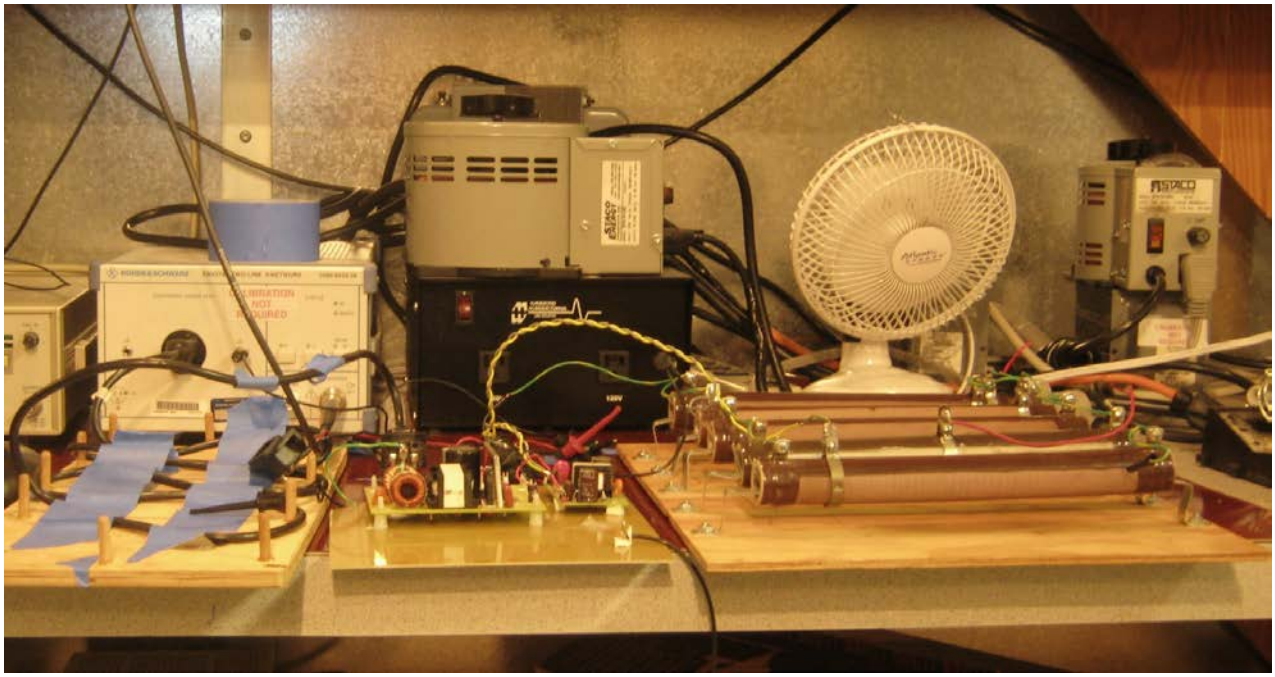

Figure 78 – EMI PFC Test Set-Up.

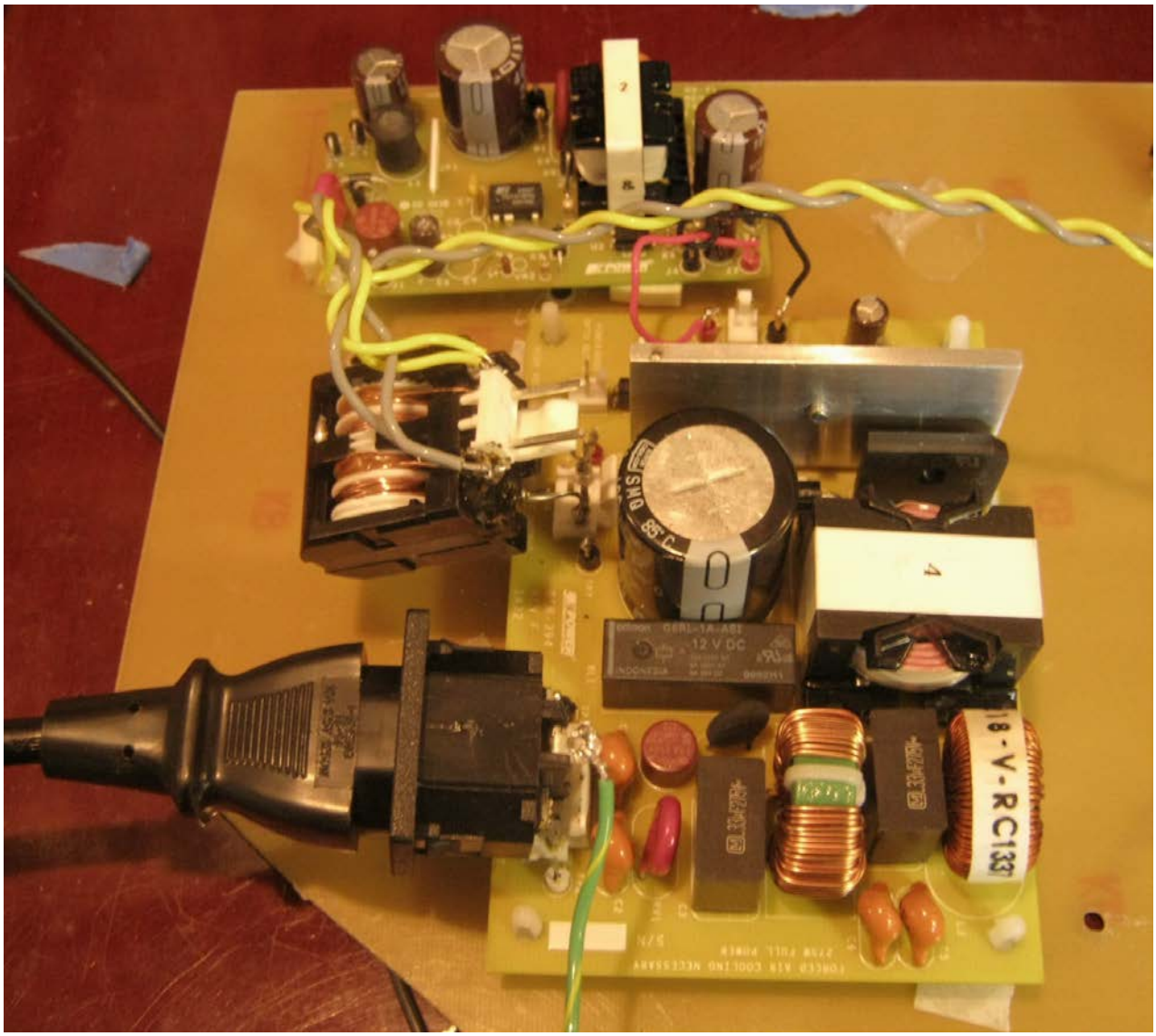

Figure 79 – Zoom in Picture of EMI PFC Test Set-Up.

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14.2 EMI Scans

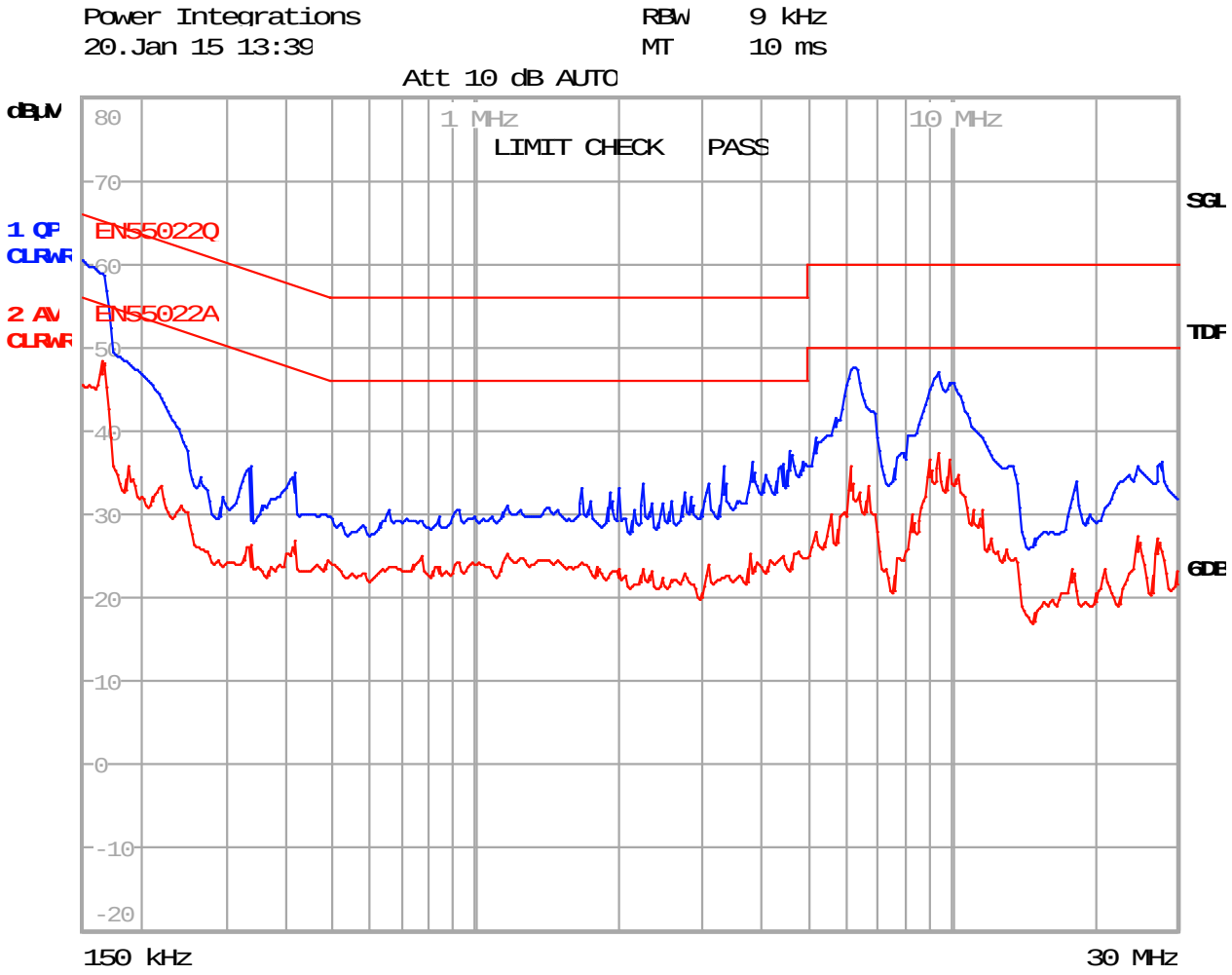

Figure 80 – 115 VAC, 100% Load.

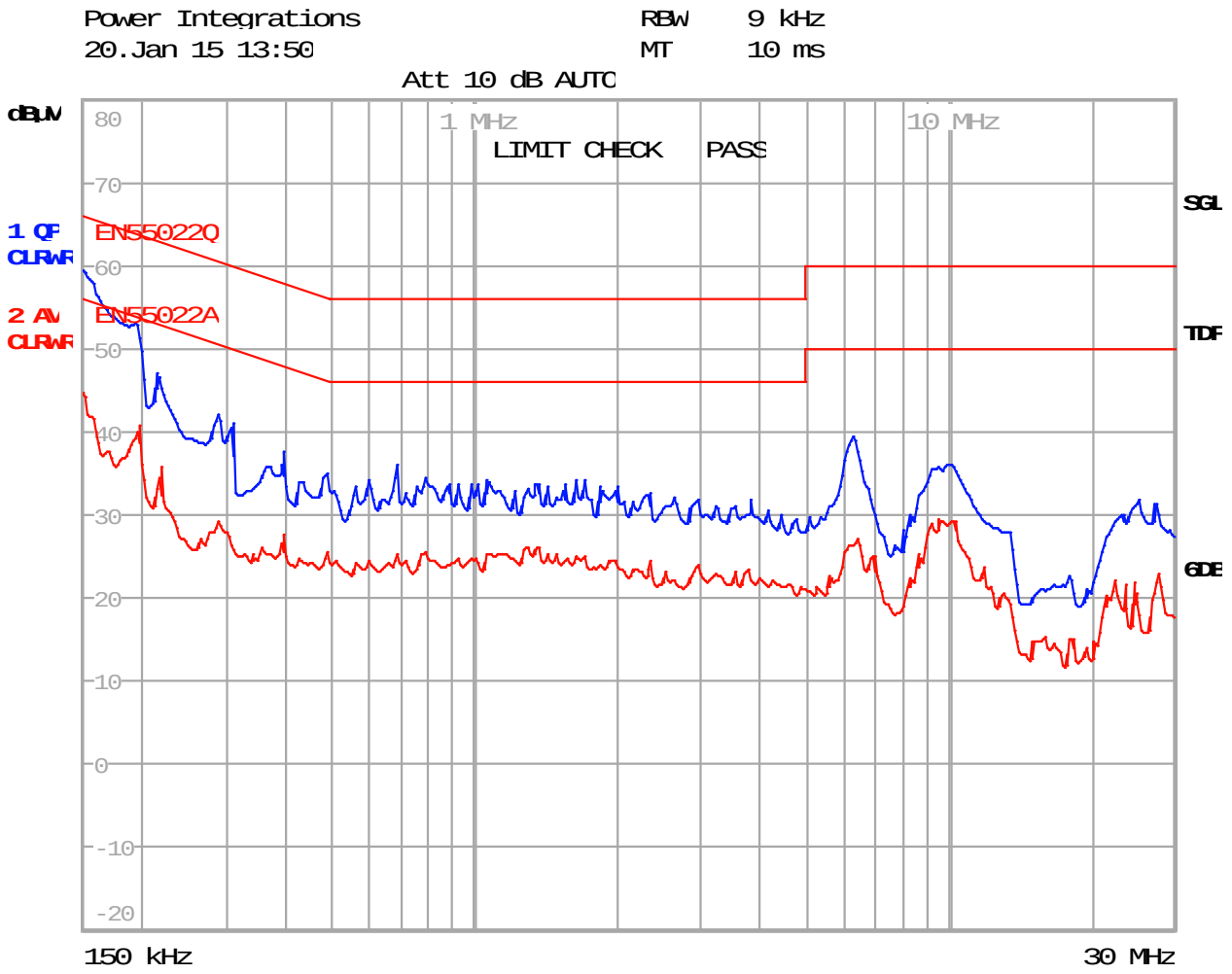

Figure 81 – 230 VAC, 100% Load.

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15 Appendix A

15.1 Test Set-up for Efficiency Measurement

The following setup is recommended for system efficiency, PF and THD measurements. Use of high resolution meters is recommended for output current and output voltage measurements. An 80 mm, 12 V DC fan (Adda A08112MS-A70GL) powered by 10 VDC is spaced 70 mm from the board edge for forced air cooling. See figures below for a typical equipment set-up, showing fan spacing and relative placement.

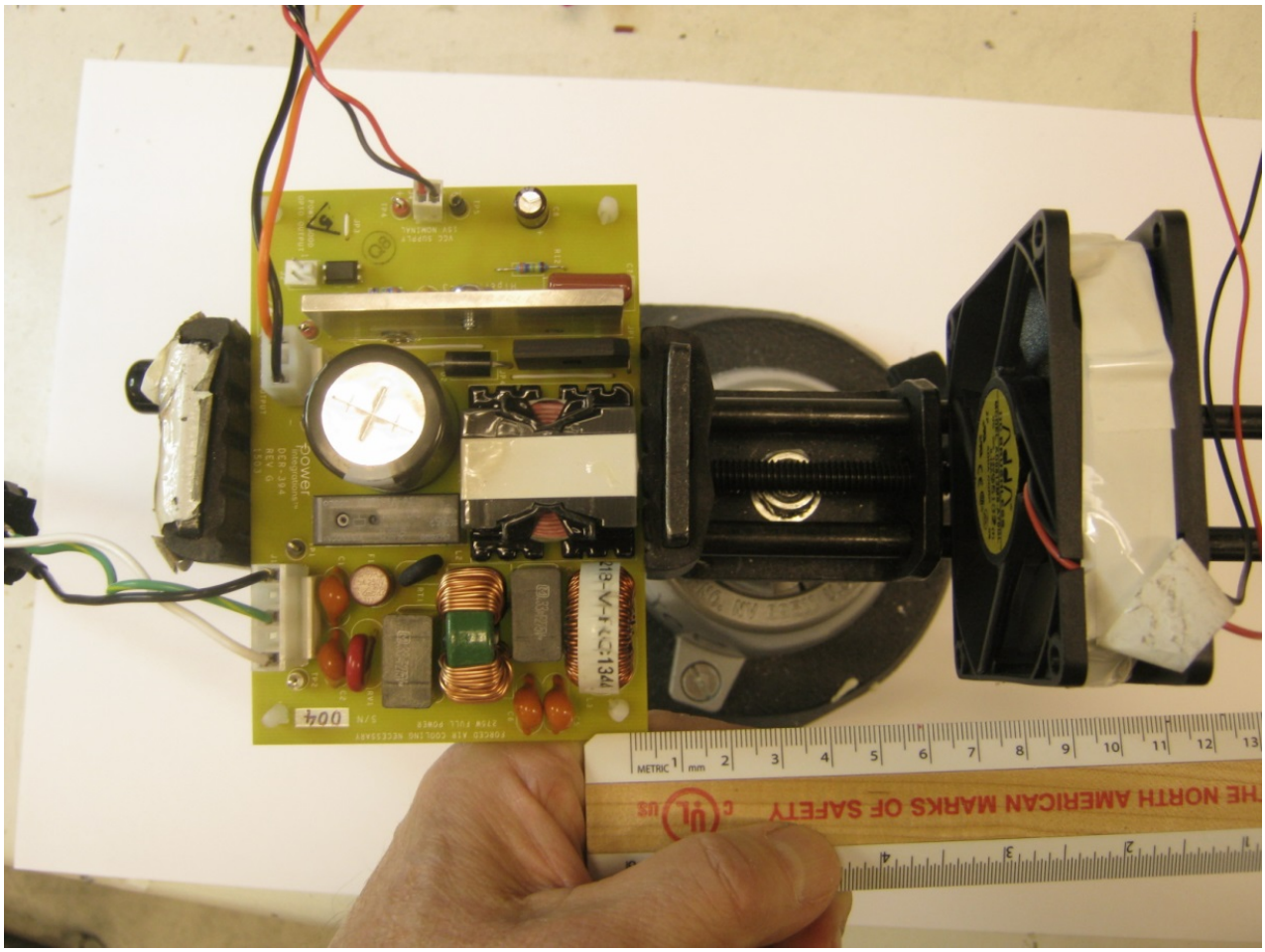

Figure 82 – Side View of the Test Set-Up for Efficiency, PF and THD Measurements.

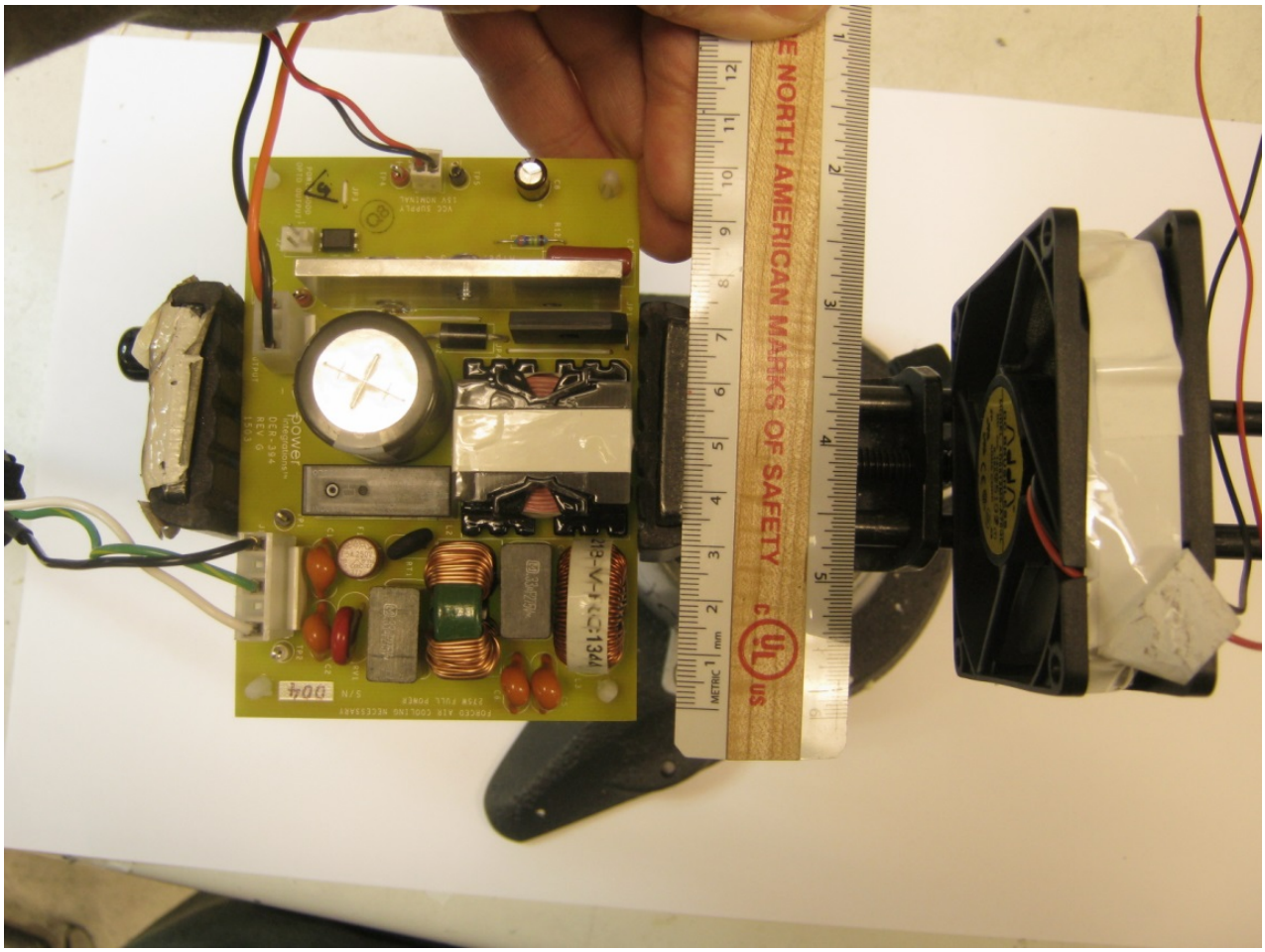

Figure 83 – Top View of the Test Set-Up for Efficiency, PF and THD Measurements.

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16 Revision History

Date	Author	Revision	Description & changes	Reviewed
24-Jun-15	RH	1.0	Initial Release	Apps & Mktg

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