Design Example Report

Title	***35 W Isolated Flyback Power Supply Using 1700 V InnoSwitch3-EP INN3647C-H606***
Specification	40 – 1000 VDC Input; 40 VDC: 4.8 W 100 VDC: 16 W 200 VDC: 25 W 300 VDC – 1000 VDC: 35 W
Application	High Input Voltage for Industrial application
Author	Applications Engineering Department
Document Number	DER-913
Date	September 14, 2022
Revision	1.2

Summary and Features

- High input voltage: up to 1000 VDC
- High ambient temperature operation: 85 ºC with continuous 30 W output at 1000 VDC input
- 1700 V InnoSwitch3-EP – industry's first 1700 V rated power IC with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >92% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
  - 5% output voltage tolerance across, load, line and temperature

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www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using a high voltage DC Supply to provide the DC input to the prototype board.

1 Introduction

This engineering report describes a 40 VDC to 1000 VDC input, 24 V output, 35 W power supply utilizing INN3647C from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

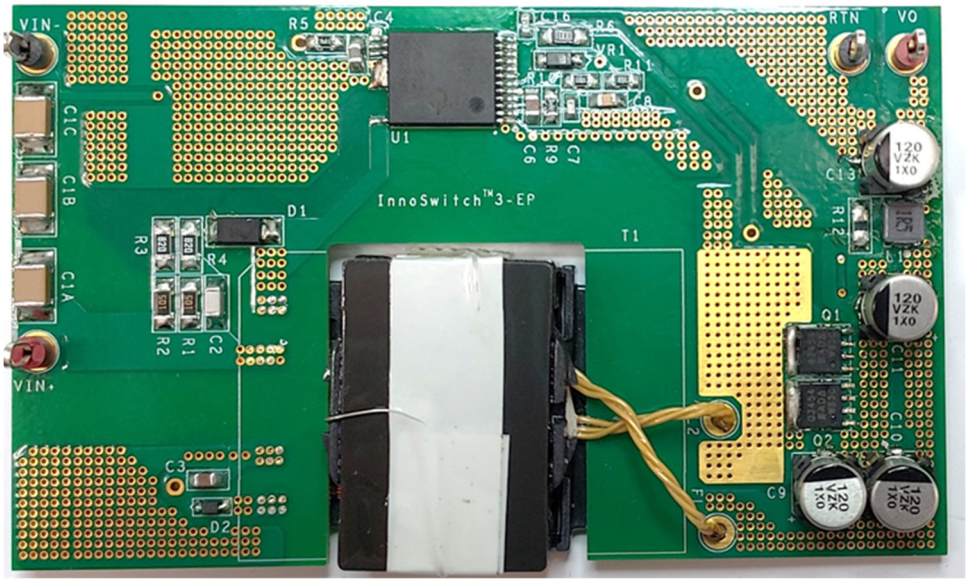


Figure 1 – Populated Circuit Board Photograph, Top.

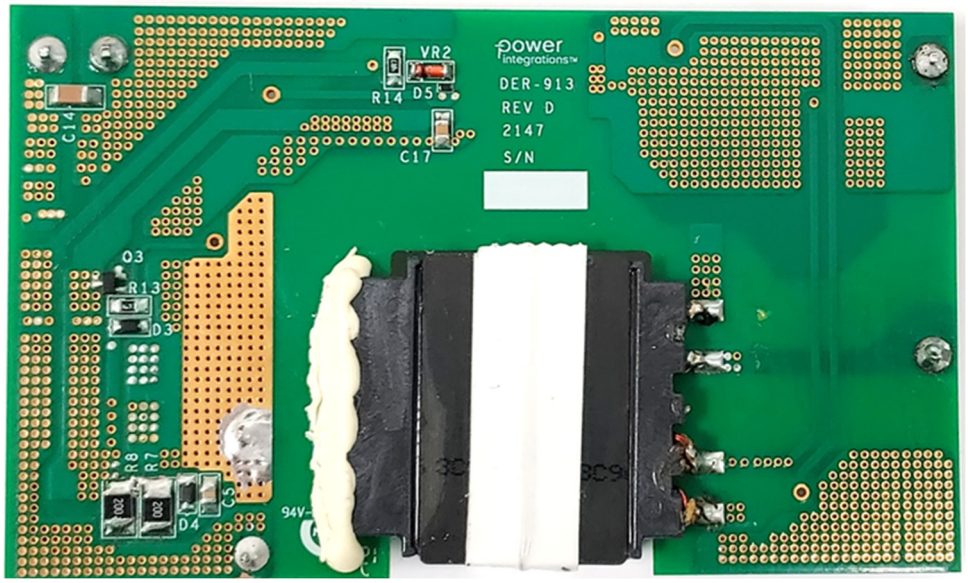


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	300	800	1000	VDC	For Electric Vehicle Emergency PSU. For 35 W Output Power.
No-load Input Power				30	mW	
Output						
Output Voltage	V_{OUT}		24		V	±5%
Output Current	I_{OUT}		1.458		A	
Output Ripple Voltage	V_{RIPPLE}			240	mV	On Board
Total Output Power						
Continuous Output Power	P_{OUT}			4.8	W	V_{IN} of 40 VDC
Continuous Output Power	P_{OUT}			16	W	V_{IN} of 100 VDC
Continuous Output Power	P_{OUT}			25	W	V_{IN} of 200 VDC
Continuous Output Power	P_{OUT}		35		W	V_{IN} 300 VDC to 1000 VDC
Ambient Temperature	T_{AMB}	-40		85	°C	Inside Inverter

3 Schematic

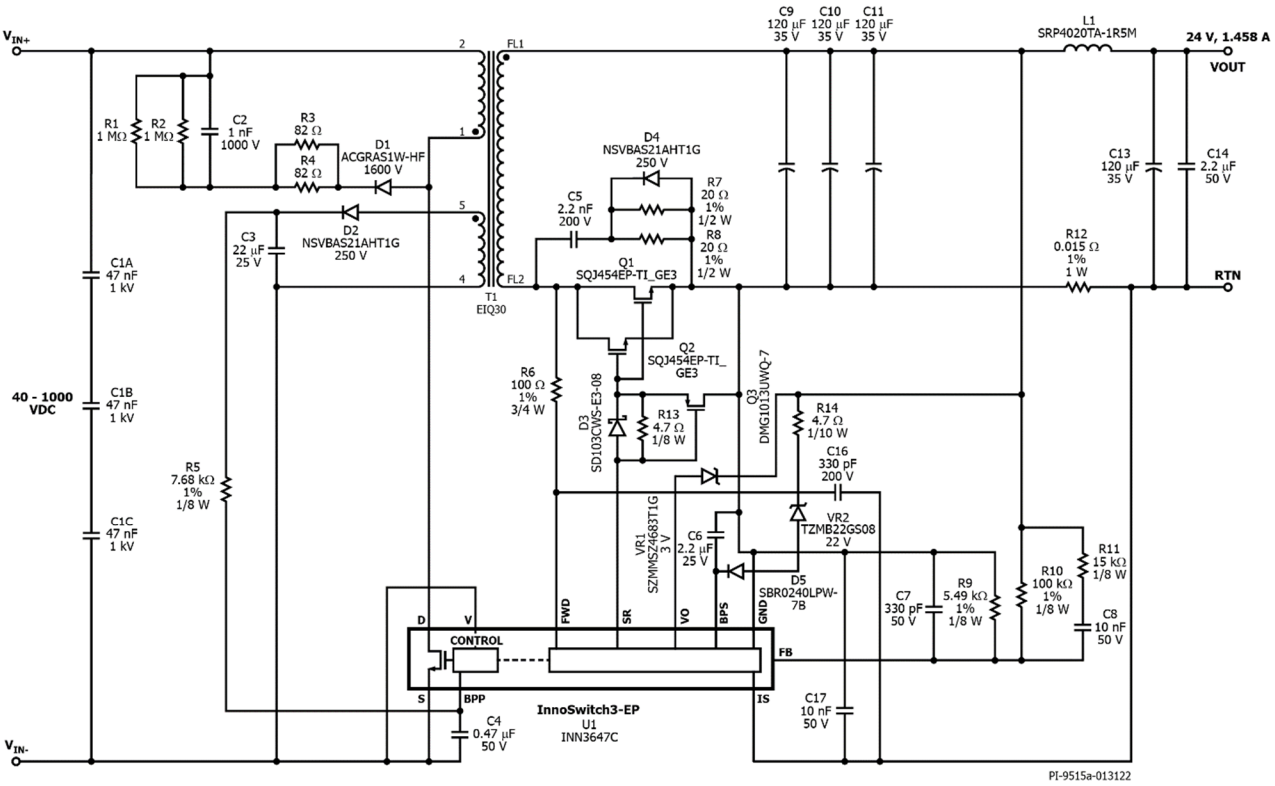


Figure 3 – Schematic.

4 Circuit Description

4.1 *INN3647C IC Primary*

One end of the transformer primary is connected to the DC bus, the other is connected to the integrated power MOSFET inside the INN3647C IC (U1). High-voltage ceramic capacitor C1A, C1B & C1C is used for the decoupling capacitor for the DC input voltage, and a low-cost RCD clamp formed by D1, R1, R2, R3, R4 and C2 limits the peak Drain voltage due transformer leakage inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C3, fed in the BPP pin via a current limiting resistor R5.

In this design the input primary under and overvoltage features were disabled by connecting the V pin to source.

4.2 **INN3647C IC Secondary**

The secondary-side of the INN3647C IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The 24 V output rectification is provided by SR FETs Q1 and Q2. Low ESR capacitors, C9, C10, C11, C13, C14 and output inductor L1 provide filtering. RC snubber network comprising D4, R7, R8, and C5 for Q1 and Q2 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R6 and the FWD pin of the IC. Capacitor C16 is used to suppress high frequency spikes on the FWD pin. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. A gate enhancement circuit comprising D3, R13 and Q3 prevents Vgs to turn-on during primary turn-ons. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into Zener diode VR1 which is connected to the VO pin. Zener VR1 is used to reduce the voltage stress on the VO pin. It will charge the BPS pin capacitor C6 via an internal regulator. The OVP sensing circuit, R14, VR2 and D5, connected to BPS pin provides secondary-side protection.

Resistors R9 and R10 form a voltage divider network that senses the output voltage. INN3647C IC has an internal reference of 1.265 V. Capacitor C7 provides decoupling from high frequency noise affecting power supply operation, and C8 and R11 is the feedforward network to speed up the response time to lower the output ripple. The output current is sensed by R12 and filtered by C17 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device will go into auto-restart.

5 PCB Layout

Layers: 4
Board Thickness: 0.062”
Board Material: FR4
Copper Weight: 2 oz
Surface finish: LF HASL

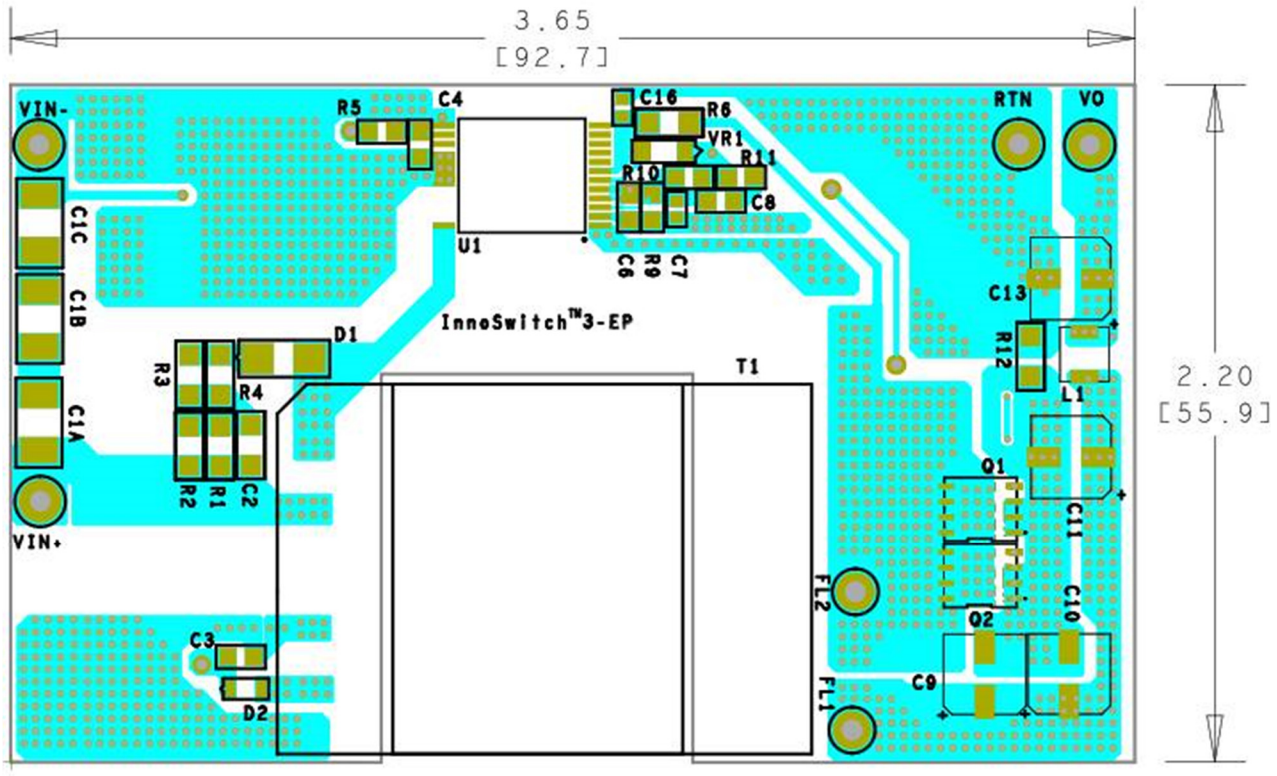


Figure 4 – Printed Circuit Board Layout (Top).

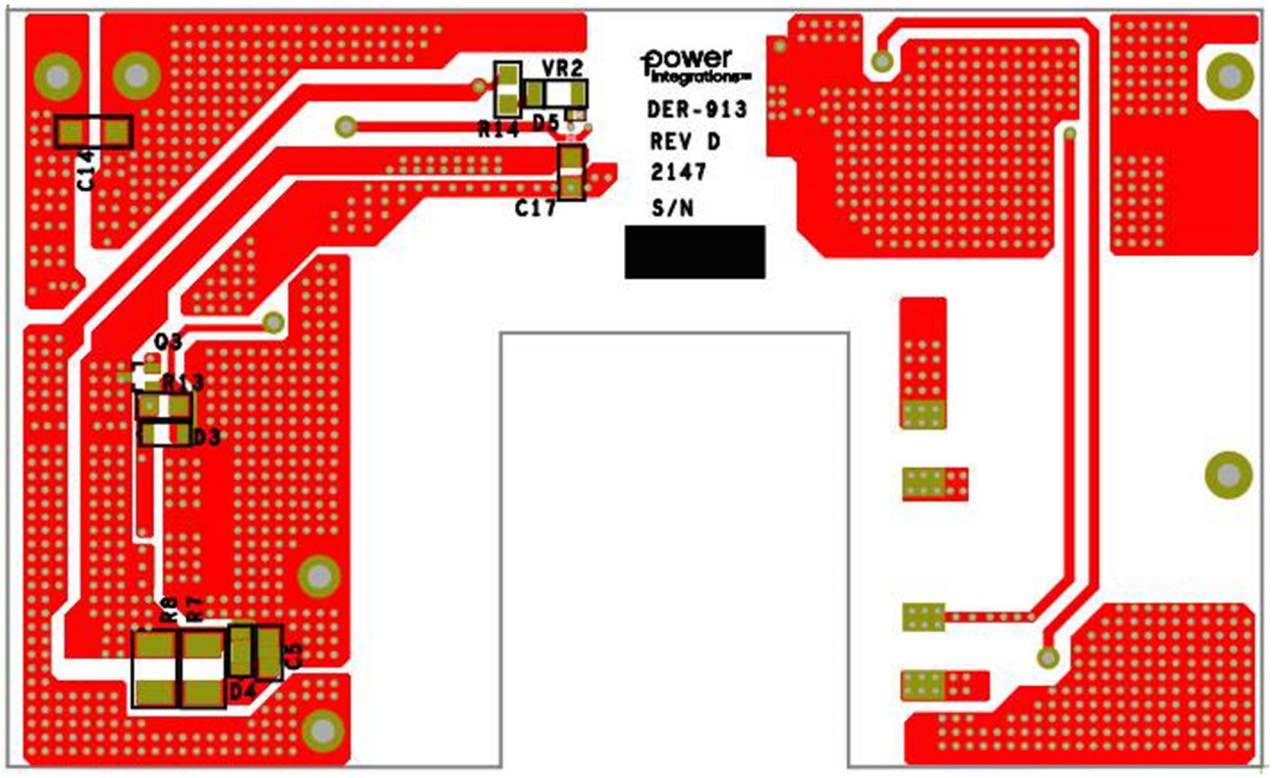


Figure 5 – Printed Circuit Board Layout (Bottom).

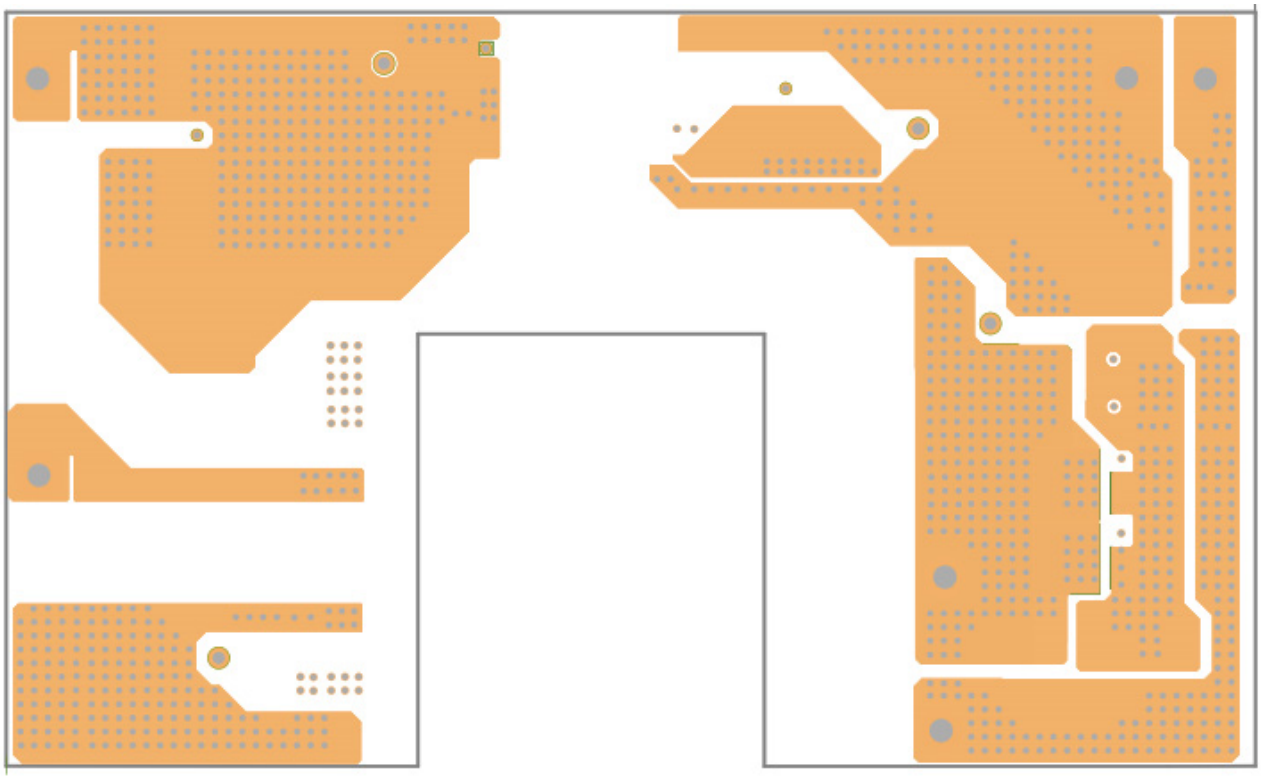


Figure 6 – Printed Circuit Board Layout (Internal Layer 1).

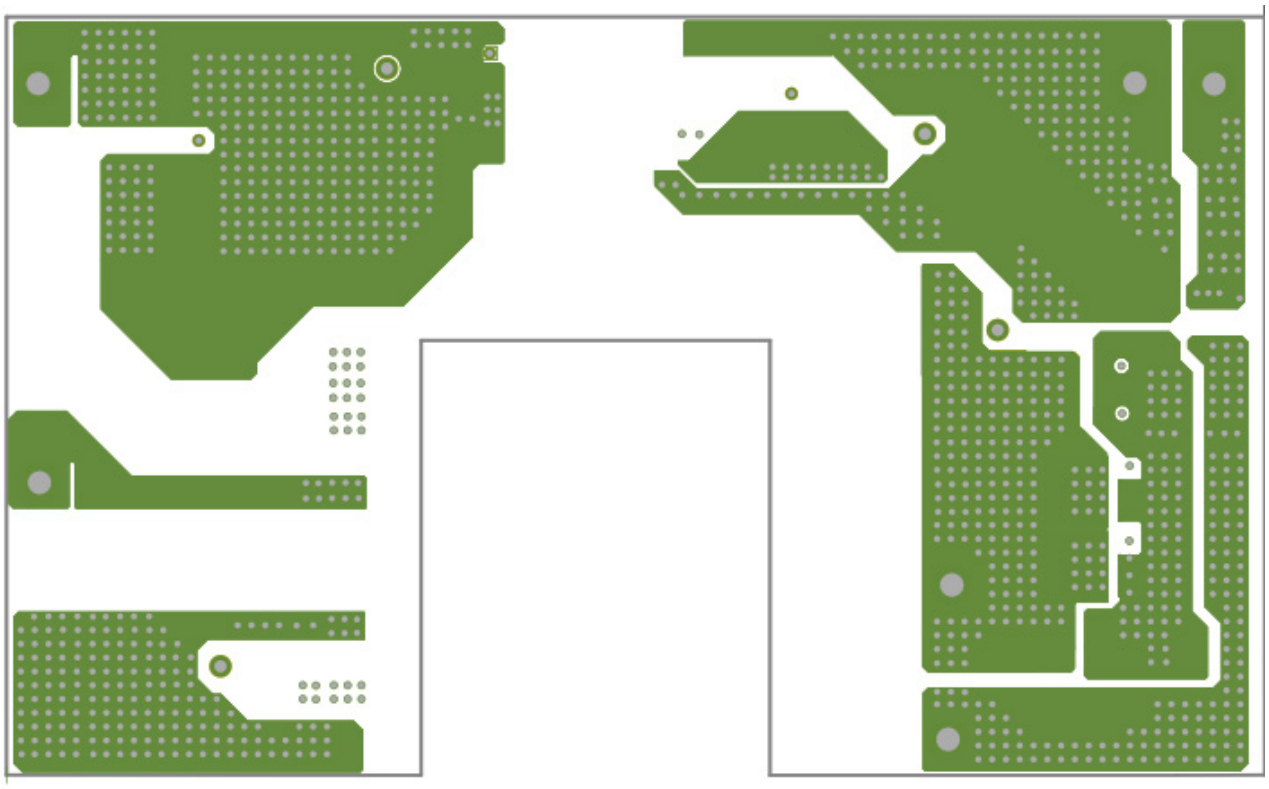


Figure 7 – Printed Circuit Board Layout (Internal Layer 2).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C2	1000 pF, ±10%, 1000 V (1 kV), Ceramic, C0G, NP0 1206	C1206C102KDGACAUTO	Kemet
2	1	C3	CAP, 22 µF ±20% 25 V Ceramic X5R 0805 (2012 Metric)	GRT21BR61E226ME13L	Murata
3	1	C4	0.47 µF, ±10% ,50 V, Ceramic, X7R, 0805 (2012 Metric), -55 °C ~ 125 °C	CGA4J3X7R1H474K125AB	TDK
4	1	C5	2200 pF, ±10%, 200 V, Ceramic, X7R, 0805 (2012 Metric)	08052C222K4T2A	AVX
5	1	C6	CAP, 2.2 µF ±10% 25 V Ceramic X7R 0805 (2012 Metric)	GCM21BR71E225KA73L	Murata
6	1	C7	330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
7	2	C8 C17	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
8	4	C9 C10 C11 C13	120 µF, ±20%, 35 V, Aluminum - Polymer, Radial, Can - SMD, 35 mΩ, 4000 Hrs @ 125°C	EEH-ZKV121XUV	Panasonic
9	1	C14	2.2 µF, ±10%, 50 V, Ceramic, X7R, Bypass, Decoupling, 1206 (3216 Metric)	C1206C225K5RACAUTO7210	KEMET Murata
10	1	C16	330 pF, ±5%, 200 V, Ceramic, C0G, NP0, 0603 (1608 Metric)	CGJ3E3C0G2D331J080AA	TDK
Alt.	1	C16	330 pF, ±5%, 200 V, Ceramic, C0G, NP0, 0805 (2012 Metric)	C0805C331J2GACAUTO	TDK
11	3	C1A C1B C1C	0.047 µF, ±10%, 1000 V (1 kV), Ceramic, X7R, 1812 (4532 Metric)	1812Y1K00473KST	Knowles Syfer
12	1	D1	Diode Standard 1600 V 1 A SMT DO-214AC (SMA)	ACGRAS1W-HF	Comchip
13	2	D2 D4	Diode, Standard, 250 V, 200 mA, SC-76, SOD-323	NSVBAS21AHT1G	ON Semi
Alt.	2	D2 D4	Diode, Standard, 200 V, 200 mA (DC), SOD-323, SC-76	SBAS20HT1G	ON Semi
14	1	D3	Diode, Schottky, 20 V, 350 mA (DC), SMT, SOD-323 SC-76	SD103CWS-E3-08	Vishay
Alt.	1	D3	Diode, Schottky, 40 V, 350 mA (DC), SMT, SOD-323 SC-76	SD103AWS-HE3-08 SD103CW-HE3-08	Vishay
15	1	D5	Diode Standard 40 V 200 mA SMT X1-DFN1006-2	SBR0240LPW-7B	Diodes, Inc.
16	2	FL1 FL2	Flying Lead, Hole size 70 mils	N/A	N/A
17	1	L1	1.5 µH, ±20%, Shielded, Wire Wound, Inductor, 4.5 A, 42 mΩ Max, Automotive, AEC-Q200, 2-SMD	SRP4020TA-1R5M	Bourns
18	2	Q1 Q2	MOSFET, N-Channel, 200 V, 13 A (Tc), 68 W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8	SQJ454EP-T1_GE3	Vishay
19	1	Q3	MOSFET, P-Channel 20 V, 820 mA (Ta), 310 mW (Ta), SMT, SOT323, SC-70, SOT-323	DMG1013UWQ-7	Diodes, Inc.
20	2	R1 R2	RES, 1 MΩ, ±5%, 0.25 W, ¼ W, 1206 (3216 Metric), High Voltage Thick Film	KTR18EZPJ105	Rohm
21	2	R3 R4	RES, 82 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ820V	Panasonic
22	1	R5	RES, 7.68 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7681V	Panasonic
23	1	R6	RES, 100 Ω, ±1%, 0.75 W, ¾ W, Chip, 1206 (3216 Metric), Pulse Withstanding, Thick Film	SR1206FR-7T100RL	YAGEO
24	2	R7 R8	RES, 20 Ω ±1% 0.5 W, Thick Film Chip 1210 (3225 Metric)	CRCW121020R0FKEA CRCW121020R0FKEAHP	Vishay
25	1	R9	RES, 5.49 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5491V	Panasonic
26	1	R10	RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
27	1	R11	RES, 15 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
28	1	R12	0.015 Ω, ±1%, ±75 ppm/°C, 1 W, 1206 (3216 Metric), Current Sense, -55 °C ~ 155 °C	ERJ-8CWFR015V	Panasonic
29	2	R13 R14	RES, 4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
30	2	RTN VIN-	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
31	1	T1	Bobbin, EIQ30, 10 pins, SMD Transformer	YIH HWA POL-INN056	YW-797 Premier Magnetics
32	1	U1	InnoSwitch3-EP, 1700 V, InSOP-24D	INN3647C-H606	Power Integrations
33	1	VR1	DIODE ZENER 3 V 500 mW SOD123	SZMMSZ4683T1G	ON Semi
34	1	VR2	DIODE ZENER 22 V 500 mW SOD80	TZMB22-GS08	Vishay
35	2	VIN+ VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

7 Transformer Design

7.1 *Electrical Diagram*

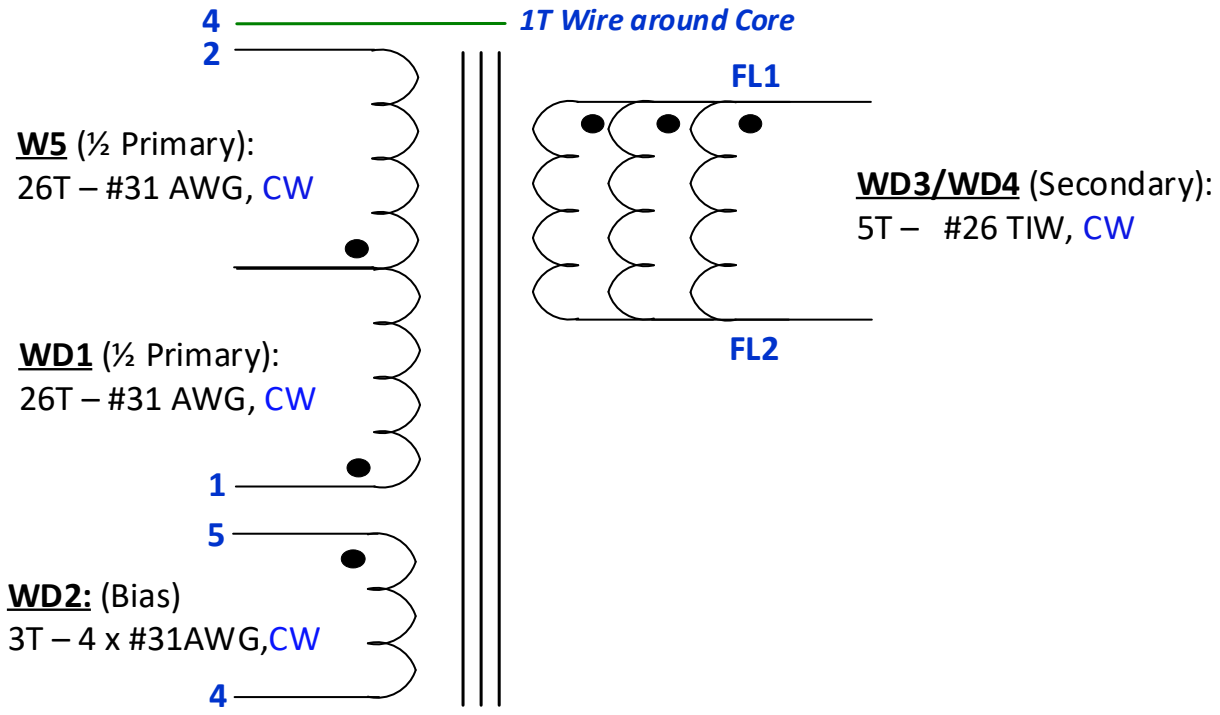


Figure 8 – Electrical Diagram.

7.2 *Electrical Specification*

Parameter	Condition	Spec.
Electrical Strength	60 seconds, 10 mA, from pins 1-4 to FL1 and FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	1100 µH ±5%
Resonant Frequency	Between pin 1 and 2, other windings open.	1,600 kHz (Min.)
Primary Leakage Inductance	Between pin 1 and 2, with pins: FL1-FL2 shorted.	20 µH (Max.)

7.3 *Materials List*

Item	Description
[1]	Core: EIQ30, 3F35 Ferroxcube, PLT30/20/3 AL = 4600 nH/T^2 (UNGAPPED) or equivalent
[2]	Bobbin: EIQ30 – 10pins SMD, P/N: 25-00887-00.
[3]	Magnet Wire: #31 AWG, Double Coated.
[4]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[5]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 3.5 mm Width.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 13.5 mm Width.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

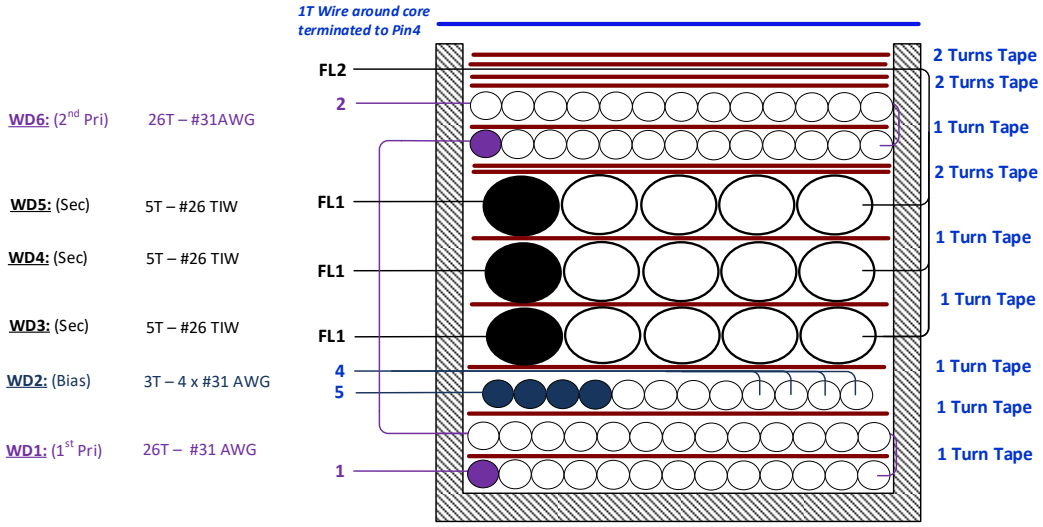
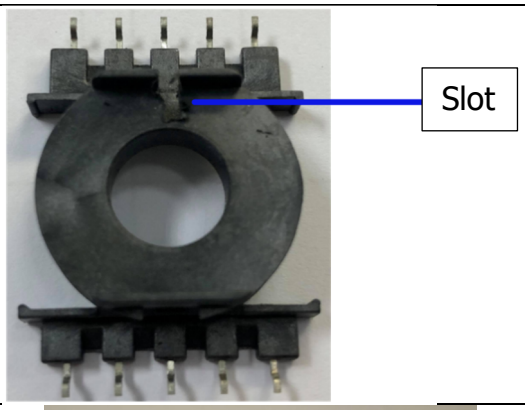
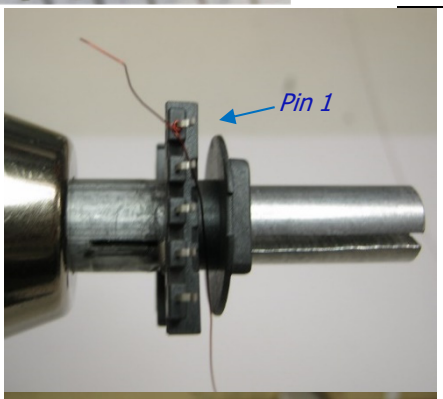
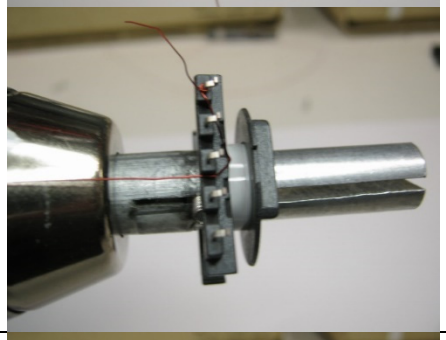
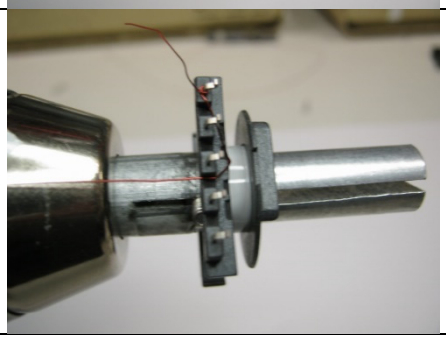


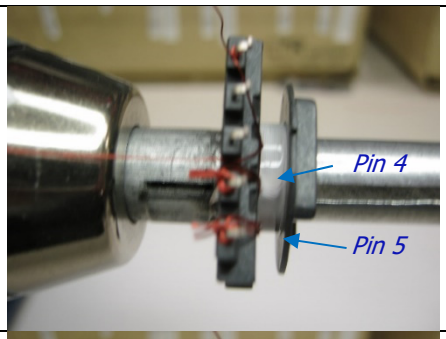
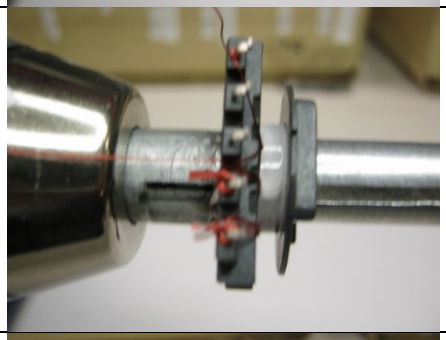
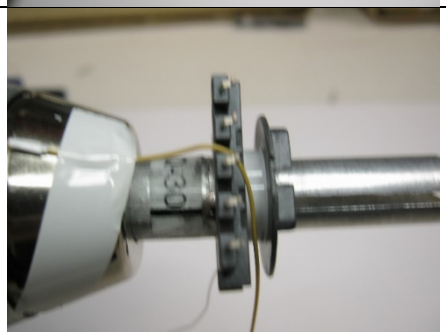
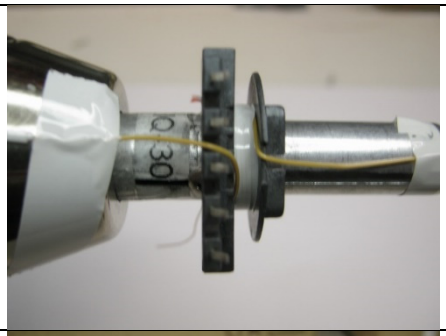
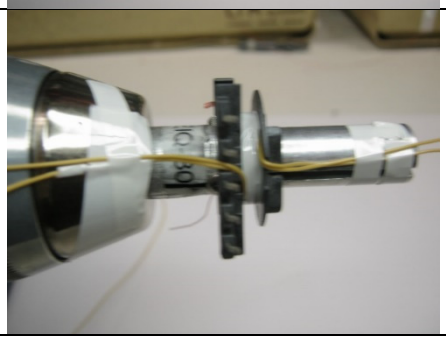
Figure 9 – Transformer Build Diagram.

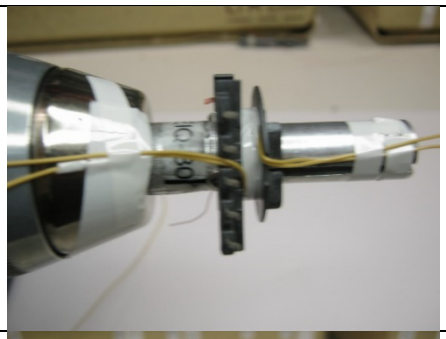
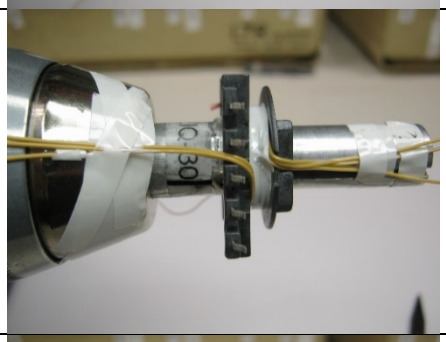
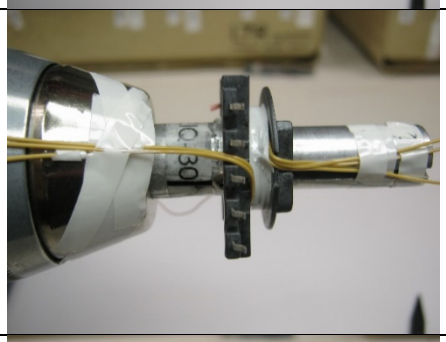
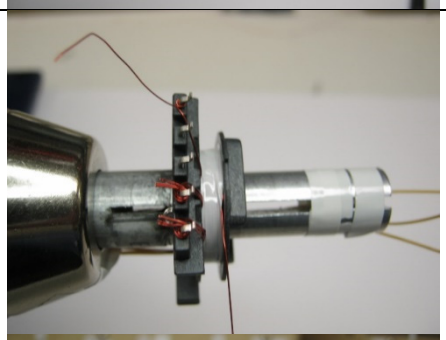
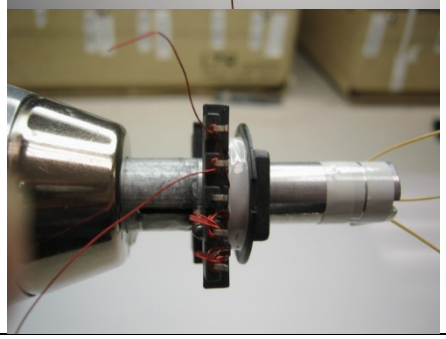
7.5 *Transformer Instruction*

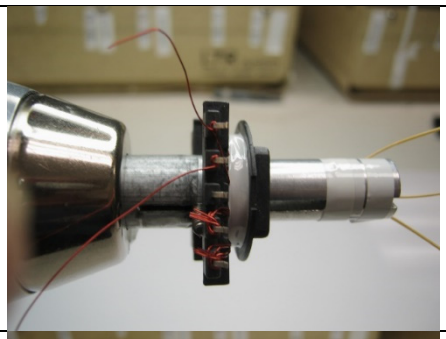
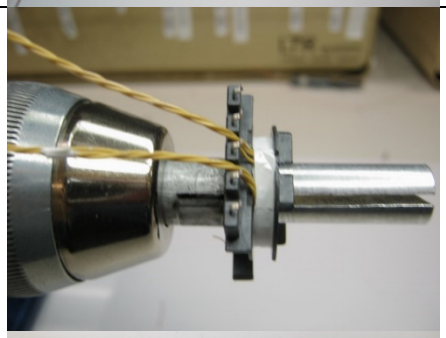
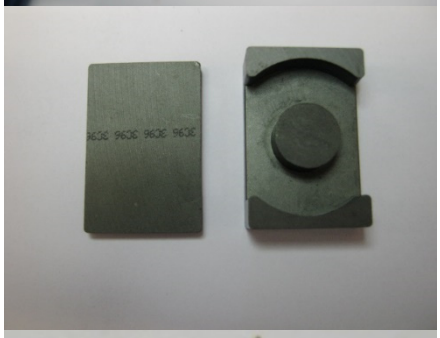
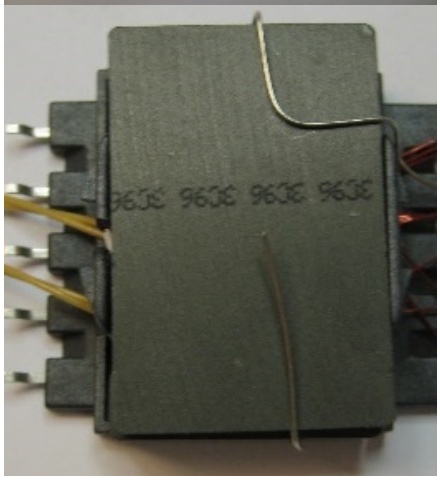
Winding Preparation	Make 2 slots with 3 mm width on bottom secondary flange of bobbin Item [2], (see illustration below). Winding direction is clockwise direction for forward direction.
WD1 1st Primary	Start at pin 1, wind 13 turns of wire Item [3] in 1 layer, with tight tension, from left to right and right to left. Put 1 layer of tape Item [6]. Continue from right to left, wind 13 turns of wire Item [3] in 1 layer. At the last turn, leave the wire floating and enough length for WD6 2nd Primary.
Insulation	1 layer of tape Item [6].
WD2: Bias	Use 4 wires of Item [3] start at pin 5, wind 3 turns from left to right, bring all wires to the left and terminate at pin 4.
Insulation	1 layer of tape Item [6].
WD3 Secondary	Start at left slot of secondary side, use wires Item [4], leaving ~ 40.0 mm floating, and mark as FL1. Wind 5 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0 mm floating, and mark FL2.
Insulation	1 layer of tape Item [6].
WD4 Secondary	Repeat the same winding above on top previous winding, also mark and finish ends as FL1 and FL2.
Insulation	1 layer of tape Item [6].
WD5 Secondary	Repeat the same winding above on top previous winding, also mark and finish ends as FL1 and FL2.
Insulation	2 layer of tape Item [6].
WD6 2nd Primary	Using floating wire from WD1-1st Primary, wind 13 turns of wire Item [3] in 1 layer, with tight tension, from left to right. Put 1 layer of tape Item [6]. Continue from right to left, wind 13 turns of wire Item [3] in 1 layer and finish at pin 2.
Insulation	2 layer of tape Item [6]. Bring 3 wires marked as FL2 to the left and secure with 2 layers of tape Item [6].
Finish Assembly	Gap core halves to get 1100 µH. Solder pin 4 with bus-wire Item [5] then lean along core halves and secure with tape. Wrap up to the body of transformer with tape Item [7]. Remove pins 3, 6, 7, 8, 9 & 10. Varnish with Item [8].

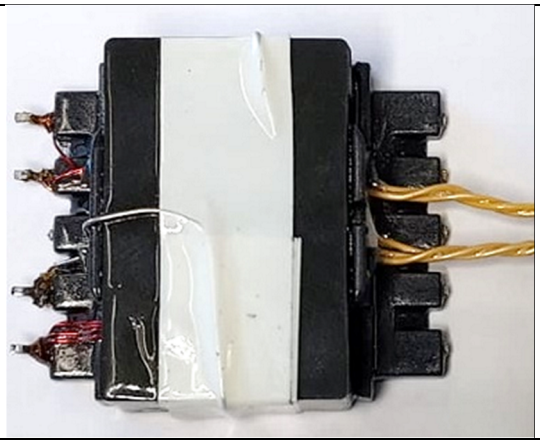
7.6 *Winding Illustrations*

Winding Preparation		Make slot with 3.0 mm width on bottom secondary flange of the bobbin Item [2]. Winding direction is clockwise direction for forward direction.
WD1: **1st Primary**	 	Start at pin 1, wind 13 turns of wire Item [3] in 1 layer, with tight tension, from left to right. Put 1 layer of tape Item [6]. Continue from right to left, wind 13 turns of wire Item [3] in 1 layer. At the last turn, leave the wire floating and enough length for WD6 2nd Primary.
Insulation		1 layer of tape Item [6].

WD2: Bias		Use 4 wires Item [3] start at pin 5, wind 3 turns from left to right, bring all wires to the left and terminate at pin 4.
Insulation		1 layer of tape item [6] for Insulation.
WD3: Secondary		Start at left slot of secondary side, use wires item [4], leaving ~ 40.0 mm floating, and mark as FL1. Wind 5 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0 mm floating, and mark FL2.
Insulation		1 layer of tape item [6] for Insulation.
WD4: Secondary		Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.

Insulation		1 layer of tape item [6] for Insulation.
WD5: Secondary		Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation		2 layers of tape item [6] for Insulation.
WD6 2nd Primary	 	Using floating wire from WD1-1st Primary, wind 13 turns of wire Item [3] in 1 layer, with tight tension, from left to right. Put 1 layer of tape Item [6]. Continue from right to left, wind 13 turns of wire Item [3] in 1 layer and finish at pin 2.

Insulation		2 layers of tape Item [6].
Finish		Bring 3 wires marked as FL2 to the left and secure with 2 layers of tape Item [6].
		Gap core halves to get 1100 μH.
		Solder pin 4 with bus-wire Item [5] then lean along core halves and secure with tape.

		Wrap up to the body of transformer with tape Item [7]. Remove pins 3, 6, 7, 8, 9 & 10. Varnish with Item [8].

7.7 *Design Spreadsheet*

1	ACDC_InnoSwitch3-EP1700V_Flyback_012822; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-EP 1700V Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	300		300	V	Minimum DC input voltage
5	VIN_MAX	1000		1000	V	Maximum DC input voltage
6	VIN_RANGE			INDUSTRIAL DC		Range of DC input voltage
7	LINEFREQ				Hz	AC Input voltage frequency
8	CAP_INPUT				uF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	PERCENT_CDC			0		Cable drop compensation desired at full load
11	IOUT	1.458		1.458	A	Output current
12	POUT			34.99	W	Output power
13	EFFICIENCY	0.85		0.85		Efficiency estimate at full load and minimum input DC voltage
14	FACTOR_Z			0.50		Z-factor estimate
15	ENCLOSURE			OPEN FRAME		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_CODE	AUTO		INN3647C		Device code
22	POUT_MAX			50	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			2.52	Ω	Primary switch on time drain resistance at 100 degC
24	ILIMIT_MIN			1.488	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			1.600	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.712	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			1700	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			0.32	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW			1320.0	V	Peak drain voltage on the primary switch during turn-off
33	**WORST CASE ELECTRICAL PARAMETERS**					
34	FSWITCHING_MAX	43000		43000	Hz	Maximum switching frequency at full load and minimum DC input voltage
35	VOR	250.0		250.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN			300.00	V	Minimum input DC voltage
37	KP			3.36		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation
39	DUTYCYCLE			0.199		Primary switch duty cycle
40	TIME_ON			5.39	us	Primary switch on-time
41	TIME_OFF			18.71	us	Primary switch off-time
42	LPRIMARY_MIN			1048.4	uH	Minimum primary inductance
43	LPRIMARY_TYP			1103.5	uH	Typical primary inductance
44	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			1158.7	uH	Maximum primary inductance
47	**PRIMARY CURRENT**					
48	IPEAK_PRIMARY			1.421	A	Primary switch peak current

49	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
50	IAVG_PRIMARY			0.127	A	Primary switch average current
51	IRIPPLE_PRIMARY			1.421	A	Primary switch ripple current
52	IRMS_PRIMARY			0.347	A	Primary switch RMS current
54	**SECONDARY CURRENT**					
55	IPEAK_SECONDARY			14.779	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
57	IRMS_SECONDARY			3.951	A	Secondary winding RMS current
61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	**CORE SELECTION**					
63	CORE	CUSTOM		CUSTOM		Core selection
64	CORE CODE	EIQ30		EIQ30		Core code
65	AE	108.00		108.00	mm^2	Core cross sectional area
66	LE	43.00		43.00	mm	Core magnetic path length
67	AL	4900		4900	nH/turns^2	Ungapped core effective inductance
68	VE	3910.0		3910.0	mm^3	Core volume
69	BOBBIN	EIQ30-10pins-Bobbin		EIQ30-10pins-Bobbin		Bobbin
70	AW	16.80		16.80	mm^2	Window area of the bobbin
71	BW	3.50		3.50	mm	Bobbin width
72	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
74	**PRIMARY WINDING**					
75	NPRIMARY			52		Primary turns
76	BPEAK			3615	Gauss	Peak flux density
77	BMAX			2874	Gauss	Maximum flux density
78	BAC			1437	Gauss	AC flux density (0.5 x Peak to Peak)
79	ALG			408	nH/turns^2	Typical gapped core effective inductance
80	LG			0.305	mm	Core gap length
81	LAYERS_PRIMARY	4		4		Number of primary layers
83	**SECONDARY WINDING**					
84	NSECONDARY	5		5		Secondary turns
86	**BIAS WINDING**					
87	NBIAS			3		Bias turns
91	**PRIMARY COMPONENTS SELECTION**					
92	**LINE UNDERVOLTAGE**					
93	BROWN-IN REQURED			270.0	V	Required DC bus brown-in voltage threshold
94	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
95	VZ			9.1	V	Zener diode reverse voltage
96	VR			6.8	V	Zener diode reverse voltage at the maximum reverse leakage current
97	ILKG			2.0	uA	Zener diode maximum reverse leakage current
98	RLS_H			8.90	MΩ	Connect five 1.8 MOhm input voltage upper sense resistors to the V-pin for the required UV threshold
99	RLS_L			249.00	kΩ	Input voltage lower sense resistor to the V-pin for the required UV threshold
100	BROWN-IN ACTUAL			221.9 - 266.0	V	Actual DC brown-in voltage range using standard resistors
101	BROWN-OUT ACTUAL			191.1 - 236.5	V	Actual DC brown-out voltage range using standard resistors

104	**BIAS DIODE**					
105	VBIAS	9.0	Info	9.0	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 10V
106	VF_BIAS			0.70	V	Bias winding diode forward drop
107	VREVERSE_BIASDIODE			66.69	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
108	CBIAS			22	uF	Bias winding rectification capacitor
109	CBPP			0.47	uF	BPP pin capacitor
113	**SECONDARY COMPONENTS**					
114	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
115	RFB_LOWER			5.62	kΩ	Lower feedback resistor
116	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
120	**MULTIPLE OUTPUT PARAMETERS**					
121	**OUTPUT 1**					
122	VOUT1			24.00	V	Output 1 voltage
123	IOUT1			1.46	A	Output 1 current
124	POUT1			34.99	W	Output 1 power
125	IRMS_SECONDARY1			3.951	A	Root mean squared value of the secondary current for output 1
126	IRIPPLE_CAP_OUTPUT1			3.672	A	Current ripple on the secondary waveform for output 1
127	NSECONDARY1			5		Number of turns for output 1
128	VREVERSE_RECTIFIER1			120.15	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
129	SRFET1	AUTO	Info	AON7254		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
130	VF_SRFET1			0.096	V	SRFET on-time drain voltage for output 1
131	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
132	RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
160	PO_TOTAL			34.99	W	Total power of all outputs
161	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
165	**TOLERANCE ANALYSIS**					
166	USER_VIN			300	V	Input DC voltage corner to be evaluated
167	USER_ILIMIT	TYP		1.600	A	Current limit corner to be evaluated
168	USER_LPRIMARY	TYP		1103.5	uH	Primary inductance corner to be evaluated
169	MODE_OPERATION			DCM		Mode of operation
170	KP			3.596		Measure of continuous/discontinuous mode of operation
171	FSWITCHING			37890	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
172	VMIN				V	Valley of the minimum input AC voltage at full load
173	DUTYCYCLE			0.188		Steady state duty cycle
174	TIME_ON			4.97	us	Primary switch on-time
175	TIME_OFF			21.42	us	Primary switch off-time

176	IPEAK_PRIMARY			1.350	A	Primary switch peak current
177	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
178	IAVERAGE_PRIMARY			0.127	A	Primary switch average current
179	IRIPPLE_PRIMARY			1.350	A	Primary switch ripple current
180	IRMS_PRIMARY			0.338	A	Primary switch RMS current
181	BPEAK			3218	Gauss	Peak flux density
182	BMAX			2652	Gauss	Maximum flux density
183	BAC			1326	Gauss	AC flux density (0.5 x Peak to Peak)

8 Performance Data

Measured at PCB output terminal.

8.1 *Efficiency vs. Load and Input Voltage*

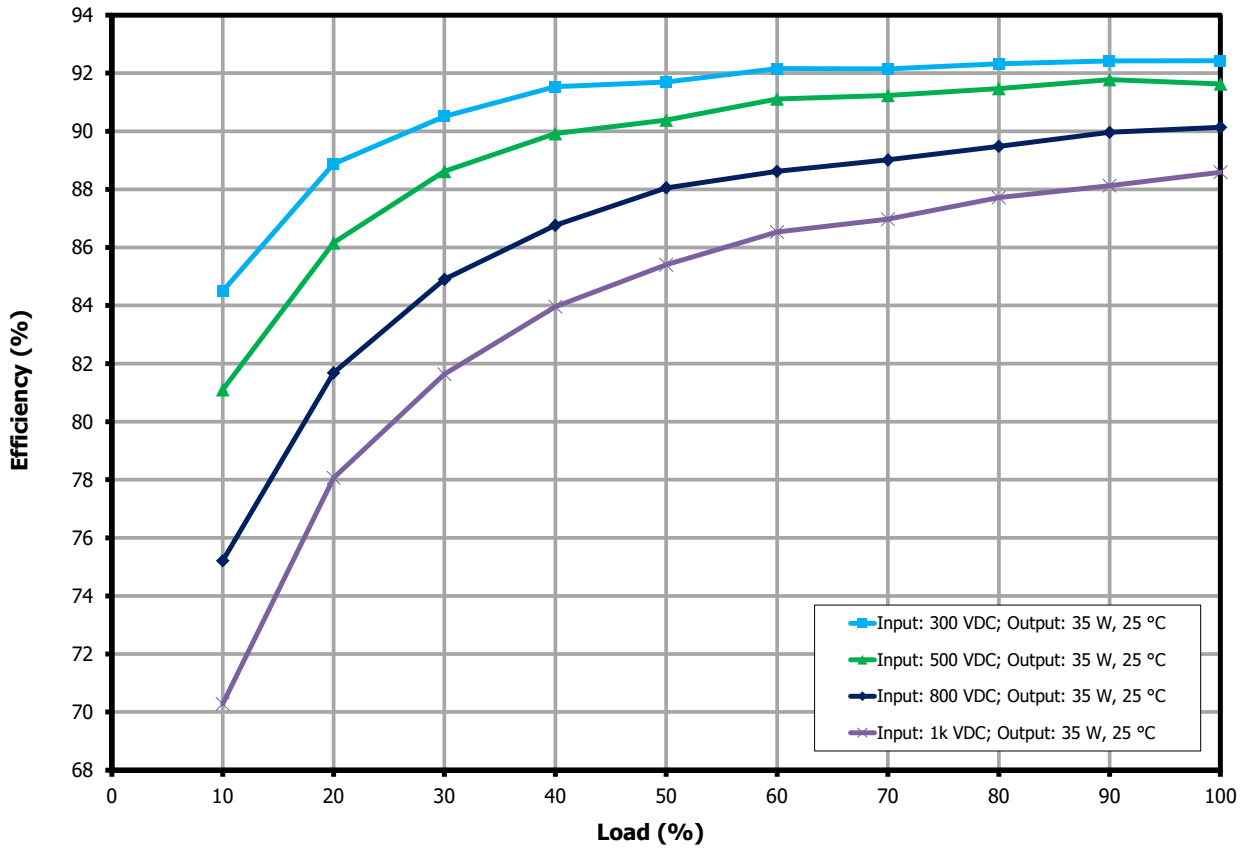


Figure 10 – Efficiency vs. Load and Input Voltage, 25 ºC Ambient Temperature.

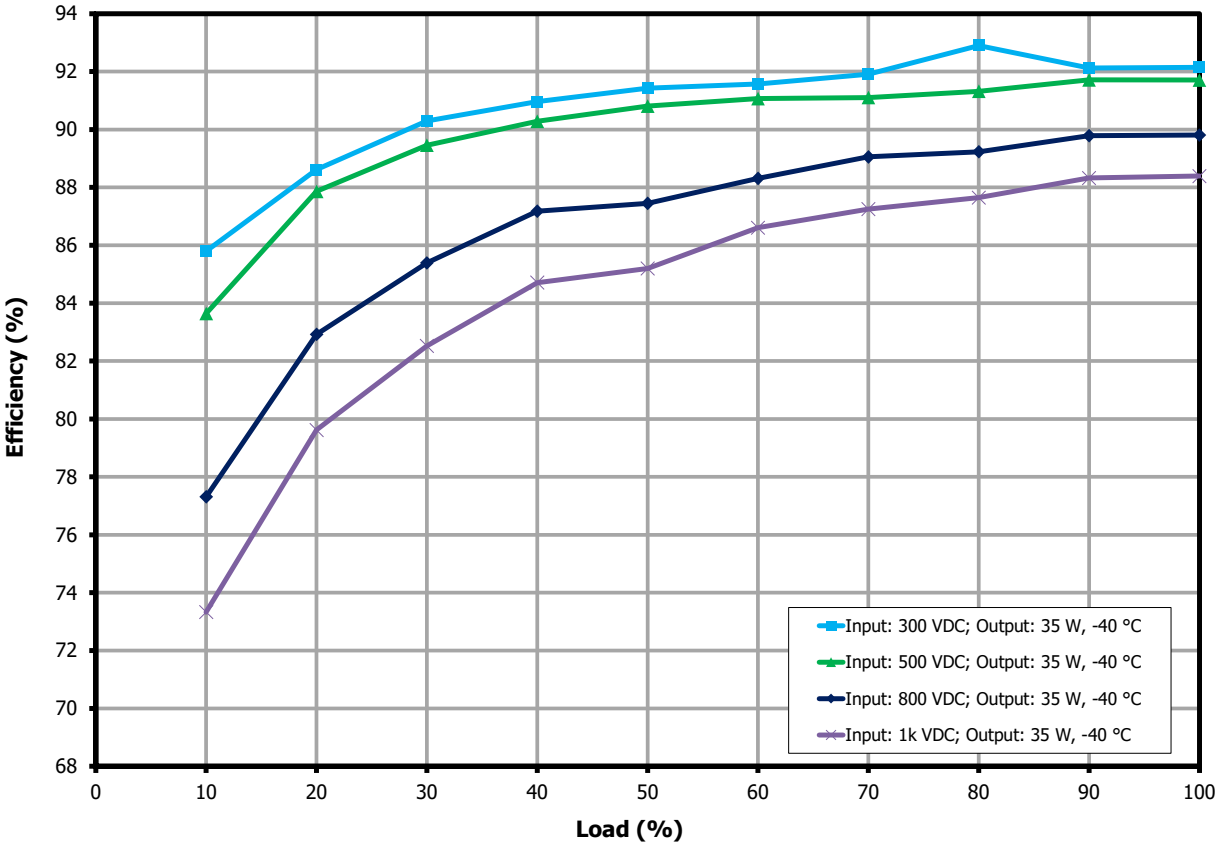


Figure 11 – Efficiency vs. Load and Input Voltage, -40 ºC Ambient Temperature.

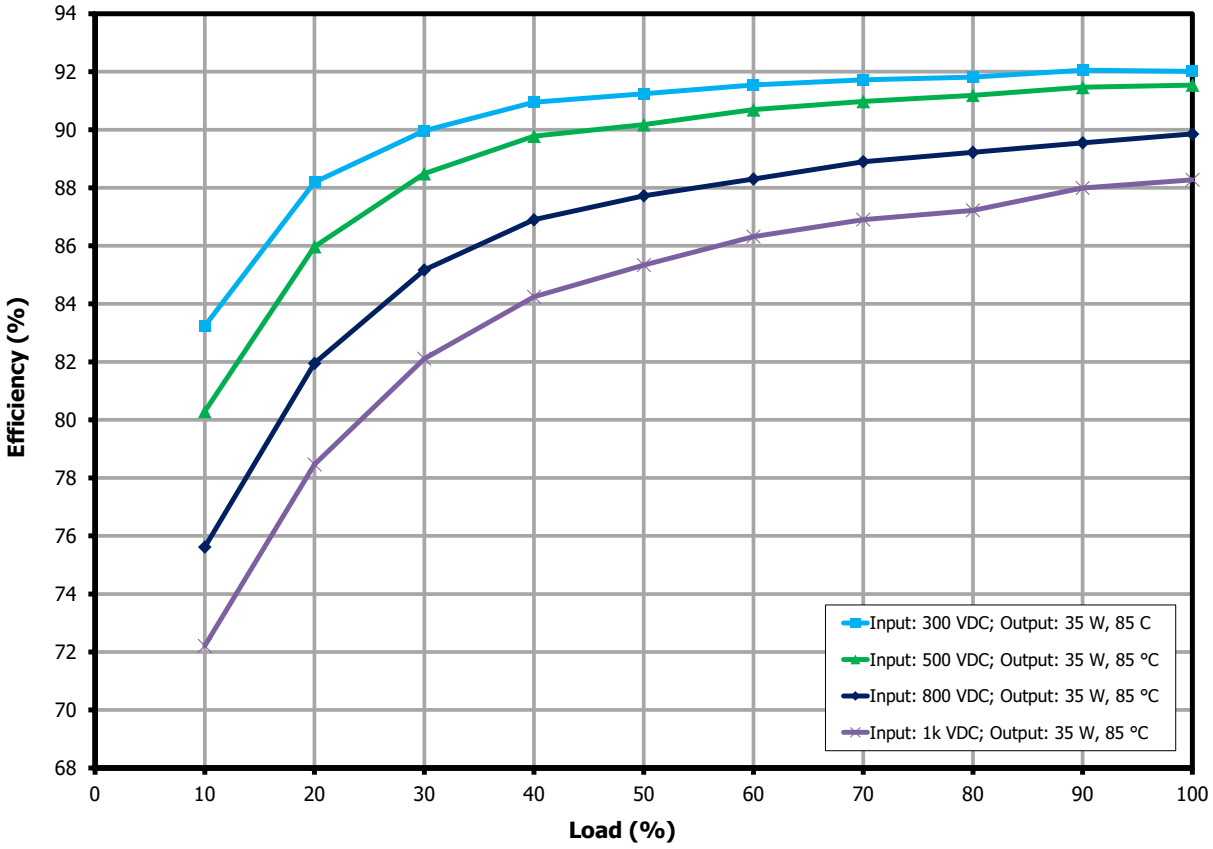


Figure 12 – Efficiency vs. Load and Input Voltage, 85 ºC Ambient Temperature.

8.2 *Full Load Efficiency vs. Line*

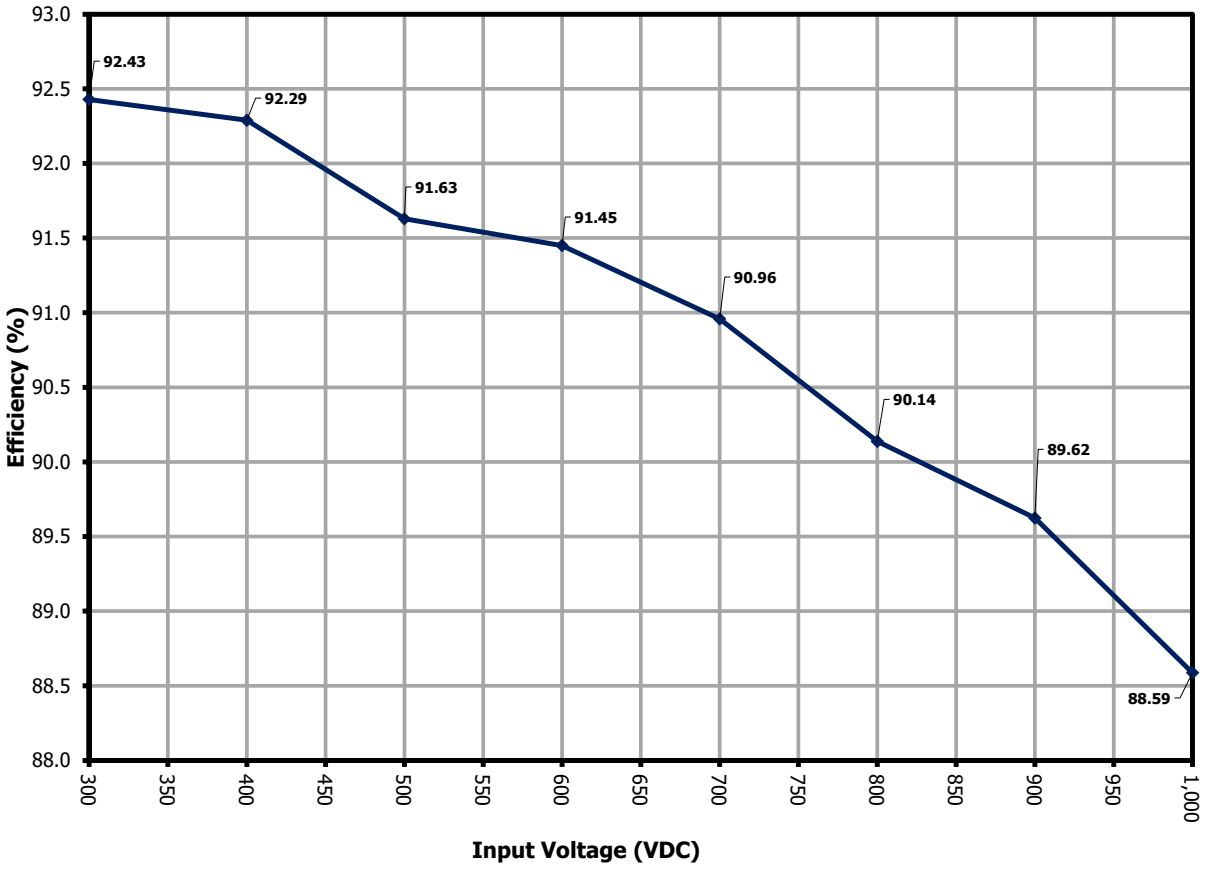


Figure 13 – Efficiency vs. Line (VDC), Room Temperature.

8.3 *Maximum Power at Low Input Voltage*

V_{IN} (VDC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
40	5.53	24.02	0.20	4.81	87.03
50	10.88	23.38	0.42	9.82	90.30
60	16.23	23.48	0.63	14.79	91.16
70	17.81	24.03	0.68	16.22	91.10
80	17.84	24.09	0.68	16.38	91.83
90	17.82	24.10	0.68	16.39	91.98
100	17.78	24.09	0.68	16.38	92.13
200	27.86	24.12	1.07	25.69	92.20

8.4 *No-Load Input Power*

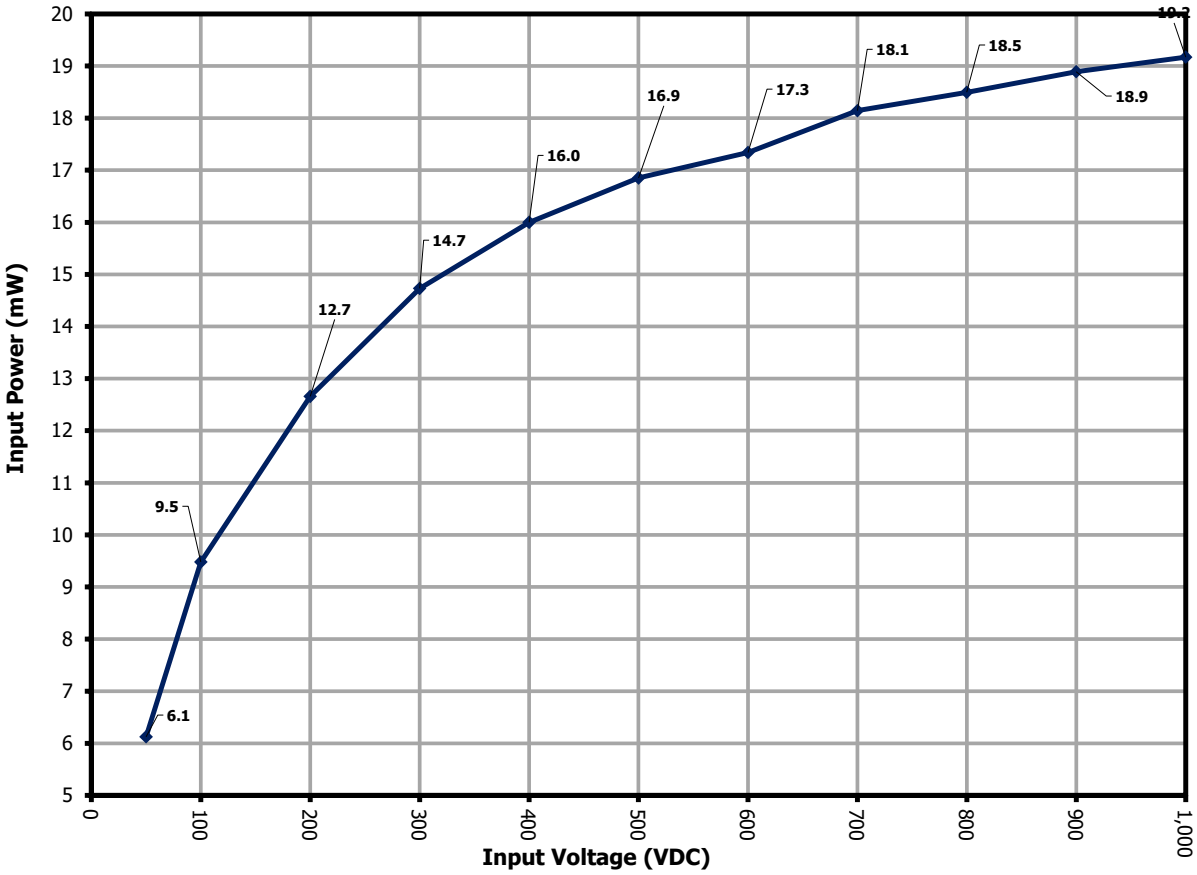


Figure 14 – No-Load Input Power, Room Temperature.

8.5 *Load and Line Regulation*

Measurements taken at 0% to 100% of rated load

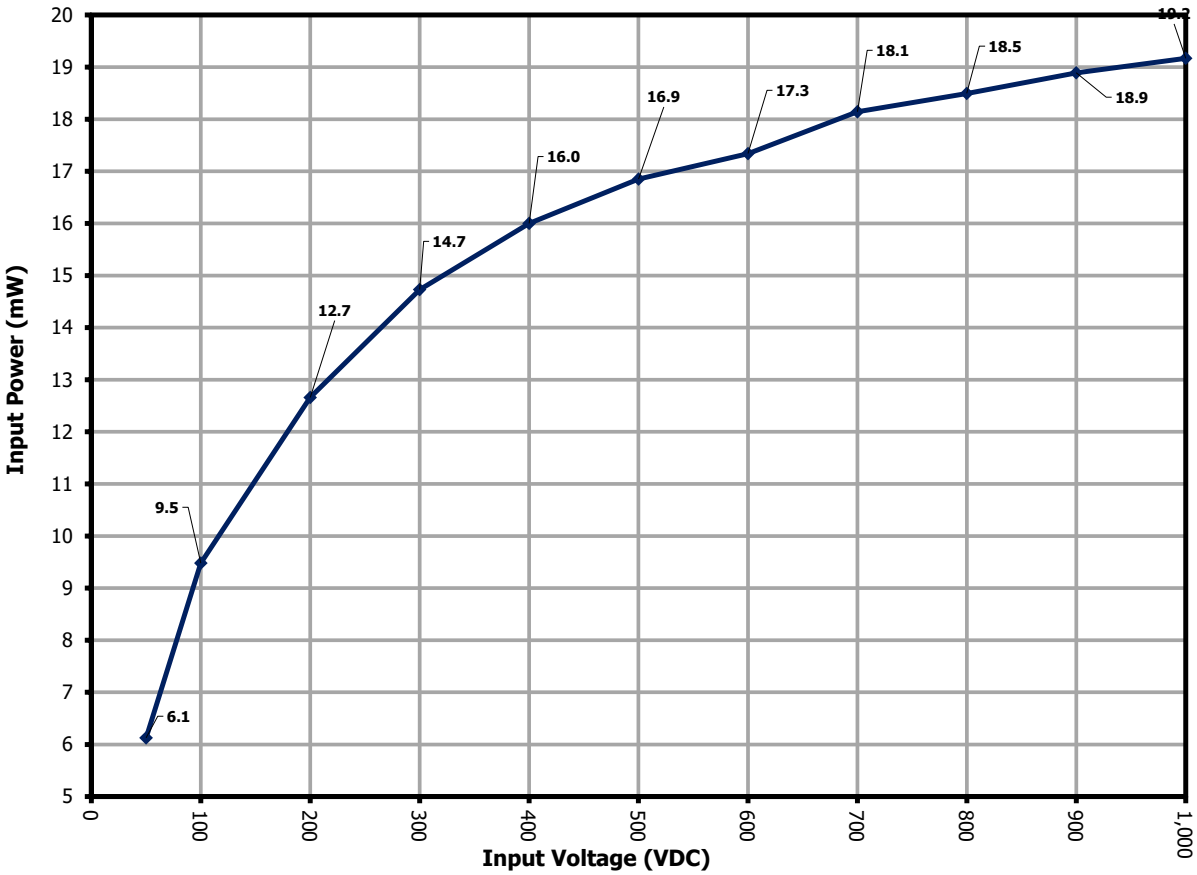


Figure 15 – Output Voltage vs. Output Current and Input Voltage (VDC), 25 ºC Ambient Temperature.

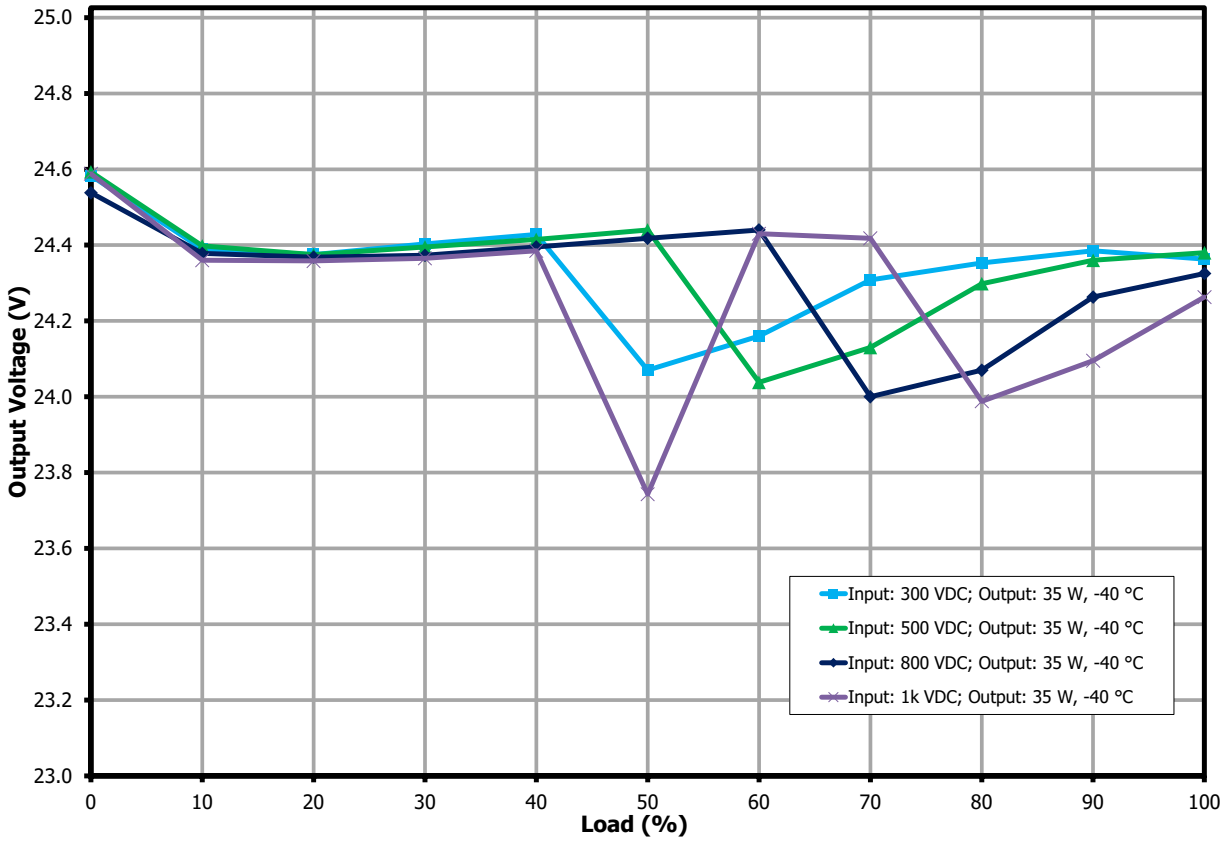


Figure 16 – Output Voltage vs. Output Current and Input Voltage (VDC), -40 ºC Ambient Temperature.

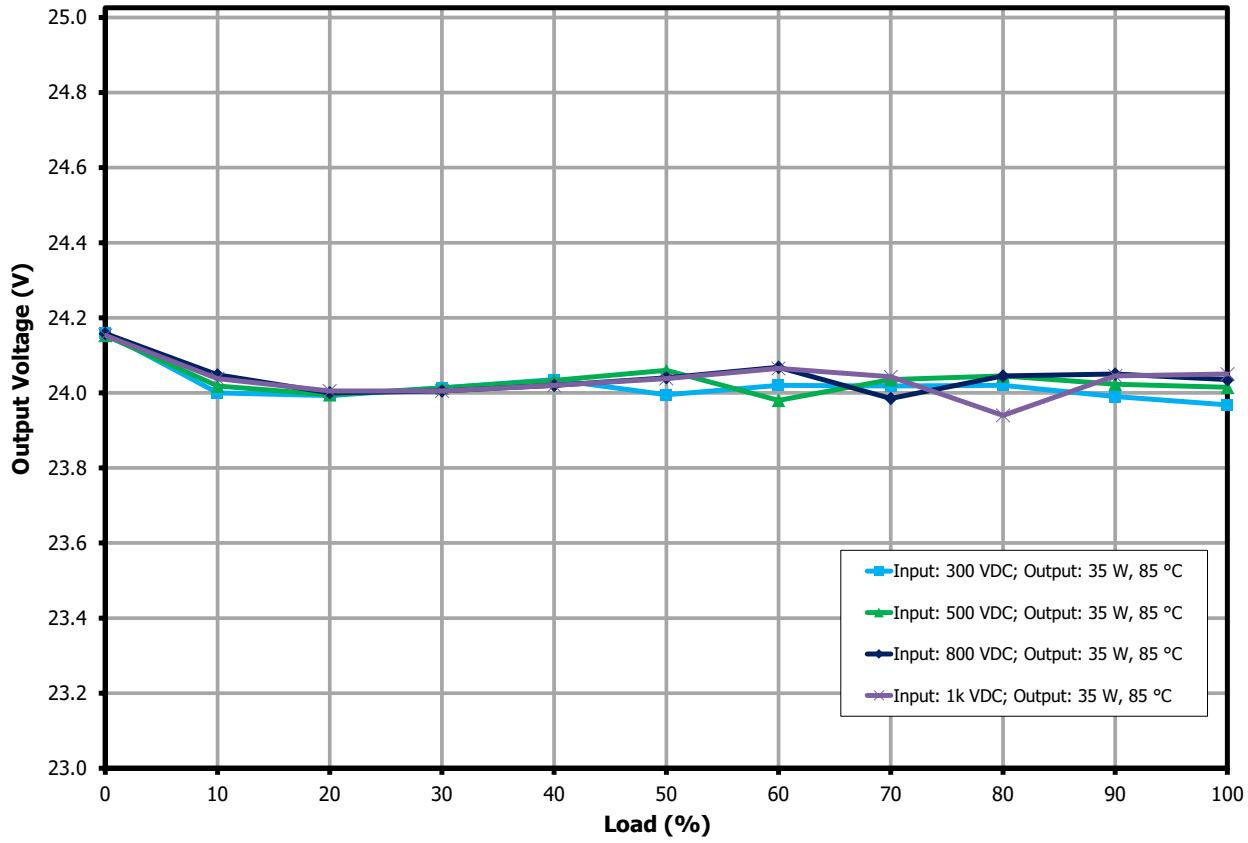


Figure 17 – Output Voltage vs. Output Current and Input Voltage (VDC), 85 ºC Ambient Temperature.

9 Waveforms

9.1 *INN3647C Drain Voltage and Current, Steady-State*

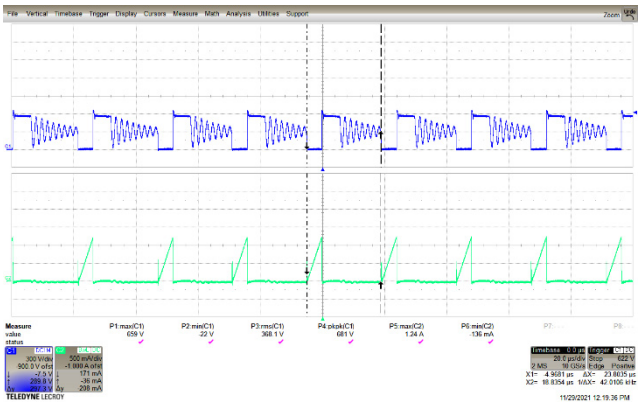


Figure 18 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 659 V.
$I_{DS(MAX)}$ = 1.24 A.
Upper: V_{DRAIN}, 300 V, 20 μs / div.
Lower: I_{DRAIN}, 500 mA, 20 μs / div.

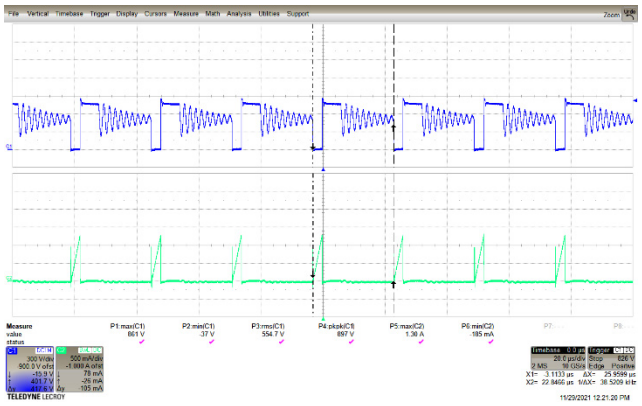


Figure 19 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 861 V.
$I_{DS(MAX)}$ = 1.30 A.
Upper: V_{DRAIN}, 300 V, 20 μs / div.
Lower: I_{DRAIN}, 500 mA, 20 μs / div.

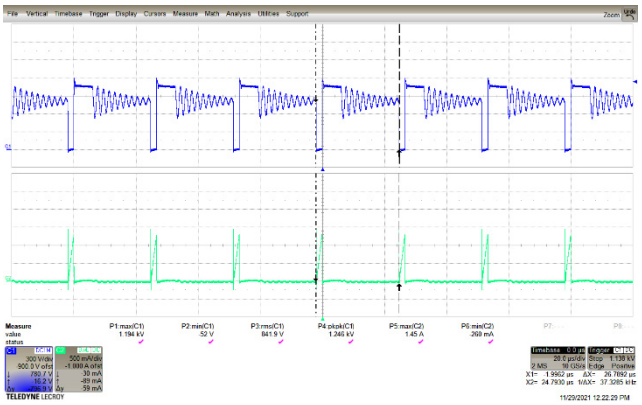


Figure 20 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 1195 V.
$I_{DS(MAX)}$ = 1.45 A.
Upper: V_{DRAIN}, 300 V, 20 μs / div.
Lower: I_{DRAIN}, 500 mA, 20 μs / div.

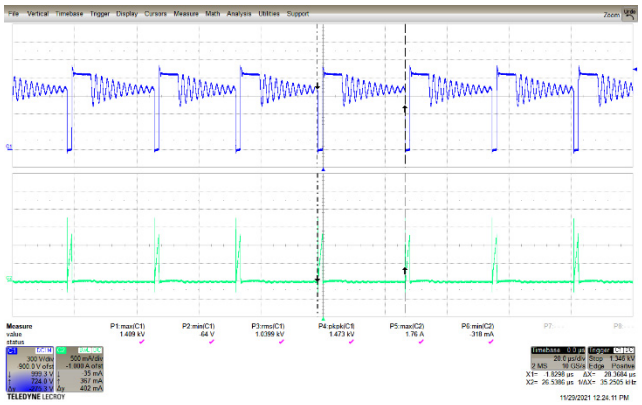


Figure 21 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 1409 V.
$I_{DS(MAX)}$ = 1.76 A.
Upper: V_{DRAIN}, 300 V, 20 μs / div.
Lower: I_{DRAIN}, 500 mA, 20 μs / div.

9.2 *INN3647C Drain Voltage and Current, Start-up*

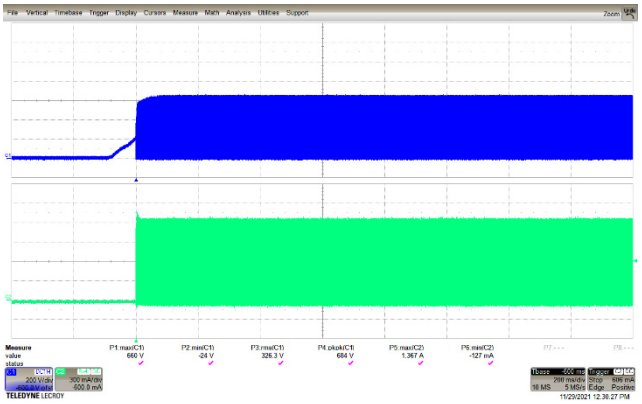


Figure 22 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 660 V.
$I_{DS(MAX)}$ = 1.37 A.
Upper: V_{DRAIN}, 200 V, 200 ms / div.
Lower: I_{DRAIN}, 300 mA, 200 ms / div.

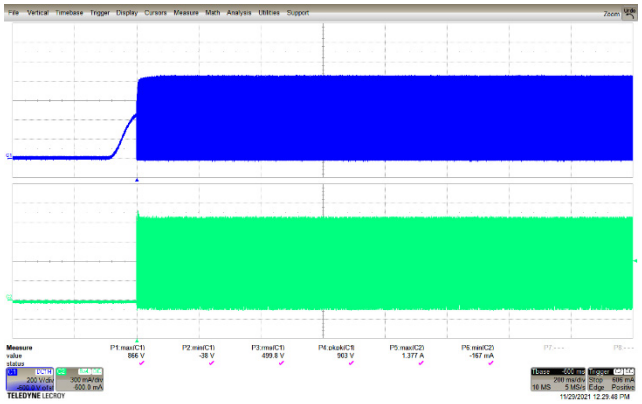


Figure 23 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 866 V.
$I_{DS(MAX)}$ = 1.38 A.
Upper: V_{DRAIN}, 200 V, 200 ms / div.
Lower: I_{DRAIN}, 300 mA, 200 ms / div.

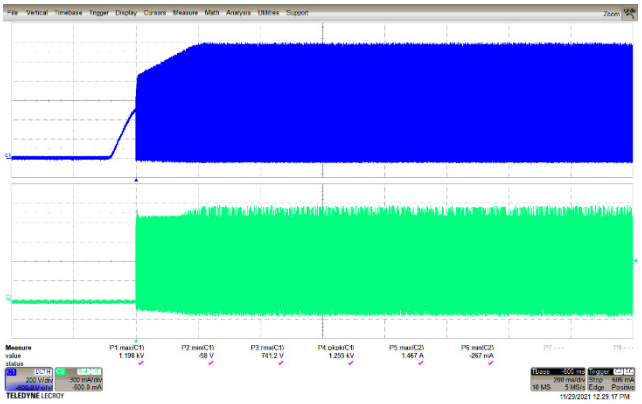


Figure 24 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 1198 V.
$I_{DS(MAX)}$ = 1.47 A.
Upper: V_{DRAIN}, 200 V, 200 ms / div.
Lower: I_{DRAIN}, 300 mA, 200 ms / div.

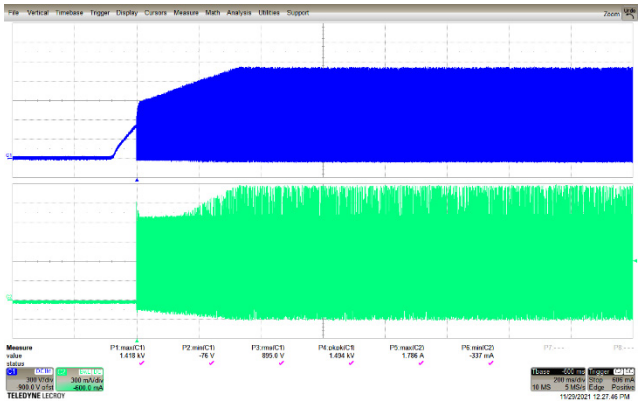


Figure 25 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A.
$V_{DS(MAX)}$ = 1418 V.
$I_{DS(MAX)}$ = 1.79 A.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 400 mA, 200 ms / div.

9.3 *INN3647C Drain Voltage and Current, Output Shorted*

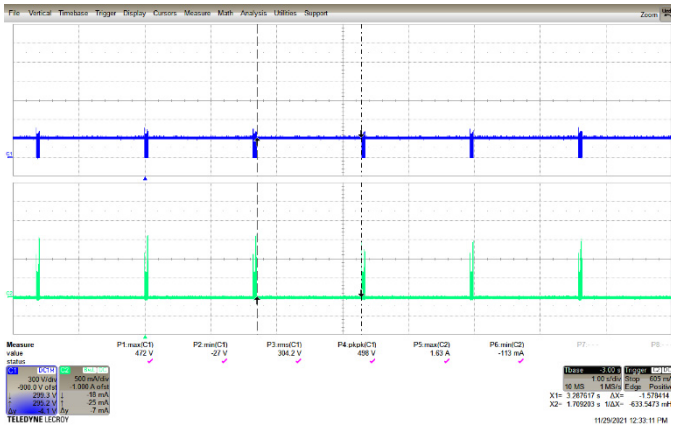


Figure 26 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 472 V.
$I_{DS(MAX)}$ = 1.63 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

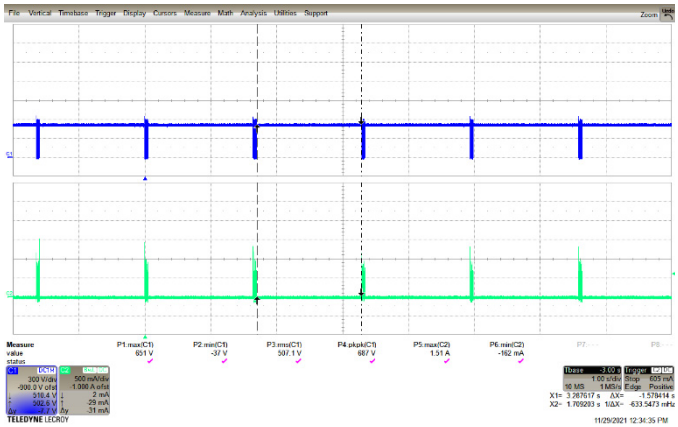


Figure 27 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 651 V.
$I_{DS(MAX)}$ = 1.51 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

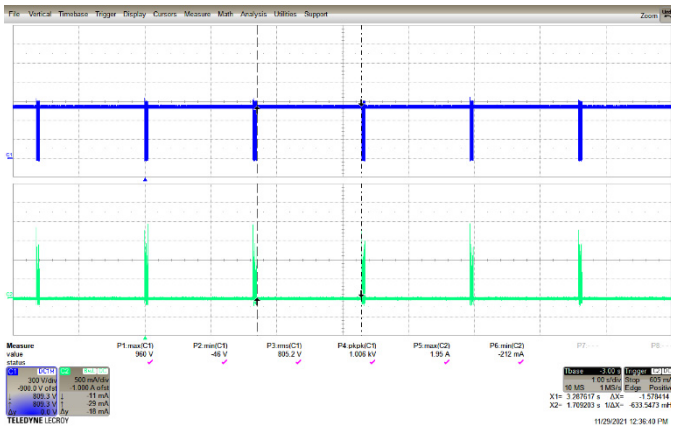


Figure 28 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 960 V.
$I_{DS(MAX)}$ = 1.95 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

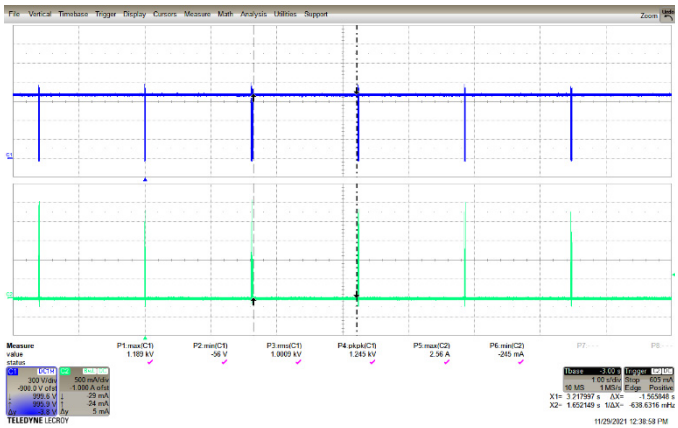


Figure 29 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 1189 V.
$I_{DS(MAX)}$ = 2.56 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

9.4 *SR FET Waveforms, Steady-State*

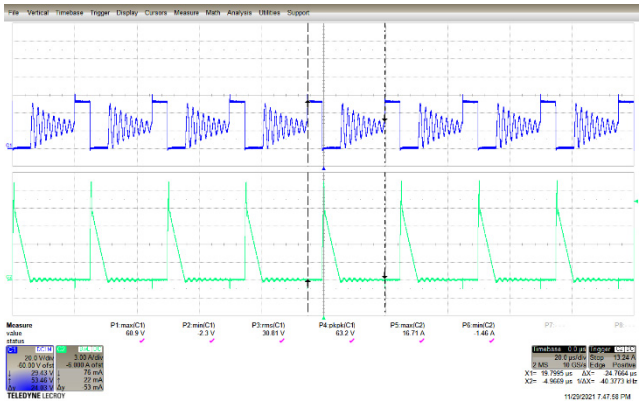


Figure 30 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 60.9 V.
SRFET $I_{DS(MAX)}$ = 16.7 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 3 A, 20 µs / div.

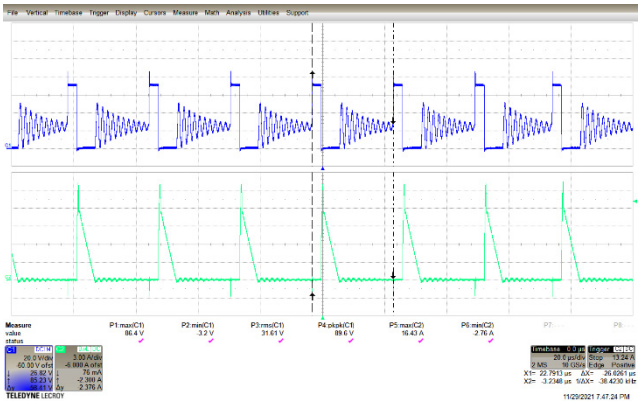


Figure 31 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 86.4 V.
SRFET $I_{DS(MAX)}$ = 16.4 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

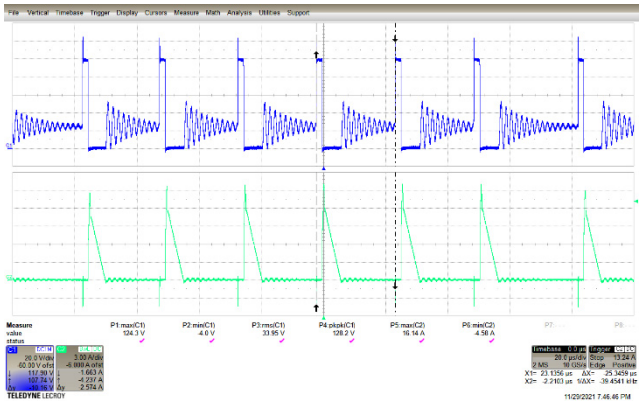


Figure 32 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 124.3 V.
SRFET $I_{DS(MAX)}$ = 16.14 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

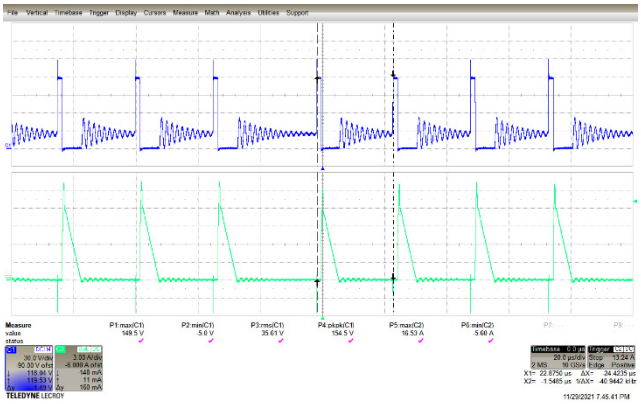


Figure 33 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 149.5 V.
SRFET $I_{DS(MAX)}$ = 16.53 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

9.5 *SR FET Waveforms, Start-up*

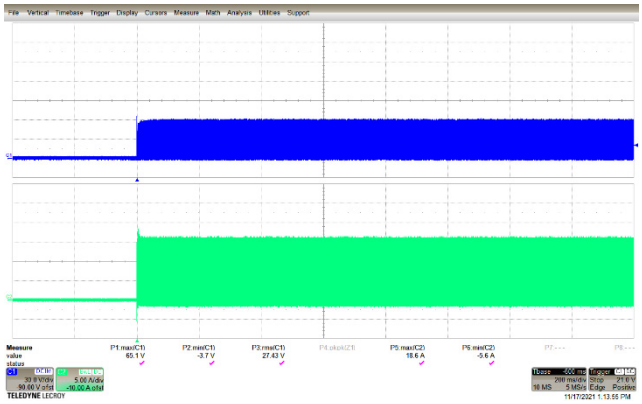


Figure 34 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 65.1 V.
SRFET $I_{DS(MAX)}$ = 18.6 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

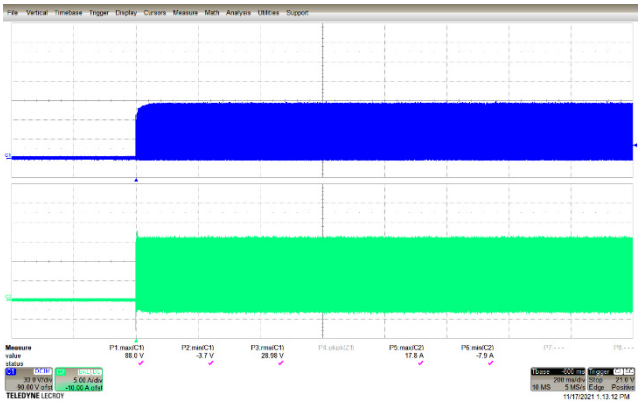


Figure 35 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 88.0 V.
SRFET $I_{DS(MAX)}$ = 17.8 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

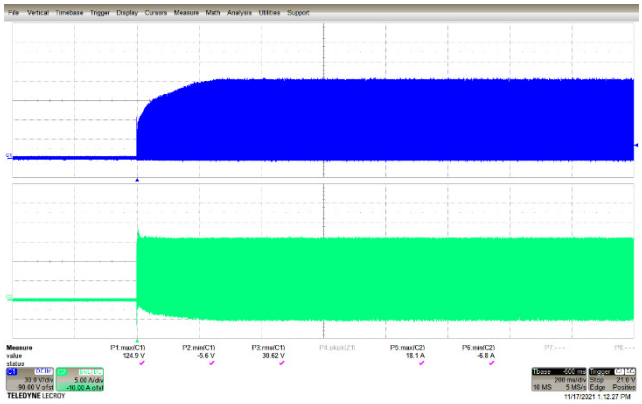


Figure 36 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 124.9 V.
SRFET $I_{DS(MAX)}$ = 18.1 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

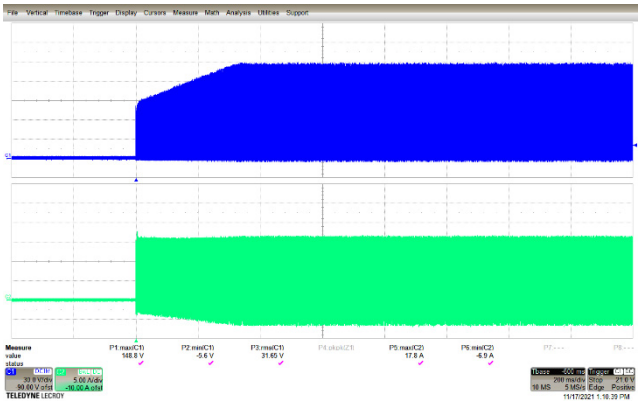


Figure 37 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A.
SRFET $V_{DS(MAX)}$ = 148.8 V.
SRFET $I_{DS(MAX)}$ = 17.8 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

9.6 *SR FET Waveforms, Output Shorted*

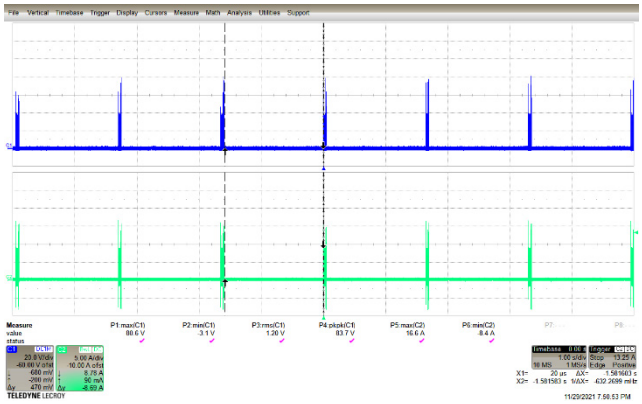


Figure 38 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = Output Shorted.
SRFET $V_{DS(MAX)}$ = 80.6 V.
SRFET $I_{DS(MAX)}$ = 16.6 A.
Upper: SRFET V_{DS}, 20 V, 1 s / div.
Lower: SRFET I_{DS}, 5 A, 1 s / div.

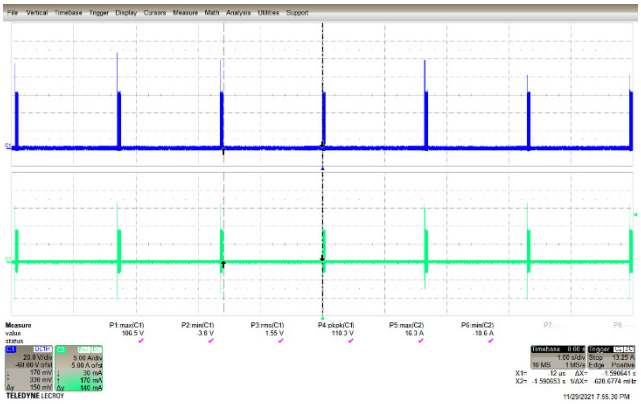


Figure 39 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = Output Shorted.
SRFET $V_{DS(MAX)}$ = 106.5 V.
SRFET $I_{DS(MAX)}$ = 16.3 A.
Upper: SRFET V_{DS}, 20 V, 1 s / div.
Lower: SRFET I_{DS}, 5 A, 1 s / div.

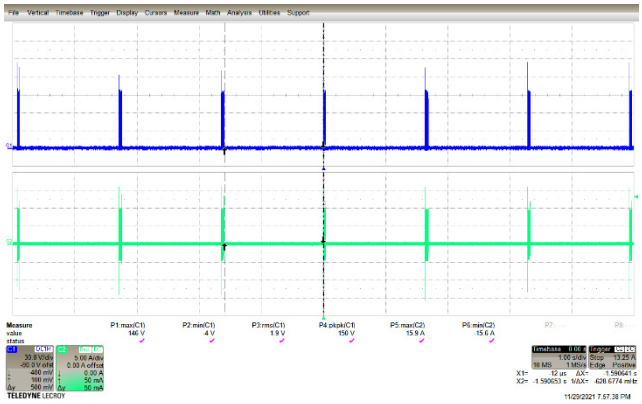


Figure 40 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = Output Shorted.
SRFET $V_{DS(MAX)}$ = 146 V.
SRFET $I_{DS(MAX)}$ = 15.9 A.
Upper: SRFET V_{DS}, 30 V, 1 s / div.
Lower: SRFET I_{DS}, 5 A, 1 s / div..

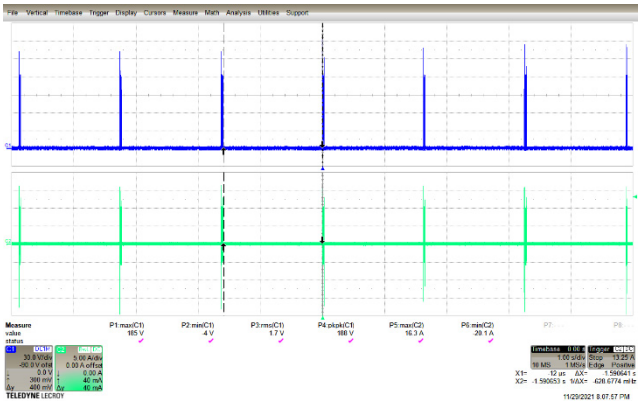


Figure 41 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = Output Shorted.
SRFET $V_{DS(MAX)}$ = 185 V.
SRFET $I_{DS(MAX)}$ = 16.3 A.
Upper: SRFET V_{DS}, 30 V, 1 s / div.
Lower: SRFET I_{DS}, 5 A, 1 s / div.

9.7 *Output Ripple Measurements*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor includes one (1) 1 μF/50 V ceramic type.

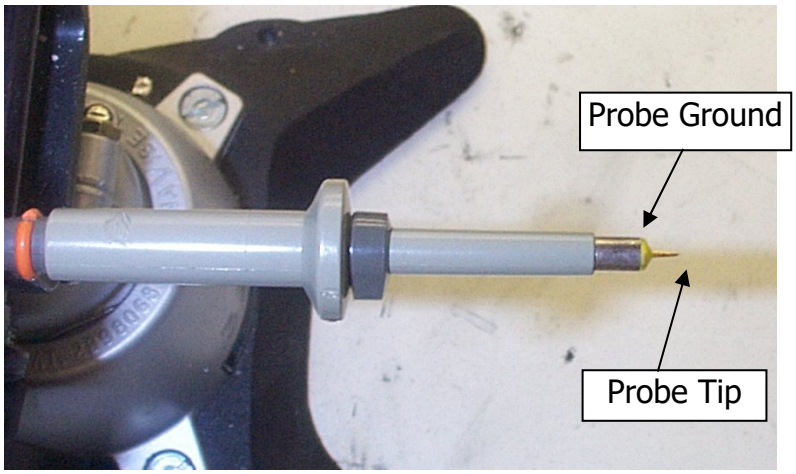


Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

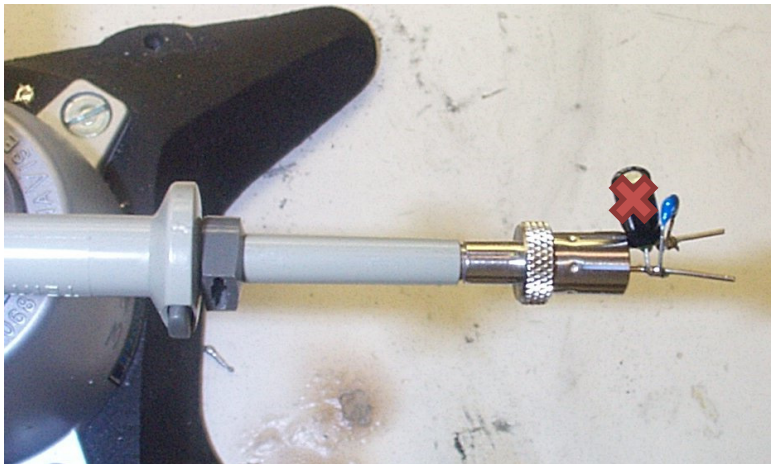


Figure 43 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)

9.7.1 100% Loading Condition

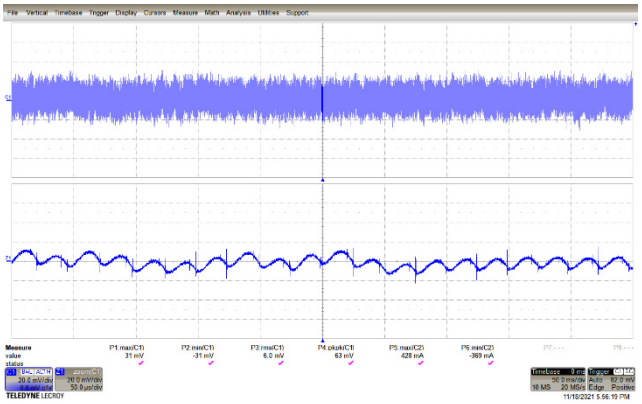


Figure 44 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 63 mV_{P-P}.

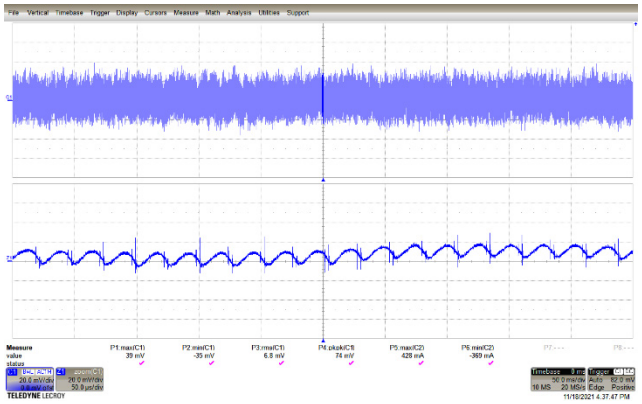


Figure 45 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 74 mV_{P-P}.

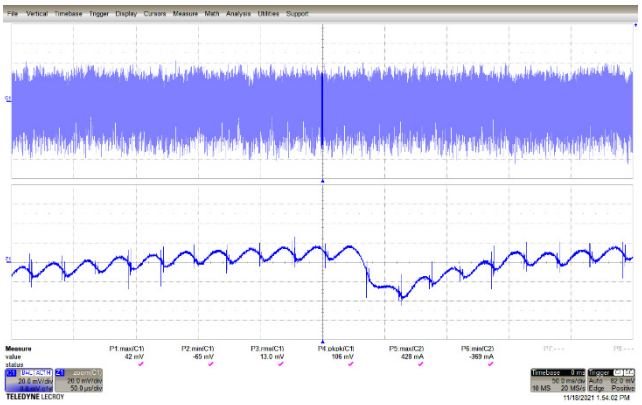


Figure 46 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 106 mV_{P-P}.

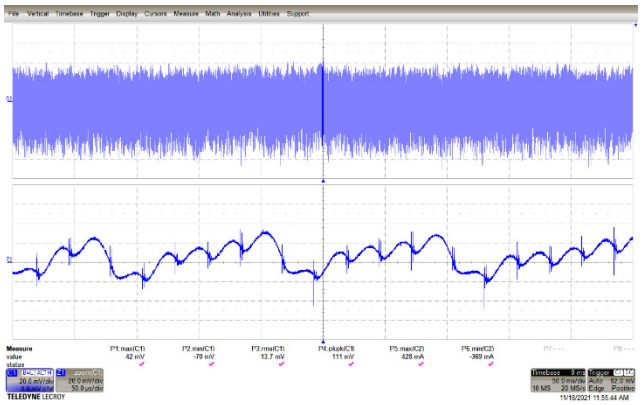


Figure 47 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 111 mV_{P-P}.

9.7.2 75% Loading Condition

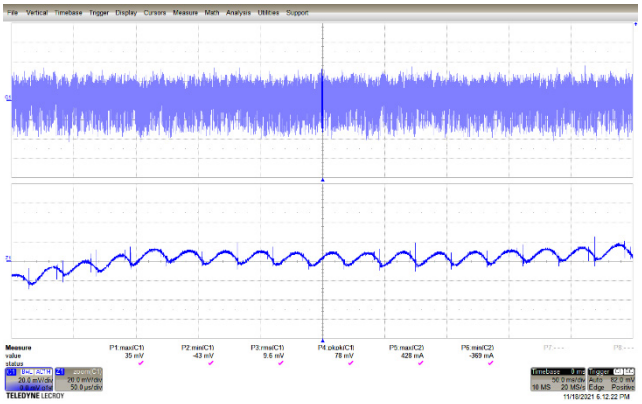


Figure 48 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 1.0935 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 78 mV_{P-P}.

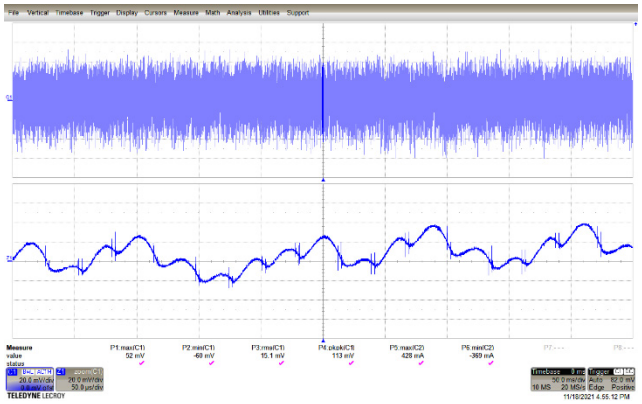


Figure 49 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 1.0935 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 113 mV_{P-P}.

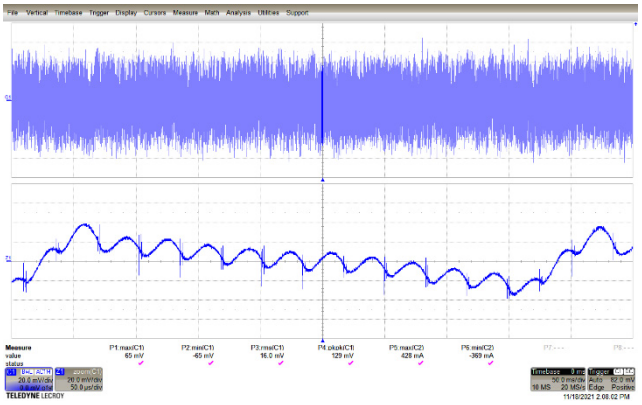


Figure 50 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.0935 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 129 mV_{P-P}.

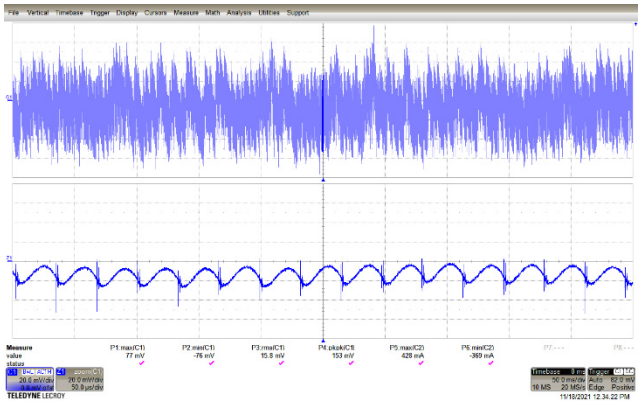


Figure 51 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.0935 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 153 mV_{P-P}.

9.7.3 50% Loading Condition

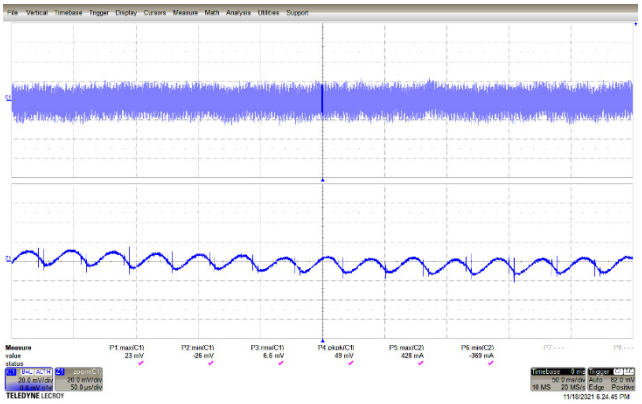


Figure 52 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 0.729 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 49 mV_{P-P}.

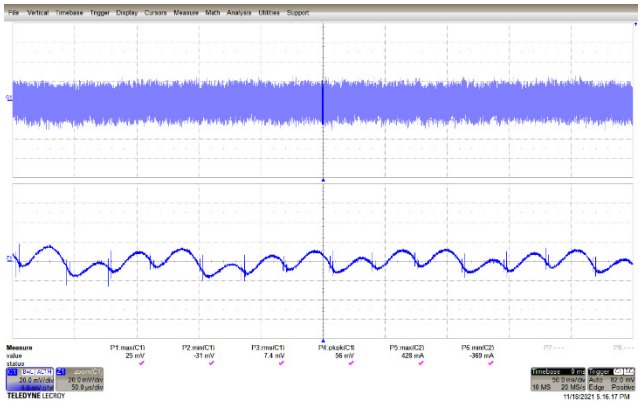


Figure 53 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 0.729 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 56 mV_{P-P}.

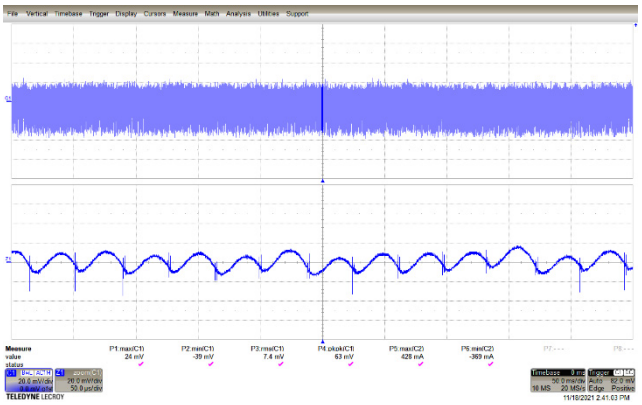


Figure 54 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0.729 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 63 mV_{P-P}.

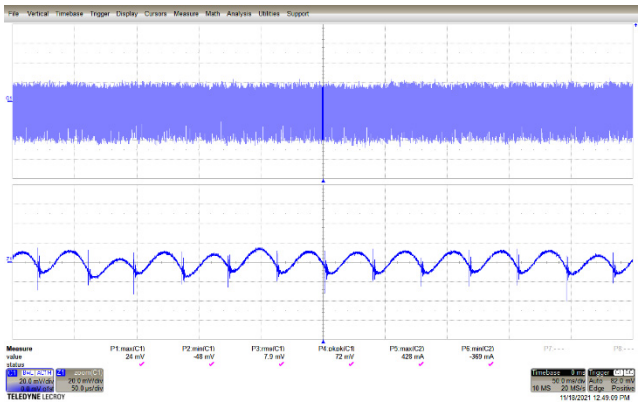


Figure 55 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 0.729 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 72 mV_{P-P}.

9.7.4 25% Loading Condition

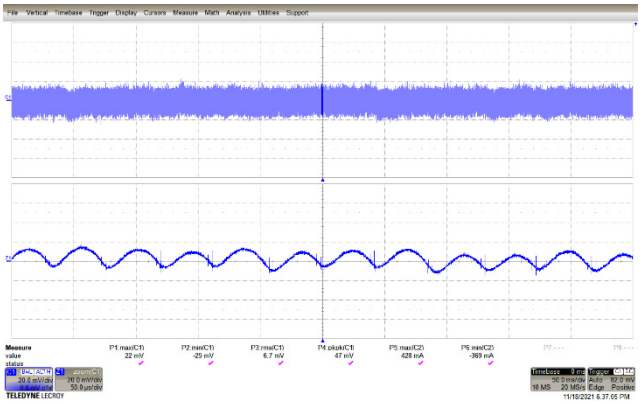


Figure 56 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 0.3645 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 47 mV_{P-P}.

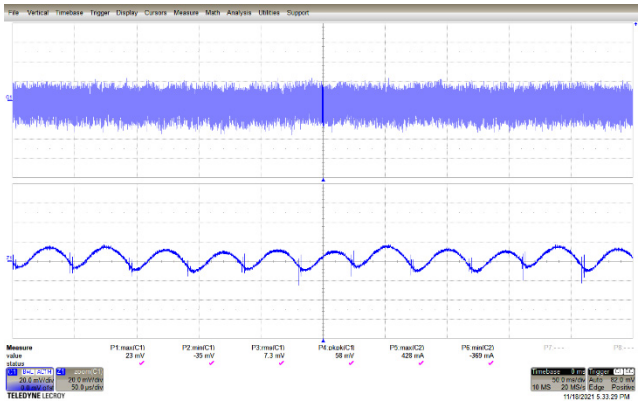


Figure 57 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 0.3645 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 58 mV_{P-P}.

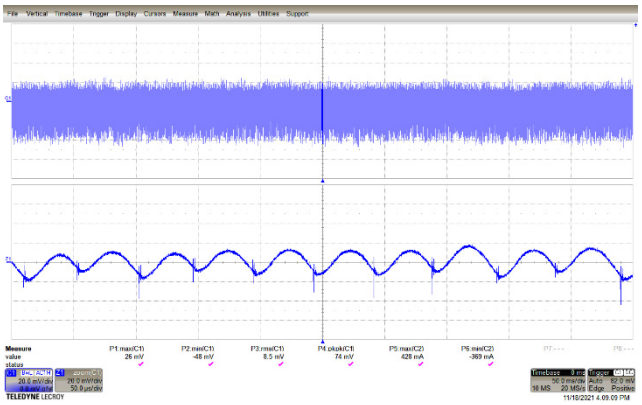


Figure 58 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0.3645 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 74 mV_{P-P}.

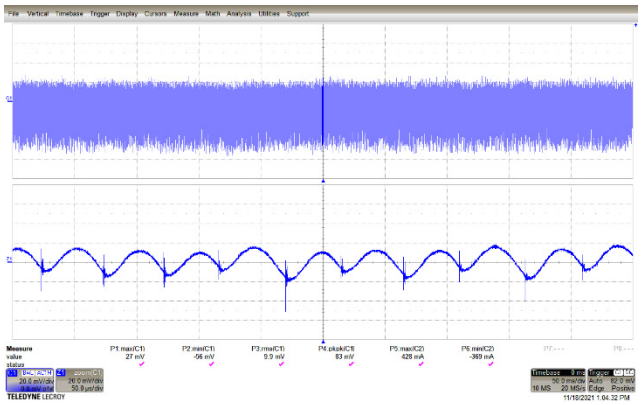


Figure 59 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 0.3645 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 83 mV_{P-P}.

9.7.5 0% Loading Condition

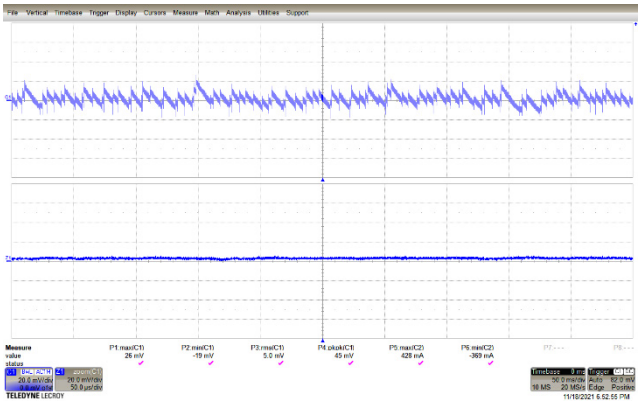


Figure 60 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 49 mV_{P-P}.

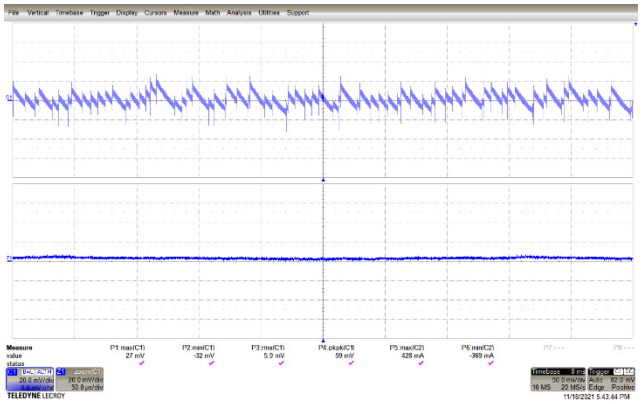


Figure 61 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 99 mV_{P-P}.

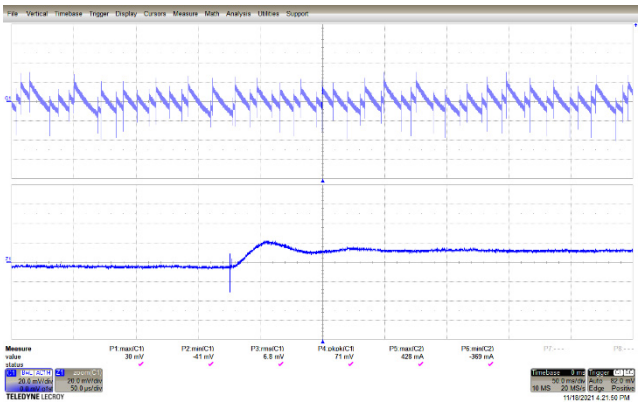


Figure 62 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 71 mV_{P-P}.

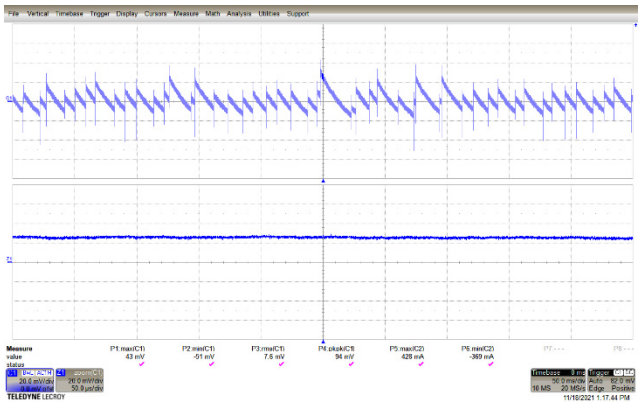


Figure 63 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 94 mV_{P-P}.

9.8 *Output Voltage Ripple (ATE)*

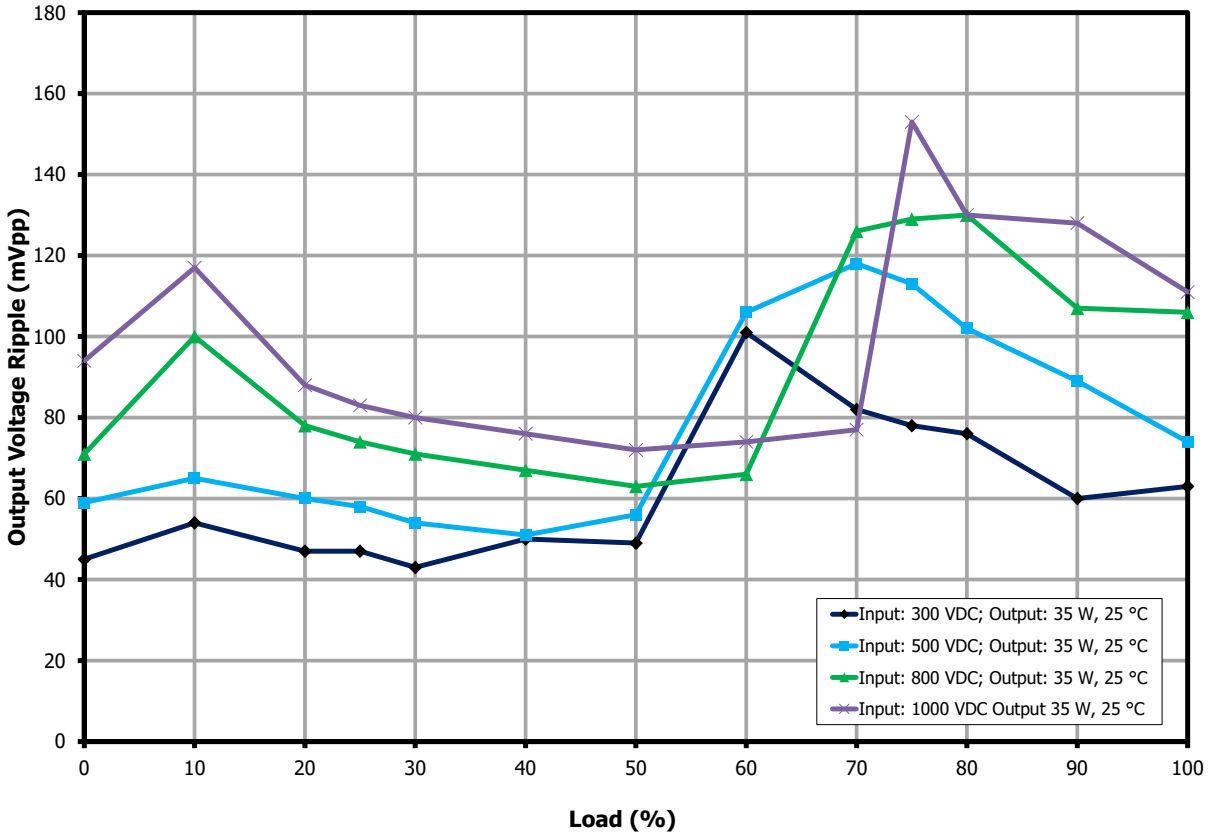


Figure 64 – Output Voltage Ripple, 25 ºC Ambient Temperature.

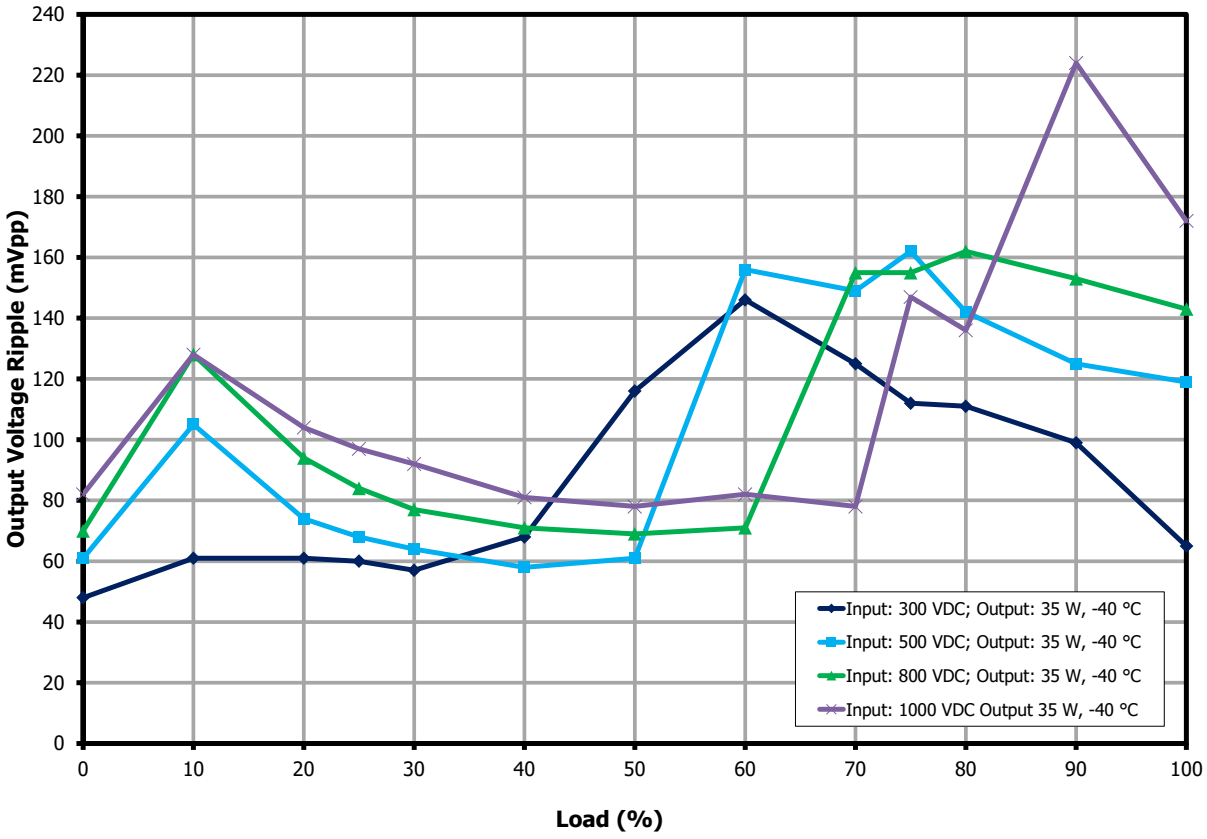


Figure 65 – Output Voltage Ripple, -40 ºC Ambient Temperature.

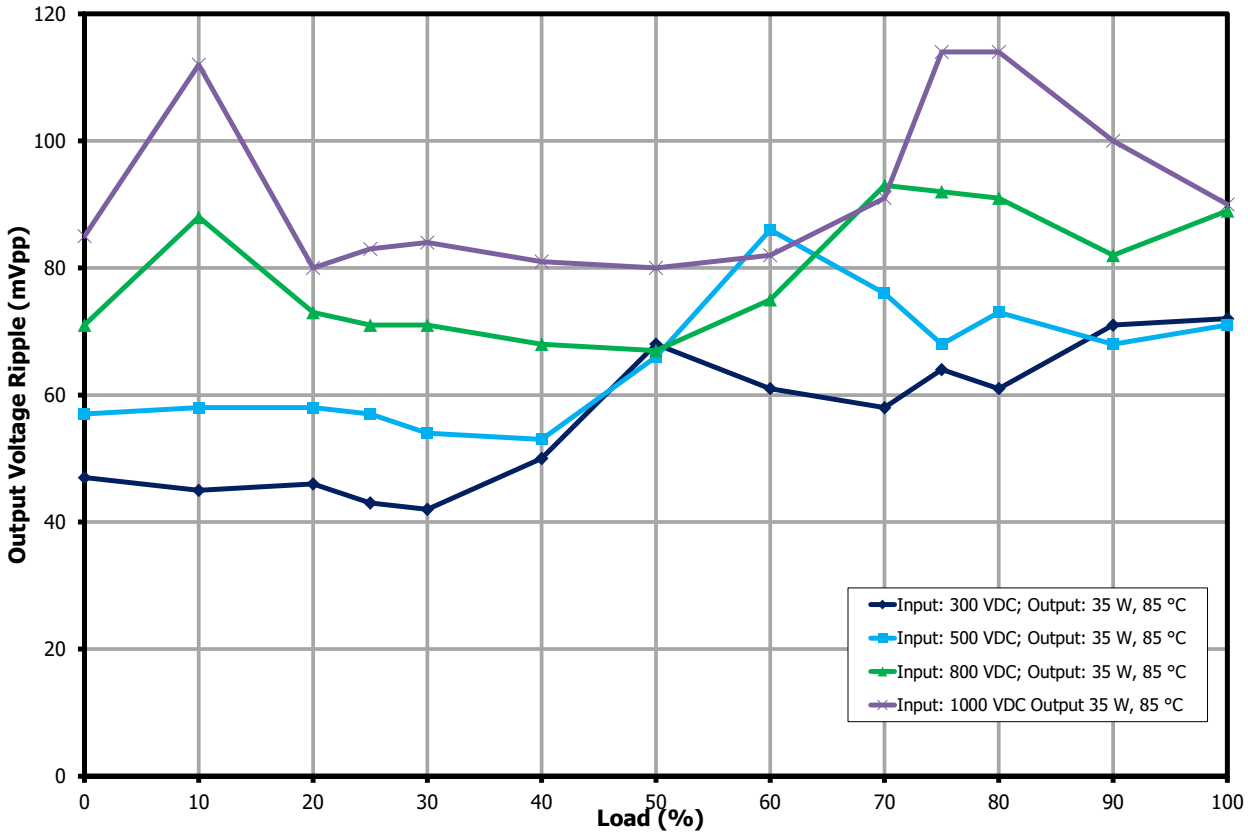


Figure 66 – Output Voltage Ripple, 85 ºC Ambient Temperature.

9.9 *Output Load Transient*

9.9.1 Output Load Transient, 100% to 50% Load

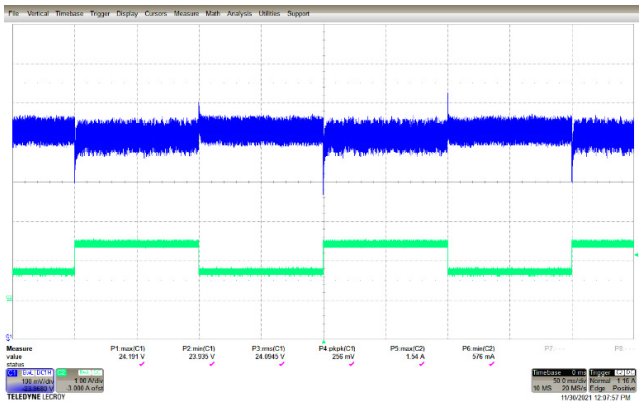


Figure 67 – Output Load Transient, 100-50% Load.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A to 0.729 A.
$V_{OUT(MAX)}$ = 24.19 V, $V_{OUT(MIN)}$= 23.94 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

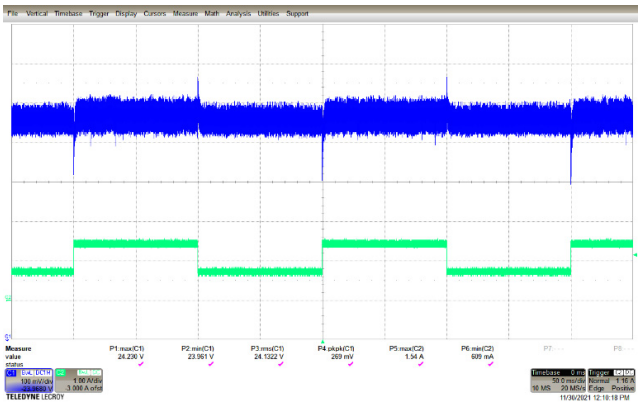


Figure 68 – Output Load Transient, 100-50% Load.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A to 0.729 A.
$V_{OUT(MAX)}$ = 24.23 V, $V_{OUT(MIN)}$= 23.96 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

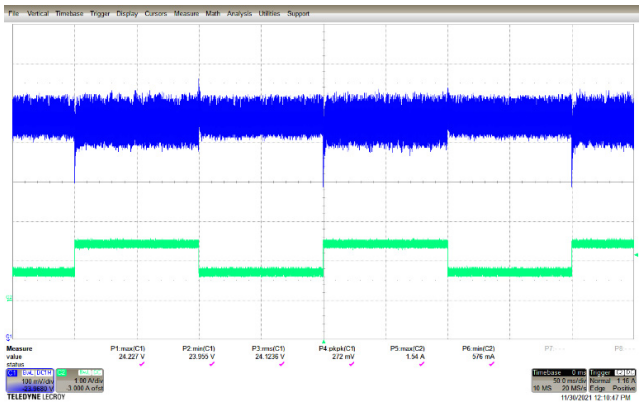


Figure 69 – Output Load Transient, 100-50% Load.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A to 0.729 A.
$V_{OUT(MAX)}$ = 24.23 V, $V_{OUT(MIN)}$= 23.96 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

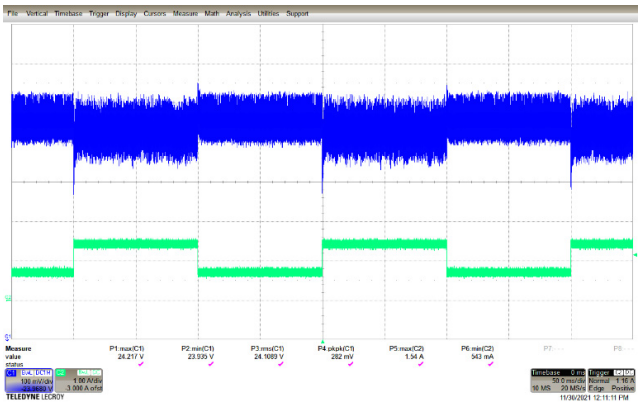


Figure 70 – Output Load Transient, 100-50% Load.
V_{IN} = 1000 VDC, I_{OUT}=1.458 A to 0.729 A.
$V_{OUT(MAX)}$ = 24.22 V, $V_{OUT(MIN)}$= 23.94 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

9.9.2 Output Load Transient, 100% to 0% Load

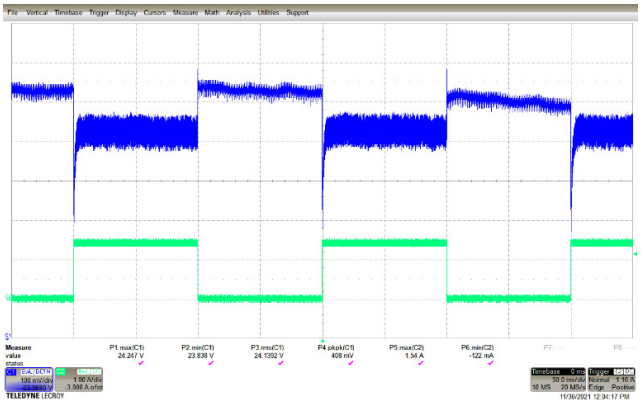


Figure 71 – Output Load Transient, 100-0% Load.
V_{IN} = 300 VDC, I_{OUT} = 1.458 A to 0 A.
$V_{OUT(MAX)}$ = 24.25 V, $V_{OUT(MIN)}$= 23.84 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

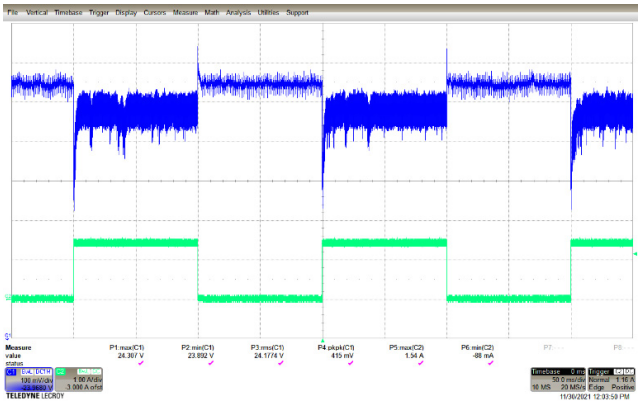


Figure 72 – Output Load Transient, 100-0% Load.
V_{IN} = 500 VDC, I_{OUT} = 1.458 A to 0 A.
$V_{OUT(MAX)}$ = 24.31 V, $V_{OUT(MIN)}$= 23.89 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

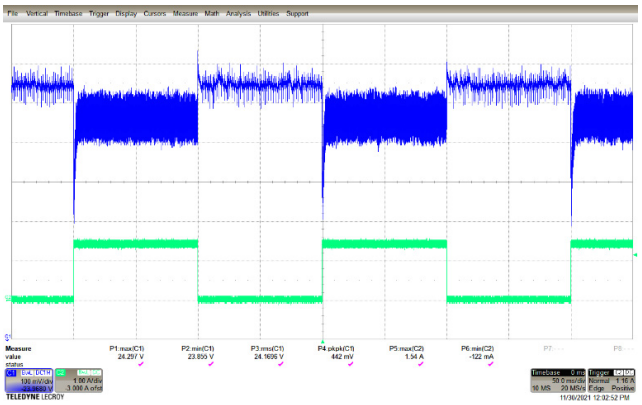


Figure 73 – Output Load Transient, 100-0% Load.
V_{IN} = 800 VDC, I_{OUT} = 1.458 A to 0 A.
$V_{OUT(MAX)}$ = 24.30 V, $V_{OUT(MIN)}$= 23.86 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

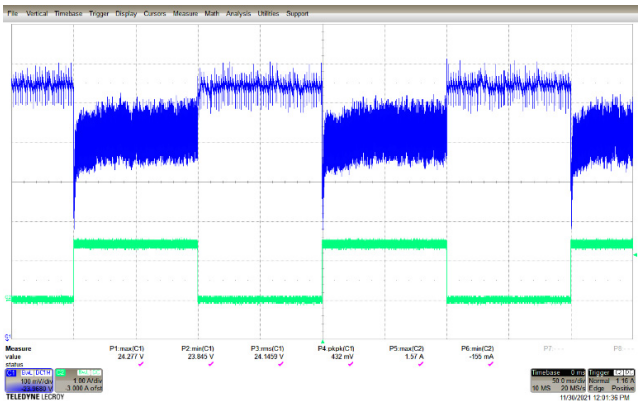


Figure 74 – Output Load Transient, 100-0% Load.
V_{IN} = 1000 VDC, I_{OUT} = 1.458 A to 0 A.
$V_{OUT(MAX)}$ = 24.28 V, $V_{OUT(MIN)}$= 23.85 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: I_{OUT}, 1 A, 50 ms / div.

9.10 *FWD Waveforms, Steady-State*

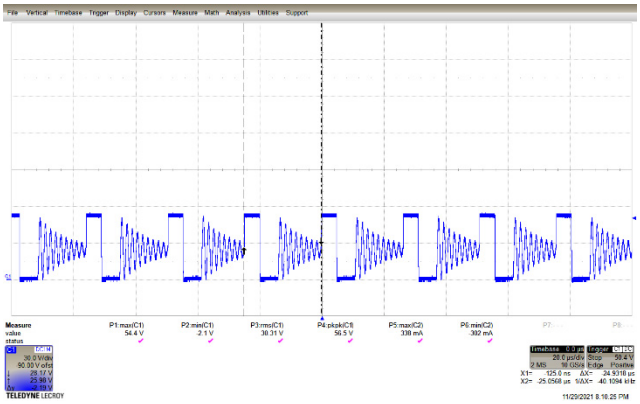


Figure 75 – FWD Voltage During Steady-State.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 54.4 V.
CH1: V_{FWD}, 30 V, 20 µs / div.

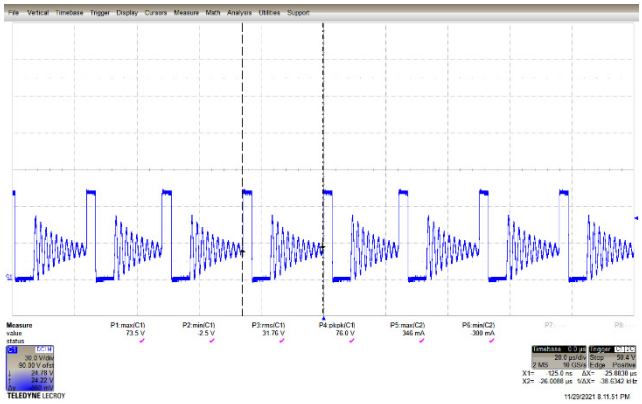


Figure 76 – FWD Voltage During Steady-State.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 73.5 V.
CH1: V_{FWD}, 30 V, 20 µs / div.

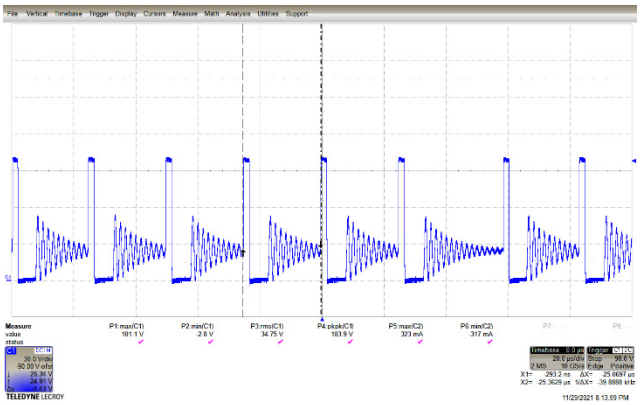


Figure 77 – FWD Voltage During Steady-State.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 101.1 V.
CH1: V_{FWD}, 30 V, 20 µs / div

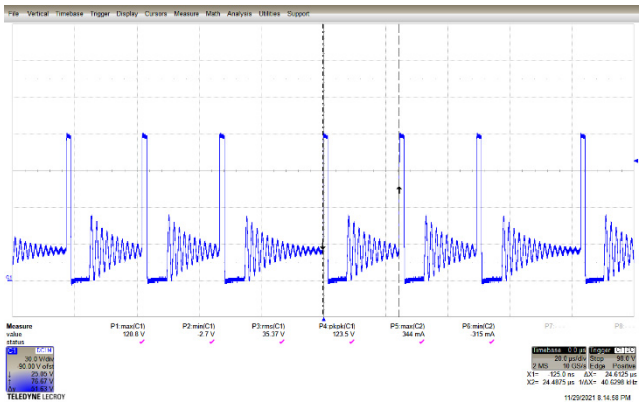


Figure 78 – FWD Voltage During Steady-State.
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 120.8 V.
CH1: V_{FWD}, 30 V, 20 µs / div

9.11 *FWD Waveforms, Start-up*

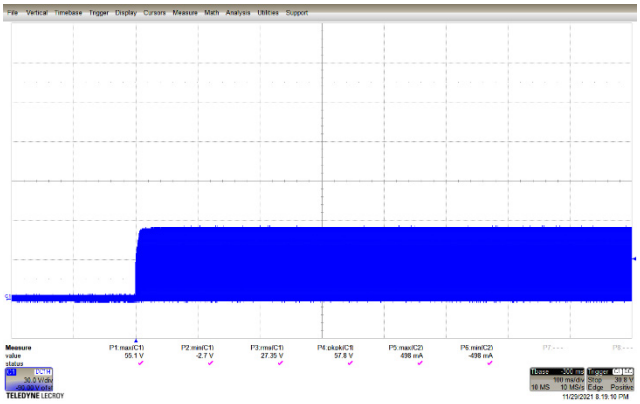


Figure 79 – FWD Voltage During Start-up.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 55.1 V.
CH1: V_{FWD}, 30 V, 100 ms / div.

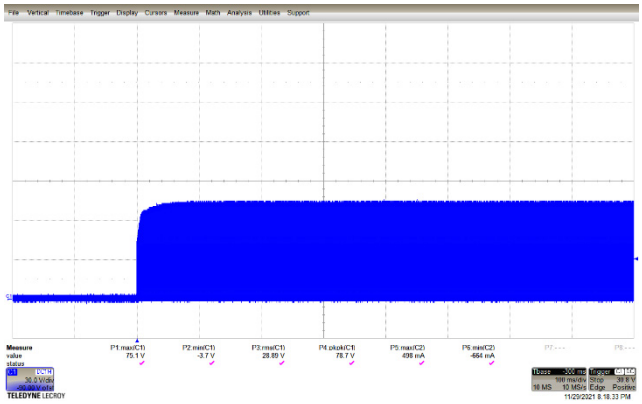


Figure 80 – FWD Voltage During Start-up.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 75.1 V.
CH1: V_{FWD}, 20 V, 50 ms / div.

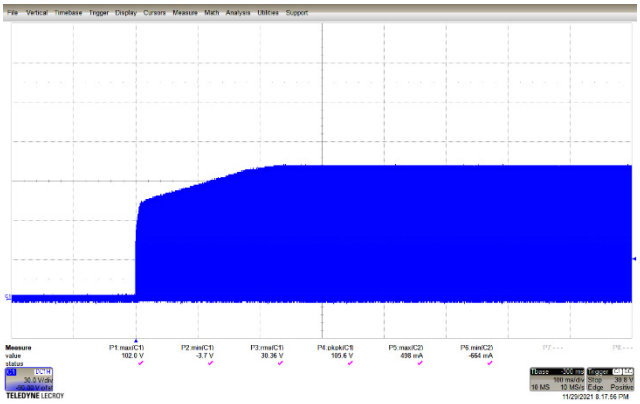


Figure 81 – FWD Voltage During Start-up.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 102 V.
CH1: V_{FWD}, 30 V, 100 ms / div

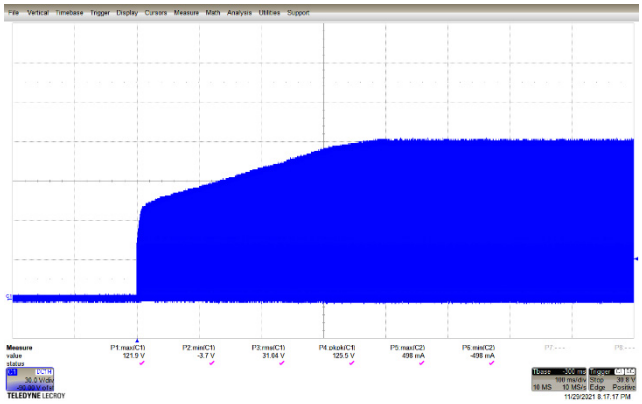


Figure 82 – FWD Voltage During Start-up.
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 121.9 V.
CH1: V_{FWD}, 30 V, 100 ms / div

9.12 *FWD Waveforms, Output Shorted*

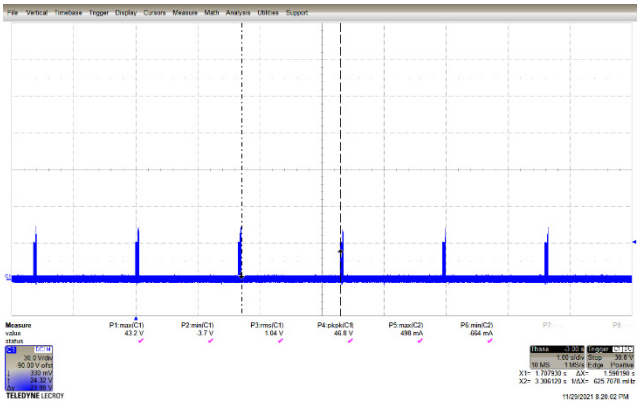


Figure 83 – FWD Voltage During Output Short.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 43.2 V.
CH1: V_{FWD}, 20 V, 1 s / div.

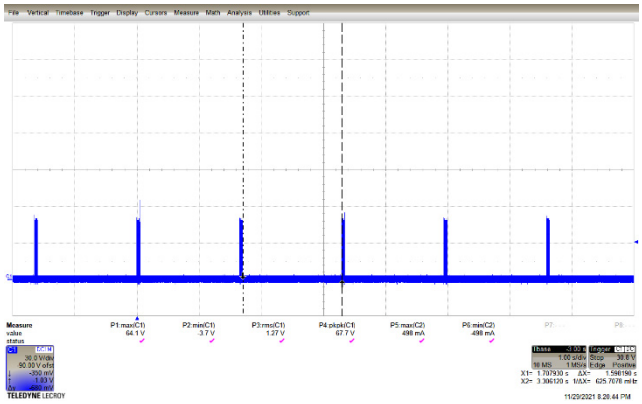


Figure 84 – FWD Voltage During Output Short.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 64.1 V.
CH1: V_{FWD}, 20 V, 1 s / div.

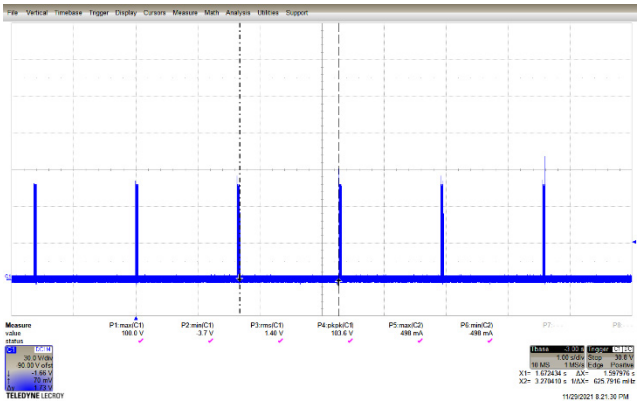


Figure 85 – FWD Voltage During Output Short.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 100 V.
CH1: V_{FWD}, 20 V, 1 s / div.

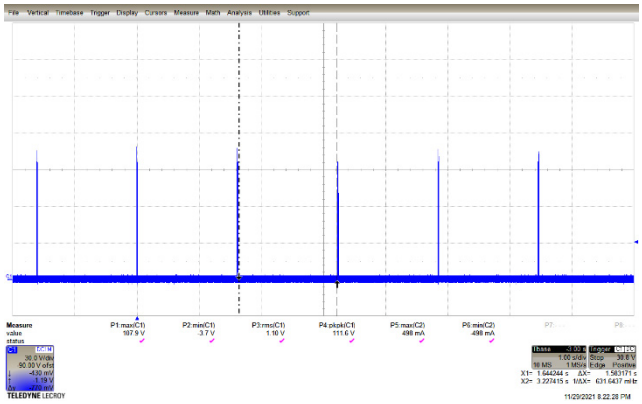


Figure 86 – FWD Voltage During Output Short
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 107.9 V.
CH1: V_{FWD}, 20 V, 1 s / div.

10 Thermal Performance

All measurements have been done at room ambient temperature after 1 hour of continuous operation.

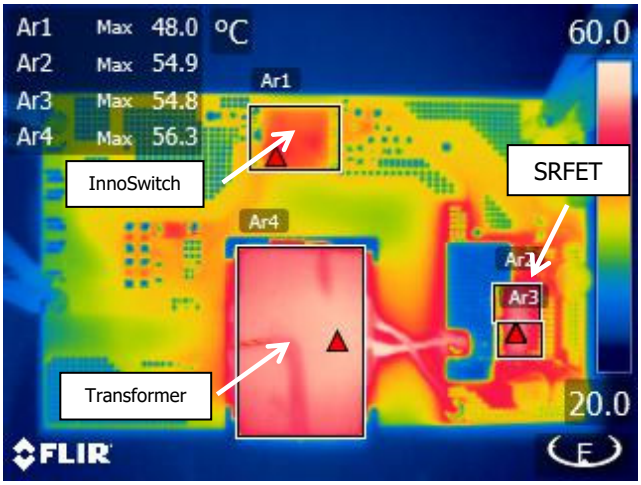


Figure 87 – 300 VDC 1.458 A Full Load.
Temperature of INN3647C: 48.0 ºC.
Temperature of SR FET1 (Q2): 54.9 ºC.
Temperature of SR FET2 (Q3): 54.8 ºC.
Temperature of Transformer: 56.3 ºC.
Ambient Temperature: 25.3 ºC.

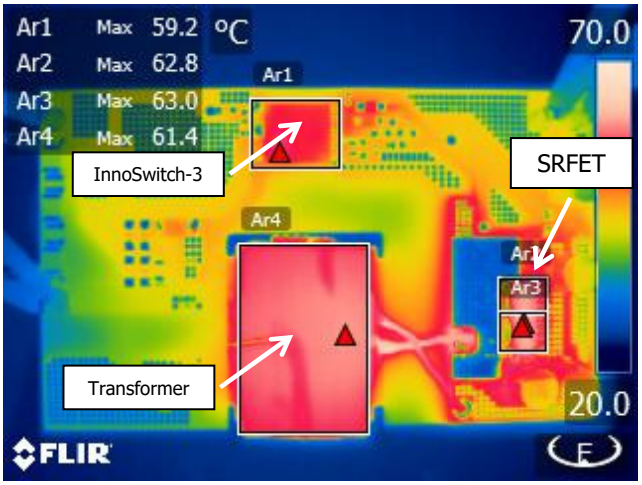


Figure 88 – 800 VDC 1.458 A Full Load.
Temperature of INN3647C: 59.2 ºC.
Temperature of SR FET1 (Q2): 62.8 ºC.
Temperature of SR FET2 (Q3): 63.0 ºC.
Temperature of Transformer: 61.4 ºC.
Ambient Temperature: 26.2 ºC.

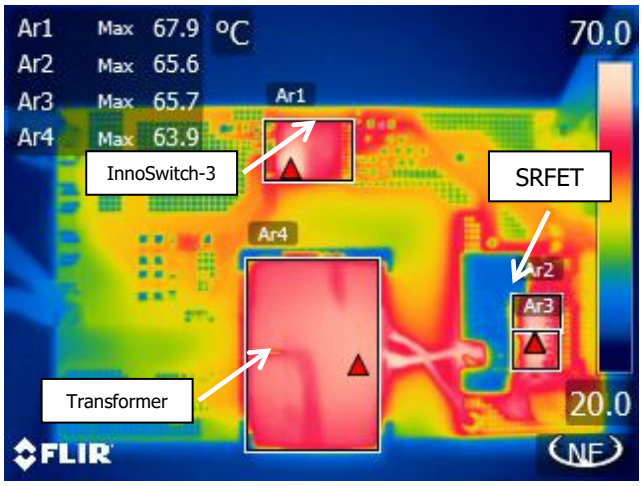


Figure 89 – 800 VDC 1.458 A Full Load.
Temperature of INN3647C: 67.9 ºC.
Temperature of SR FET1 (Q2): 65.6 ºC.
Temperature of SR FET2 (Q3): 65.7 ºC.
Temperature of Transformer: 63.9 ºC.
Ambient Temperature: 25.2 ºC.

10.1 *Temperature vs. Output Power*

Data below is taken with no additional thermal mitigation.

Available output power at elevated ambient can be increased by providing a thermal path from the PCB area connected to the SOURCE pin of the InnoSwitch3-EP to a surface that is lower in temperature. This is typically the outer wall of the inverter or internally above the water channel cooling the power modules. A very simple approach is a compliant thermal pad (e.g. TGP 1500 from Berquist) placed between the PCB and bottom or top surface of the enclosure.

In the design of the cast enclosure features may be added at no cost to provide a location to place the pad for manufacturing simplicity and reduce the thickness of pad needed to reduce cost of pad needed.

300 VDC								
P_{IN} (W)	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**Efficiency (%)**	**INN3647C (ºC)**	**AMB (ºC)**	**INN3647C Trise (ºC)**	**Projected Max AMB Operating Temperature (125 ºC – Trise)**
6.98	24.17	0.26	6.16	88.3	31.2	22.2	9	116
13.17	24.20	0.49	11.93	90.6	36.5	23.5	13	112
19.40	24.22	0.73	17.71	91.3	39.4	23.9	15.5	109.5
25.39	23.99	0.98	23.39	92.1	41.8	23.9	17.9	107.1
31.78	24.14	1.21	29.29	92.2	43.2	23.4	19.8	105.2
38.08	24.18	1.46	35.17	92.4	48.0	25.3	22.7	102.3

400 VDC								
P_{IN} (W)	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**Efficiency (%)**	**INN3647C (ºC)**	**AMB (ºC)**	**INN3647C Trise (ºC)**	**Projected Max AMB Operating Temperature (125 ºC – Trise)**
7.08	24.18	0.26	6.16	87.1	33.2	22.3	10.9	114.1
13.28	24.20	0.49	11.93	89.9	36.4	22.3	14.1	110.9
19.51	24.23	0.73	17.72	90.8	41.3	24.3	17	108
25.77	24.25	0.98	23.65	91.8	44.2	24.3	19.9	105.1
31.71	24.02	1.21	29.14	91.9	46.3	24.5	21.8	103.2
38.16	24.16	1.46	35.16	92.1	47.9	24.3	23.6	101.4

500 VDC								
P_{IN} (W)	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**Efficiency (%)**	**INN3647C (ºC)**	**AMB (ºC)**	**INN3647C Trise (ºC)**	**Projected Max AMB Operating Temperature (125 ºC – Trise)**
7.17	24.3	0.26	6.20	86.4	36.5	24.0	12.5	112.5
13.41	24.2	0.49	11.93	89.0	39.2	24.4	14.8	110.2
19.64	24.22	0.73	17.71	90.2	42.1	24.0	18.1	106.9
25.91	24.26	0.98	23.66	91.3	44.9	24.5	20.4	104.6
31.79	23.96	1.21	29.07	91.4	47.4	24.8	22.6	102.4
38.28	24.14	1.46	35.13	91.8	48.9	24.6	24.3	100.7

600 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3647C (ºC)	AMB (ºC)	INN3647C Trise (ºC)	Projected Max AMB Operating Temperature (125 ºC – Trise)
7.30	24.18	0.26	6.17	84.5	37.5	23.8	13.7	111.3
13.55	24.21	0.49	11.94	88.1	40.8	23.9	16.9	108.1
19.81	24.23	0.73	17.72	89.5	43.7	24.1	19.6	105.4
26.09	24.26	0.98	23.66	90.7	46.8	24.6	22.2	102.8
32.05	24.01	1.21	29.13	90.9	48.5	24.6	23.9	101.1
38.42	24.10	1.46	35.07	91.3	50.7	24.9	25.8	99.2

700 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3647C (ºC)	AMB (ºC)	INN3647C Trise (ºC)	Projected Max AMB Operating Temperature (125 ºC – Trise)
7.43	24.18	0.26	6.17	83.0	38.9	23.9	15.0	110.0
13.74	24.21	0.49	11.94	86.9	41.8	24.0	17.8	107.2
20.00	24.24	0.73	17.73	88.6	46.0	24.4	21.6	103.4
26.31	24.26	0.98	23.65	89.9	49.3	24.9	24.4	100.6
32.57	24.23	1.21	29.39	90.2	52.4	24.9	27.5	97.5
38.60	24.07	1.46	35.03	90.8	54.7	24.8	29.9	95.1

800 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3647C (ºC)	AMB (ºC)	INN3647C Trise (ºC)	Projected Max AMB Operating Temperature (125 ºC – Trise)
7.58	24.18	0.26	6.17	81.4	39.8	23.4	16.4	108.6
13.92	24.21	0.49	11.94	85.8	44.8	23.6	21.2	103.8
20.20	24.24	0.73	17.73	87.7	48.1	23.8	24.3	100.7
26.52	24.27	0.98	23.66	89.2	51.5	24.0	27.5	97.5
32.83	24.29	1.21	29.46	89.7	53.8	24.2	29.6	95.4
38.77	24.01	1.46	34.94	90.1	59.2	26.2	33.0	92.0

900 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3647C (ºC)	AMB (ºC)	INN3647C Trise (ºC)	Projected Max AMB Operating Temperature (125 ºC – Trise)
7.33	24.18	0.26	6.17	84.1	43.6	25.2	18.4	106.6
14.13	24.21	0.49	11.94	84.5	48.7	25.4	23.3	101.7
20.44	24.24	0.73	17.73	86.7	52.8	25.6	27.2	97.8
26.79	24.26	0.98	23.65	88.3	56.3	25.8	30.5	94.5
33.15	24.29	1.21	29.47	88.9	60.0	25.9	34.1	90.9
39.02	23.96	1.46	34.87	89.4	63.3	25.9	37.4	87.6

1000 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3647C (ºC)	AMB (ºC)	INN3647C Trise (ºC)	Projected Max AMB Operating Temperature (125 ºC – Trise)
7.94	24.19	0.26	6.17	77.7	45.1	24.9	20.2	104.8
14.37	24.21	0.49	11.94	83.1	51.1	25.4	25.7	99.3
20.71	24.24	0.73	17.72	85.6	56.6	25.7	30.9	94.1
27.05	24.26	0.98	23.66	87.5	60.5	26.0	34.5	90.5
33.46	24.29	1.21	29.47	88.1	64.7	26.6	38.1	86.9
39.36	23.95	1.46	34.85	88.5	68.2	25.3	42.9	82.1

10.2 *Maximum Output Power vs. Ambient Temperature*

(Based on 125 ºC junction temperature of INN3647C)
Data below is taken with no additional thermal mitigation

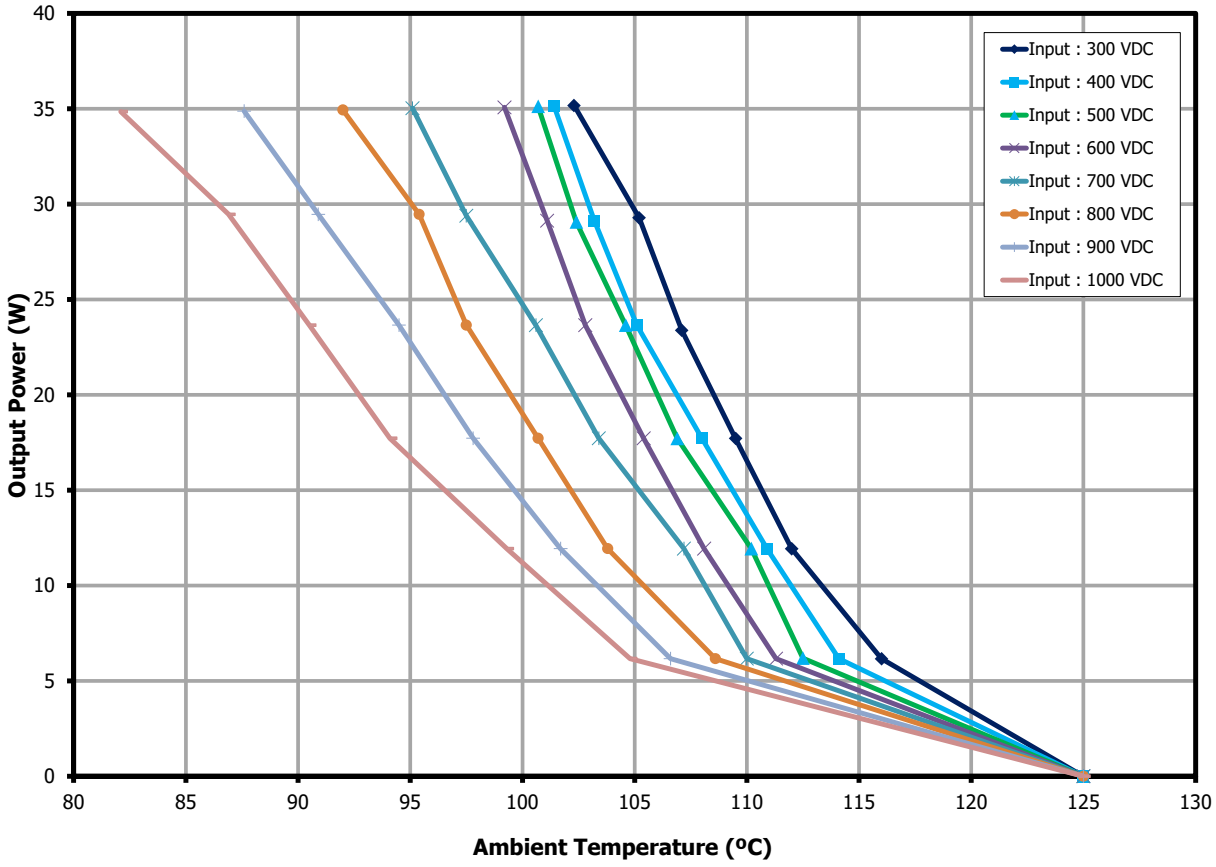


Figure 90 – Maximum Output Power vs. Ambient Temperature.

11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
01-Feb-22	JMR/MA	1.0	Initial Release	Mktg & Apps
23-Jun-22	KM	1.1	Updated Manufacturing BOM P/Ns for D3, R7 and R8.	Mktg & Apps
14-Sep-22	KM	1.2	Added Supplier for T1.	Mktg & Apps

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