Application Note AN-98
LinkSwitch-TNZ Family

Buck and Buck-Boost Design Guide

Introduction

The LinkSwitch™-TNZ family of ICs combine power conversion with lossless generation of an AC zero crossing signal. This signal is typically used for system clock and timing functions. Designs using the highly integrated LinkSwitch-TNZ ICs reduce component count more than 40% compared to discrete solutions. As well as enabling efficiency greater than 80% in low power flyback designs, the very low consumption at light load enabled by ON/OFF control allows for more functions (display, wireless connectivity, sensors etc.) to be active during system standby. The LinkSwitch-TNZ family is highly flexible, supporting buck, buck-boost and flyback converter topologies.

Each device incorporates a 725 V power MOSFET, driver, oscillator, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit and protection into a monolithic IC.

LinkSwitch-TNZ ICs consume less than 100 μA in no-load operation resulting in power supply designs that can meet no-load and standby regulations worldwide. MOSFET current limit thresholds can be selected through the BYPASS pin capacitor value. Choosing the high current limit provides maximum continuous output current while selecting the low current limit permits the use of small surface mount inductors. The comprehensive suite of protection features means that LinkSwitch-TNZ-based power supplies protect both the power supply itself and the system against input and output overvoltage and undervoltage faults. The LinkSwitch-TNZ ICs also protect against device over-temperature faults, lost regulation, and power supply output overload or short-circuit faults.

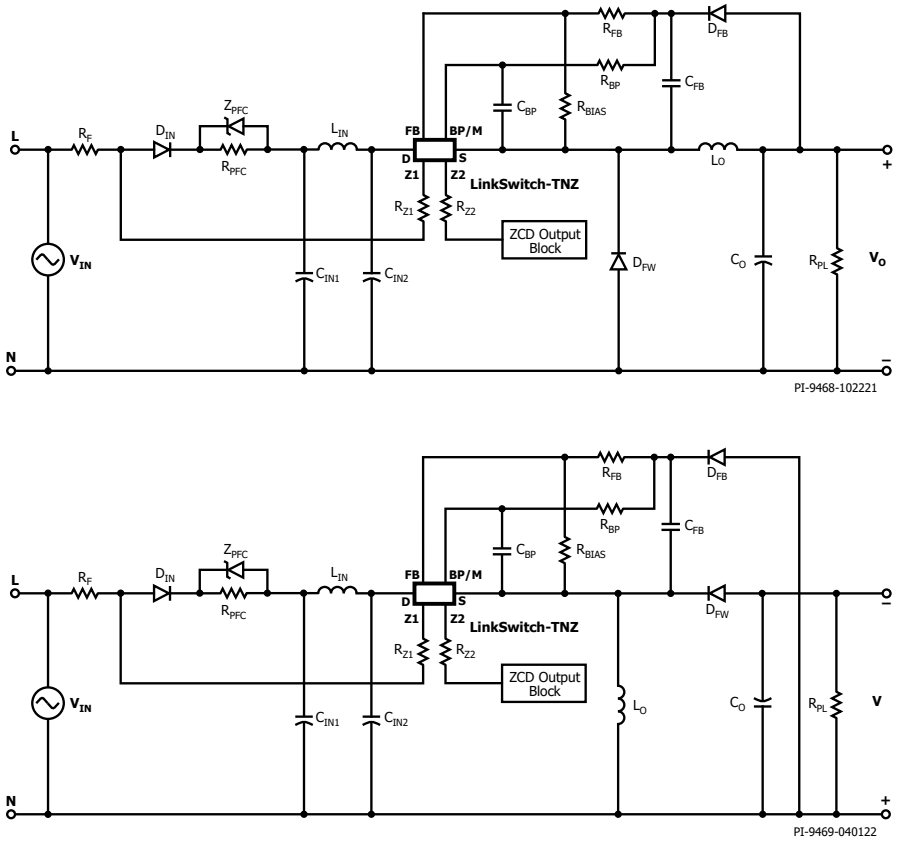


Figure 1. Basic Configuration Using LinkSwitch-TNZ in a Buck Converter, 1(a) and Buck-Boost Converter, 1(b).

Scope

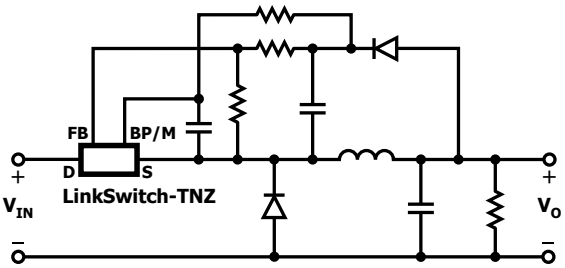
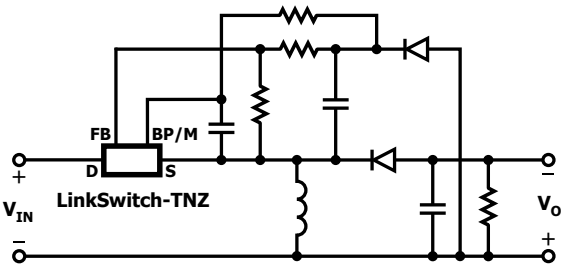
This application note provides information for designing a non-isolated power supply using the LinkSwitch-TNZ family of devices. This document describes the design procedure for buck and buck-boost converters. The objective of this document is to provide power supply engineers with guidelines in order to enable them to quickly build efficient buck or buck-boost converter based power supplies using low-cost off-the- shelf inductors. Complete design equations are provided for the selection of the converter's key components. Since the power MOSFET and controller are integrated into a single IC, the design process is greatly simplified, the circuit configuration has few parts and no transformer is required. Therefore a quick start section is provided that allows easy selection of components for typical output voltages and currents. To simplify the task this application note refers directly to the PIXls design spreadsheet that is part of the PI Expert™ design software suite (go to power.com for a free download of the design software or to use the web version of PI Expert). The basic schematic for LinkSwitch-TNZ power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications throughout this application note.

In addition to this application note, the reader may also find the LinkSwitch-TNZ Reference Design Kit (RDK) containing an engineering prototype board and engineering report useful as an example of a working power supply. Further details on downloading PI Expert, obtaining a RDK and updates to this document can be found at www.power.com.

Quick Start

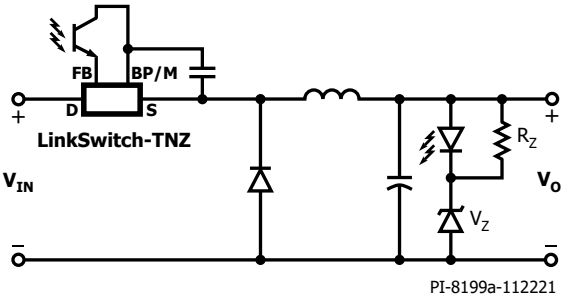
Readers familiar with power supply design and wanting to start immediately can use the following information to select the components for a new design, using Figure 1 and Tables 1 and 2 as references.

1. For AC input designs select the input stage (Table 9).
2. Select the topology (Tables 1 and 2). If better than ±5% output regulation is required, then use of optocoupler feedback and not with suitable reference such as a TL431 or a precision Zener is required.
3. Select the LinkSwitch-TNZ device, L_O, R_{FB} or V_Z, R_{BIAS}, C_{FB}, R_Z and the reverse recovery time for D_{FW} (Table 4: Buck, Table 5: Buck-Boost).
4. Select freewheeling diode to meet t_{RR} determined in Step 3 (table 3).
5. For direct feedback designs, if the minimum load <3 mA then calculate $R_{PL} = V_O/3$ mA.
6. Select C_O as 100 µF, 1.25 × V_O, low ESR type.
7. Construct prototype and verify design.

Topology	Basic Circuit Schematic	Key Features
High-Side Buck – Direct Feedback	 PI-8199a-101121	1. Output referenced to input. 2. Positive output (V_O) with respect to -V_{IN}. 3. Step down: $V_O < V_{IN}$. 4. Direct feedback (±5% typ.). 5. Requires an output load to maintain regulation (Note 2).
High-Side Buck-Boost – Direct Feedback	 PI-8200a-040122	1. Output referenced to input. 2. Negative output (V_O) with respect to -V_{IN}. 3. Step up/down: $V_O < V_{IN}$ or $V_O > V_{IN}$. 4. Direct feedback (±5% typ.). 5. Fail-safe – output is not subjected to input voltage if the internal MOSFET fails. 6. Requires an output load to maintain regulation (Note 2).

Notes:
1. Directly sensed feedback typically achieves overall regulation tolerance of ±5% with 3 mA pre-load for 12 V design.
2. To ensure output regulation, a pre-load may be required to maintain a minimum load current of 3 mA (buck and buck-boost only).
3. Boost topology (step-up) is also possible but not shown.

Table 1. LinkSwitch-TNZ Circuit Configurations using Directly Sensed Feedback.

Topology	Basic Circuit Schematic	Key Features
High-Side Buck – Optocoupler Feedback		1. Output referenced to input. 2. Positive output (V_O) with respect to -V_{IN}. 3. Step down: $V_O < V_{IN}$. 4. Direct feedback (±5% typ.). 5. Requires an output load to maintain regulation (Note 2).

Notes:
1. Regulation of optocoupler feedback only limited by accuracy of reference (Zener or IC).
2. Optocoupler does not need to be safety approved.
3. The current for the reference voltage acts as a pre-load. The value of RZ is determined by Zener test current or reference IC bias current, typically 470 Ω to 2 kΩ, 1/8 W, 5%.
4. Boost topology (step-up) is also possible but not shown.
5. Optocoupler feedback provides lowest no-load consumption.

Table 2. LinkSwitch-TNZ Circuit Configurations using Optocoupler Feedback.

Part Number	V_{RRM} (V)	I_F (A)	t_{RR} (ns)	Package	Manufacturer
MUR160	600	1	50	Leaded	Vishay
UF4005	600	1	75	Leaded	Vishay
BYV26C	600	1	30	Leaded	Vishay/Philips
FE1A	600	1	35	Leaded	Vishay
STTA10 6	600	1	20	Leaded	ST Microelectronics
STTA10 6U	600	1	20	SMD	ST Microelectronics
US1J	600	1	75	SMD	Vishay
SFM18PL	600	1	35	SMD	MCC

Table 3. List of Ultrafast Diodes Suitable for use as the Freewheeling Diode.

V_{OUT} (V)	$I_{OUT(MAX)}$ (mA)	Inductor		Suggested LinkSwitch-TNZ Device	Mode	Diode t_{RR}	R_{FB}* (kΩ)	V_Z (V)
		Typical Inductance (µH)	I_{RMS} (mA)					
5	≤63 80	2000 2400	88 96	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	3.48	3.9
	120 160	910 1300	171 194	LNK33x4	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 225	620 1300	315 380	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	470 820	564 642	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
12	≤63 80	2000 2700	87 95	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	11.8	11
	85 120 160	910 1100 1800	143 166 189	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	175 225	620 1500	315 378	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	470 910	562 634	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
15	≤63 80	2400 3300	85 93	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	15.4	13
	70 120 160	910 1300 2200	130 163 186	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	175 225	680 1800	311 376	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	470 1000	561 628	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
24	≤63 80	3900 5100	81 90	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	25.5	22
	50 120 160	910 2000 3300	109 156 183	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	175 225	1100 2700	296 373	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 1600	524 609	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		

Other standard components
R_{BIAS}: 2.49 kΩ, 1%, 1/8 W
C_{FB}: 10 µF, 1.25 × V_O
D_{FB}: 1N4005GP
R_Z: 470 Ω to 2 kΩ, 1/8 W, 5%

Table 4. Components Quick Select for Buck Converters. *Select nearest standard or combination of standard values.

V_{OUT} (V)	$I_{OUT(MAX)}$ (mA)	Inductor		Suggested LinkSwitch-TNZ Device	Mode	Diode t_{RR}	R_{FB}* (kΩ)	V_Z (V)
		Typical Inductance (µH)	I_{RMS} (mA)					
5	≤60 80	2000 2700	88 96	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	3.48	3.9
	110 170	910 1300	165 196	LNK33x4	MDCM CCM	≤ 75 ns ≤ 35 ns		
	215 360	620 1500	311 390	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	340 575	470 910	546 642	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
12	≤55 80	2200 3300	82 96	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	11.8	11
	85 105 170	910 1000 2700	146 160 201	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	195 360	620 3300	299 417	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	330 5780	470 1800	543 664	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
15	≤55 80	2200 4300	82 98	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	15.4	13
	70 100 170	910 1100 3600	133 155 204	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	195 335	620 3000	300 407	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	315 550	470 1800	533 655	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		
24	≤50 80	3300 9100	77 105	LNK33x2	MDCM CCM	≤ 75 ns ≤ 35 ns	25.5	22
	50 90 165	910 1600 6800	114 146 214	LNK33x4	MDCM MDCM CCM	≤ 75 ns ≤ 75 ns ≤ 35 ns		
	170 300	910 3600	275 398	LNK33x6	MDCM CCM	≤ 75 ns ≤ 35 ns		
	825 510	560 3000	496 660	LNK33x7	MDCM CCM	≤ 75 ns ≤ 35 ns		

Other Standard Components:
R_{BIAS}: 2.49 kΩ, 1%, 1/8 W
C_{FB}: 10 µF, 1.25 × V_O
D_{FB}: 1N4005GP
R_Z: 470 Ω to 2 kΩ, 1/8 W, 5%

Table 5. Components Quick Select for Buck-Boost Converters. *Select nearest standard or combination of standard values. The inductor values indicated in the table above are conservative estimates. In some designs it may be possible to reduce the inductance value further based on evaluation.

LinkSwitch-TNZ Circuit Design

LinkSwitch-TNZ Operation

The basic circuit configuration for a buck converter using a LinkSwitch-TNZ IC is shown in Figure 1(a). To regulate the output, an ON/OFF control scheme is used as illustrated in Table 6. As the decision to switch is made on a cycle-by-cycle basis, the resultant power supply has extremely good transient response and removes the need for control loop compensation components. If the output requests switching cycles (IFB < 49 μA) continuously for longer then 50 ms then switching is inhabited and the circuit enters auto-restart mode. During auto-restart the duty cycle is reduced to prevent overheating of the power supply or damage to the board or load. If no feedback is received for 50 ms, then the supply enters auto-restart and switching is inhibited for a period of time to limit power dissipation.

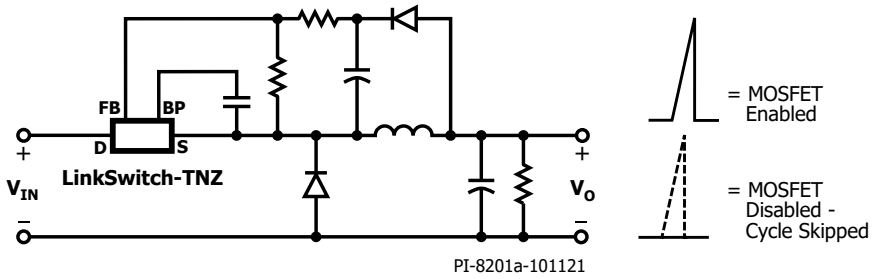
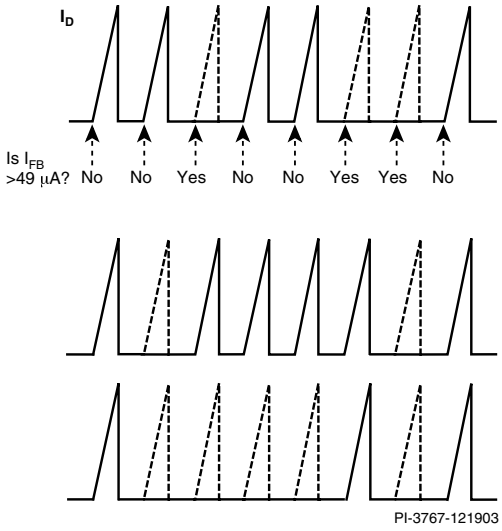
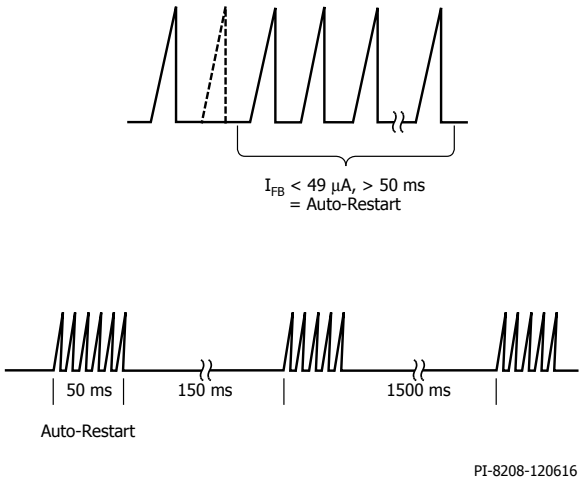
Reference Schematic And Key		
Normal Operation		At the beginning of each cycle, the FEEDBACK (FB) pin is sampled. If I_{FB} < 49 μA then next cycle occurs If I_{FB} > 49 μA then next switching cycle is skipped High load – few cycles skipped Low load – many cycles skipped
Auto-Restart		If no feedback (I_{FB} < 49 μA) for > $t_{AR(ON)}$ (50 ms), then output switching is disabled equal to the auto-restart off-time. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

Table 6. LinkSwitch-TNZ Operation.

To allow direct sensing of the output voltage without the need for a reference (Zener diode or reference IC), the FEEDBACK pin voltage is tightly toleranced over the entire operating temperature range. For example, this allows a 12 V design with an overall output tolerance of ±5%. For higher performance, an optocoupler can be used with a reference as shown in Table 2. Since the optocoupler just provides level shifting, it does not need to be safety rated or approved. The use of an optocoupler also allows flexibility in the location of the device, for example it allows a buck converter configuration with the LinkSwitch-TNZ IC in the low-side return rail, reducing EMI as the SOURCE pins and connected components are no longer part of the switching node.

Selecting the Topology

If possible, use the buck topology. The buck topology maximizes the available output power from a given LinkSwitch-TNZ IC and inductor value. Also, the voltage stress on the power switch and freewheeling diode and the average current through the output inductor are slightly lower in the buck topology as compared to the buck-boost topology.

Selecting the Operating Mode – MDCM and CCM Operation

At the start of a design, select between mostly discontinuous conduction mode (MDCM) and continuous conduction mode (CCM) as this decides the selection of the LinkSwitch-TNZ device, freewheeling diode and inductor. For maximum output current select CCM, for all other output components MDCM is recommended. Overall, select the operating mode and components to give the lowest overall solution cost. Table 7 summarizes the trade-offs between the two operating modes.

Additional differences between CCM and MDCM include better transient response for DCM and lower output ripple (for same capacitor ESR) for CCM. However these differences, at the low output currents of LinkSwitch-TNZ applications, are normally not significant.

The conduction mode CCM or MDCM of a buck or buck-boost converter primarily depends on input voltage, output voltage, output current and device current limit. The input voltage, output voltage and output current are fixed design parameters. The current limit for the LinkSwitch-TNZ is the design parameter that can be used to set the conduction mode, therefore the LinkSwitch-TNZ current limit is the only design parameter that sets the conduction mode.

The phrase "mostly discontinuous" is used with ON/OFF control, because while a few switching cycles may exhibit continuous inductor current flow, the majority of the switching cycles will be discontinuous. A design can be made fully discontinuous but that will limit the available output current, making the design less cost effective.

Comparison of CCM and MDCM Operating Modes

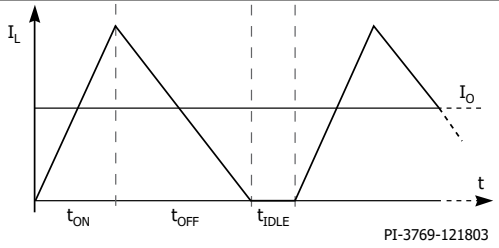
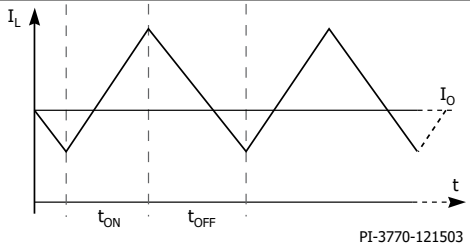
Operating Mode	MDCM	CCM
Operating Description	 Inductor current falls to zero during t_{OFF}, borderline between MDCM and CCM when t_{IDLE} = 0.	 Current flows continuously in the inductor for the entire duration of a switching cycle.
Inductor	**Lower Cost** Lower value, smaller size.	**Higher Cost** Higher value, larger size.
Freewheeling Diode	**Lower Cost** 75 ns ultrafast reverse recovery type (≤35 ns for ambient >70 °C).	**Higher Cost** 35 ns ultrafast recovery type required.
LinkSwitch-TNZ	**Potentially Higher IC Cost** May require larger device to deliver required output current – depends on required output current.	**Potentially Lowest IC Cost** May allow smaller device to deliver required output current: depends on required output current.
Efficiency	**Higher Efficiency** Lower switching losses.	**Lower Efficiency** Higher switching losses.
Overall	Typically lower cost but reduced output power.	Typically higher cost but increased output power.

Table 7. Comparison of Mostly Discontinuous Conduction (MDCM) and Continuous Conduction (CCM) Modes of Operation.

ON/OFF Operation with Current Limit State Machine

LNK33x7 has a special operating mode in which the current limit has multiple states depending on the output load. It has an advantage of generating less audible noise across varying load.

The internal clock of the LNK33x7 runs all the time. At the beginning of each clock cycle, it samples the FEEDBACK pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine reduces the current limit to reduced values.

At near maximum load, LNK33x7 will conduct during nearly all of its clock cycles (Figure 2). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 3). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 4). At very light loads, the current limit will be needed to reduced even further (Figure 5). Only a small percentage of cycles will be needed to occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides accurate regulation and excellent transient response.

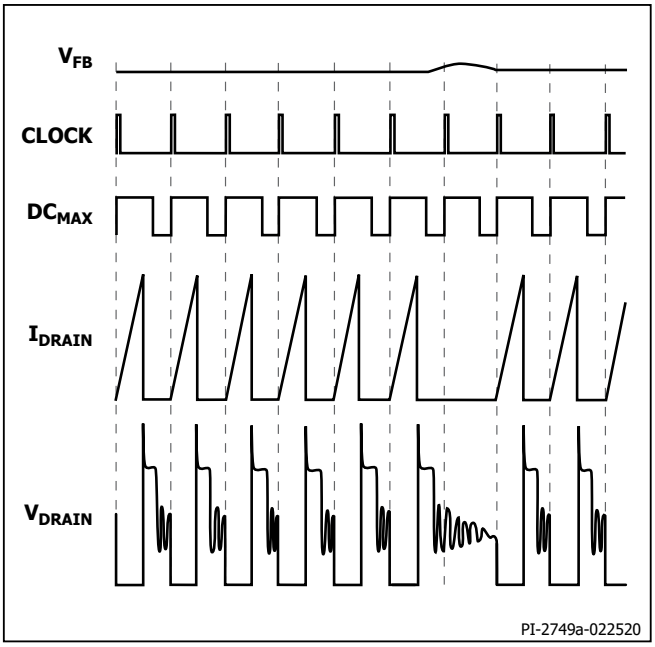


Figure 2. Operation at Near Maximum Loading (Flyback).

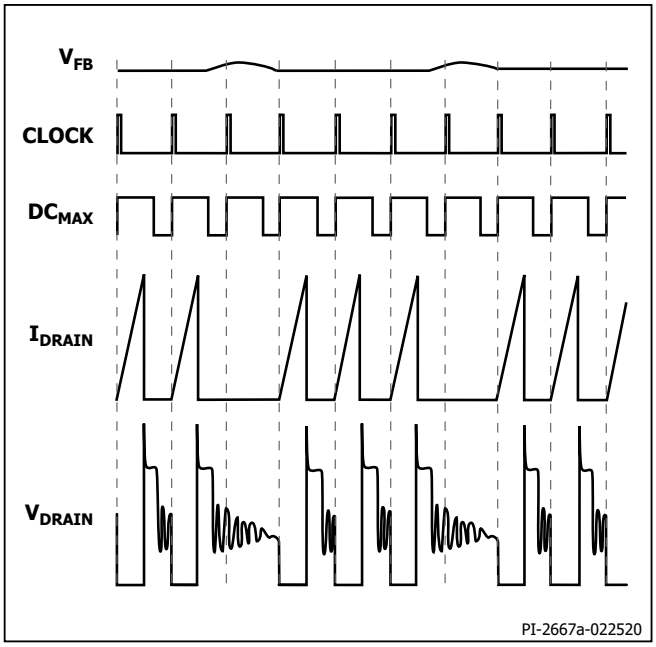


Figure 3. Operation at Moderately Heavy Loading (Flyback).

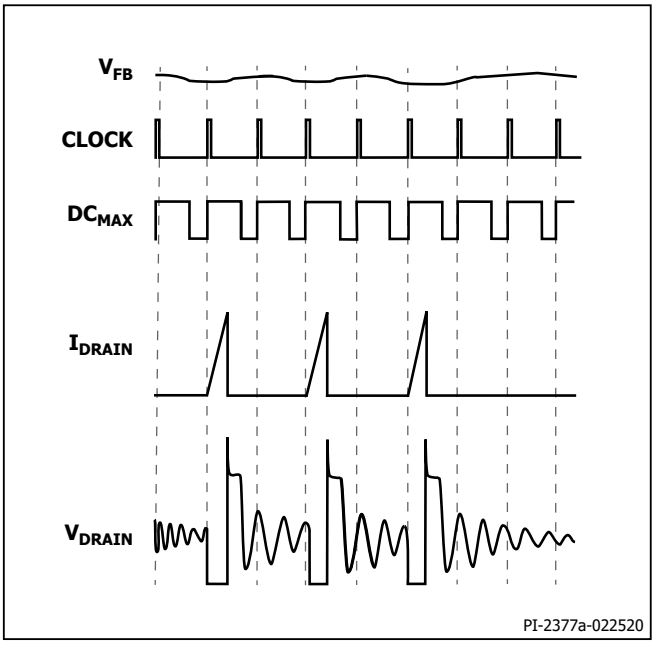


Figure 4. Operation at Medium Loading (Flyback).

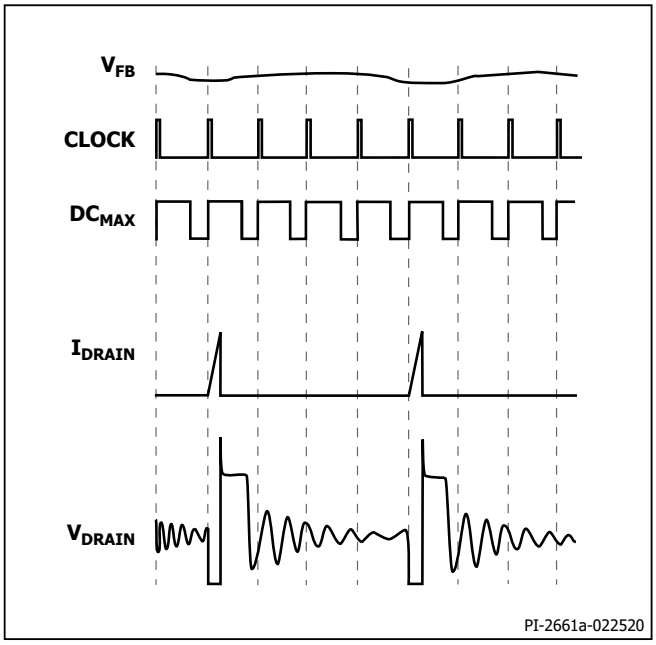


Figure 5. Operation at Very Light Load (Flyback).

Step-by-Step Design Procedure

Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, η, C_{IN}

1	ACDC_LinkSwitchTNZ_Buck_052621; Rev.1.0; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch™-TNZ Buck
2	ENTER APPLICATION VARIABLES					Design Title
3	LINE VOLTAGE RANGE			Universal		AC line voltage range
4	VACMIN			85.00	V	Minimum AC line voltage
5	VACMAX			265.00	V	Maximum AC line voltage
6	fL			60.00	Hz	AC mains frequency
7	LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
8	VOUT	12.00		12.00	V	Output voltage
9	IOUT	0.500		0.500	A	Average output current
10	EFFICIENCY_ESTIMATED			0.80		Efficiency estimate at output terminals
11	EFFICIENCY_CALCULATED			0.78		Calculated efficiency based on real components and operating point
12	POUT			6.00	W	Continuous output power
13	CIN			15.00	uF	Input capacitor
14	VMIN			91.0	V	Valley voltage of the rectified minimum AC line voltage
15	VMAX			374.8	V	Peak voltage of the maximum AC line voltage
16	INPUT STAGE RESISTANCE			10	Ohms	Input stage resistance in ohms (includes thermistor, filtering components, etc)
17	PLOSS_INPUTSTAGE			0.068	W	Maximum input stage loss

Table 8. Application Variable Section of LinkSwitch-TNZ Design Spreadsheet.

Input Voltage
Determine the input voltage range from Table 9.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 9. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, fL
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. For most applications this gives adequate overall design margin. For absolute worst-case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz).

Nominal Output Voltage, V_{OUT} (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally the main output is the output from which feedback is derived.

Output Current, I_{OUT} (A)
Enter the output current of the power supply. If the power supply is a multiple output power supply, enter the sum total equivalent current of all the outputs, the sum total power divides the main output voltage.

In multiple output designs, the output power of the main output (typically the output from which feedback is taken) should be increased such that the maximum continuous output power as applicable, matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 0.7 for a 12 V output, 0.55 for a 5 V output if no better reference data is available, typical for a design where the majority of the output power is drawn from an output voltage of 12 V or greater. Once a prototype has been constructed then measured efficiency should be entered.

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 10 for guidance. The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} > 70 V.

	Total Input Capacitance per Watt Output Power μF/W	
AC Input Voltage (VAC)	Full-Wave Rectification	Half-Wave Rectification
100/115	2	4-5
230	1	1-2
85-265	2	4-5

Table 10. Suggested Total Input Capacitance Values for Different Input Voltage Ranges.

Step 2 – Determine AC Input Stage

The input stage comprises fusible resistor(s), input rectification diodes and line filter network. Flameproof fusible resistors are recommended and depending on the differential line input surge requirements, a wire-wound type may be required. The fusible resistor(s) provides fuse safety, inrush current limiting and differential mode noise attenuation. Table 12 shows the recommended input stage based on output power for a universal input design while Table 10 shows how to adjust the input capacitance for other input voltage ranges.

Step 3 – Determine Minimum and Maximum DC Input Voltages V_{MIN} and V_{MAX} Based on AC Input Voltage

Calculate V_{MAX} as:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX} \quad (1)$$

Assuming that the value of input fusible resistor is small, the voltage drop across it can be ignored.

Derive minimum input voltage V_{MIN}

Half-wave rectifier:

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}{}^2) - \frac{2 \times P_O \left(\frac{1}{f_L} - t_C\right)}{\eta \times C_{IN(TOTAL)}}} \quad (2)$$

Bridge rectifier:

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}{}^2) - \frac{2 \times P_O \left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN(TOTAL)}}} \quad (3)$$

If V_{MIN} is ≤ 70 V then increase value of $C_{IN(TOTAL)}$. T_C is the rectifier diode conduction time.

Step 4 – Select LinkSwitch-TNZ Device Based on Output Current, Current Limit and X Capacitor Discharge

Decide on the operating mode – refer to Table 7.

For MDCM operation, the output current I_O should be less than or equal to half the value of the minimum current limit of the chosen device from the data sheet.

$$I_{LIMIT\_MIN} > 2 \times I_O \quad (4)$$

For CCM operation, the device should be chosen such that the output current I_O is more than 50% but less than 80% of the minimum current limit I_{LIMIT_MIN}.

$$0.5 \times I_{LIMIT\_MIN} < I_O < 0.8 \times I_{LIMIT\_MIN} \quad (5)$$

Please see the data sheet for LinkSwitch-TNZ current limit values.

A typical LinkSwitch-TNZ part can be programmed to operate in one of the two current limits. The "RED" or reduced current limit enables operation at a reduced current limit and is recommended when the part is to be used at a current level considerably lower than the rated output current. A "STD" or standard current limit will be selected in most applications to optimize on BP capacitor cost.

Use of a 0.1 µF capacitor results in the standard current limit value. Use of a 1 µF capacitor results in the current limit being reduced, allowing design with lower cost surface-mount buck chokes.

21	ENTER LINKSWITCH™-TNZ VARIABLES					
22	OPERATION MODE			MCM		Mostly continuous mode of operation
23	CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
24	XCAP REQUIRED	YES		YES		Select whether an X-capacitor is required or not
25	PACKAGE			SO-8C		Device package
26	DEVICE SERIES	AUTO		LNK3317		Generic LinkSwitch™-TNZ device
27	DEVICE CODE			LNK3317D		Required LinkSwitch™-TNZ device
28	ILIMITMIN			0.725	A	Minimum current limit of the device
29	ILIMITTYP			0.780	A	Typical current limit of the device
30	ILIMITMAX			0.835	A	Maximum current limit of the device

Table 11. LinkSwitch-TNZ Variable Section of LinkSwitch-TNZ Design Spreadsheet.

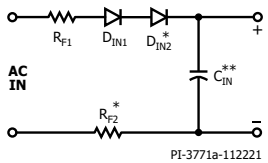
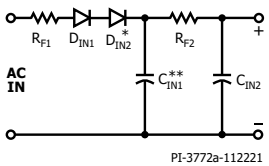
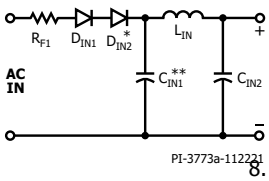
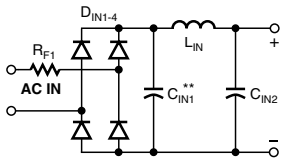
POUT	≤0.25 W	0.25 - 1 W	>1 W	
85 - 265 VAC Input Stage	 PI-3771a-112221	 PI-3772a-112221	 PI-3773a-112221	 PI-3774-121603
	R_{F1}, R_{F2}: 100-470 Ω, 0.5 W, Fusible C_{IN}: ≥2.2 µF, 400 V D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible R_{F2}: 100 Ω, 0.5 W, Flameproof C_{IN1}, C_{IN2}: ≥3.3 µF, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH – 2.2 mH, 0.05 A – 0.3 A C_{IN1}, C_{IN2}: ≥4 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH – 2.2 mH, 0.05 A – 0.3 A C_{IN1}, C_{IN2}: ≥2 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V
Comments	*Optional for improved EMI and line surge performance. Remove for designs requiring no impedance in return rail. **Increase value to meet required differential line surge performance.			

Table 12. Recommended AC Input Stages for Universal Input.

Step 5 – Select the Output Inductor

Choose any standard off-the-shelf inductor that meets the design requirements. As shown in the figure below, a "drum" or "dog bone" "I" core inductor is recommended with a single ferrite element due to its low cost and very low audible noise properties. However, the inductor should be selected as varnished type in order to get low audible noise.

Tables 4 and 5 provide inductor values and RMS current ratings for common output voltages and currents based on the calculations in the design spreadsheet. Select the next nearest higher voltage and/or current above the required output specification. Alternatively, the PIXls spreadsheet tool in the PI Expert software design suite or Appendix B can be used to calculate the exact inductor value (Eq. C13) and RMS current rating (Eq. C29). It is recommended that the value of inductor chosen should be closer to L_{TYP} rather than 1.5 × L_{TYP} due to lower DC resistance and higher RMS rating.

$$L_O < 1.5 \times L_{TYP}$$

For LinkSwitch-TNZ designs, the mode of operation is not dependent on the inductor value. The mode of operation is a function of load current and current limit of the chosen device. The inductor value merely sets the average switching frequency. Table 14 shows a typical standard inductor manufacturer's data sheet. The value of off-the- shelf "drum core / dog bone / I core" inductors will drop up to 20% in value as the current increases. The constant K_{L_TOL} in equation (C14) and the design spreadsheet adjusts for both this drop and the initial inductance value tolerance. For example, if a 680 µH, 360 mA inductor is required, referring to Table 14, the tolerance is 10% and an estimated 9.5% for the reduction in inductance at the operating current (approximately [0.36/0.38] x 10). Therefore the value of K_{L_TOL} = 0.195 (19.5%).

Not all the energy stored in the inductor is delivered to the load due to losses after the LinkSwitch-TNZ device, the inductor (winding resistance and core losses), the freewheeling diode, feedback circuit, output capacitor loss and preload. This will limit the maximum power delivering capability and thus reduce the maximum output current. The minimum inductance must compensate for these losses in order to deliver specified full-load power. To compensate for this, a loss factor K_{LOSS} is used. This has a recommended value of between 50% and 66% of the total supply losses as given by equation 6. For example, a design with an overall efficiency (η) of 0.75 would have a K_{LOSS} value of between 0.875 and 0.833.

$$K_{LOSS} = 1 - \left(\frac{1-\eta}{2}\right) \; to \; 1 - \left(\frac{2(1-\eta)}{3}\right) \quad (6)$$

Figure 6. Example of Drum Core Inductor.

52	BUCK INDUCTOR PARAMETERS					
53	INDUCTANCE_MIN			558	uH	Minimum design inductance required for current delivery
54	INDUCTANCE_TYP	AUTO		620	uH	Typical design inductance required for current delivery
55	INDUCTANCE_MAX			682	uH	Maximum design inductance required for current delivery
56	TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
57	DC RESISTANCE OF INDUCTOR			2.0	ohms	DC resistance of the buck inductor
58	FACTOR_KLOSS			0.50		Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%)
59	IRMS_INDUCTOR			0.621	A	Maximum inductor RMS current
60	PLOSS_INDUCTOR			0.772	W	Maximum inductor losses

Table 13. Buck Inductor Parameters Section of LinkSwitch-TNZ Design Spreadsheet.

● **SBC3 Series**

Model	Inductance L(µH) at 10 kHz)	Rdc (Ω) max.	Rated Current (A) ΔT = 20 °C	Current (Reference Value) (A) ΔT = 40 °C	Current (Reference Value) (A) L change rate -10%
681-361	680±10%	1.62	0.36	0.50	0.38
102-281	1000±10%	2.37	0.28	0.39	0.31
152-251	1500±10%	3.64	0.25	0.35	0.26
222-191	2200±10%	5.62	0.19	0.26	0.21
332-151	3300±10%	7.66	0.15	0.21	0.17

Inductance and Tolerance; Current Rating for 20 °C Rise; Current Rating for 40 °C Rise; Current Rating for Value -10%

PI-3783-121521

Table 14. Example of Standard Inductor Data Sheet.

Step 6 – Select Freewheeling Diode

For MDCM operation at t_{AMB} ≤ 70 °C, select an ultrafast diode with t_{RR} ≤ 75 ns. At t_{AMB} > 70 °C, t_{RR} ≤ 35 ns. For CCM operation, select an ultrafast diode with t_{RR} ≤ 35 ns. Allowing 25% design margin for the freewheeling diode,

$$V_{PIV} = 1.25 \times V_{MAX} \quad (7)$$

The diode must be able to conduct the full load current. Thus:

$$I_F > 1.25 \times I_O \quad (8)$$

Table 3 lists common freewheeling diode choices.

Step 7 – Select Output Capacitor

The output capacitor should be chosen based on the output voltage ripple requirement. Typically the output voltage ripple is dominated by the capacitor ESR and can be estimated as:

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (9)$$

Where V_{RIPPLE} is the maximum output ripple specification and I_{RIPPLE} is the LinkSwitch-TNZ output ripple current (Refer to equations C2 and C3 on appendix B).

The capacitor ESR value should be specified approximately at the switching frequency of 66 kHz. Capacitor values above 100 µF are not recommended for non-resistive load as they can prevent the output voltage from reaching regulation during the 50 ms period prior to auto-restart. If more capacitance is required, then a soft-start capacitor should be added (see Tips for Design section). Select a voltage rating such that V_{RATED} ≥ 1.25 x V_O.

Step 8 – Select the Feedback Resistors

The values of R_{FB} and R_{BIAS} are selected such that at the regulated output voltage, the voltage on the FEEDBACK pin (V_{FB}) is 2 V. This voltage is specified for a FEEDBACK pin current (I_{FB}) of 49 µA.

Let the value of R_{BIAS} = 2.49 kΩ. This biases the feedback network at a current of

$$R_{FB} = \frac{V_O - V_{FB}}{\frac{V_{FB}}{R_{BIAS}} + I_{FB}} = \frac{(V_O - V_{FB}) \times R_{BIAS}}{V_{FB} + (I_{FB} \times R_{BIAS})} \quad (10)$$

Step 9 – Select the Feedback Diode and Capacitor

For the feedback capacitor, use a 10 µF general purpose electrolytic capacitor with a voltage rating of ≥ 1.25 x V_O. For the feedback diode, use a glass-passivated 1N4005GP or DFLR1600-7 device with a voltage rating of ≥ 1.25 x V_{MAX}.

Step 10 – Select the External Biased Resistor for BYPASS Pin

The external BYPASS pin resistor R_{BP} reduces the no-load input power for output voltage > $V_{BP(SHUNT)}$.

To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than I_{S1} on the data sheet. For best full-load efficiency and thermal performance, the current should be slightly higher than I_{S2}.

The BYPASS pin current should not exceed 16 mA ($I_{BP(MAX)}$) at the maximum output voltage (normally when the output voltage is at no-load condition).

Step 11 – Select Preload Resistor

In high-side, direct feedback designs where the minimum load is < 3 mA, a preload resistor is required to maintain output regulation. This ensures sufficient inductor energy to pull the inductor side of the feedback capacitor C_{FB} to input return via D_{FB}. The value of R_{PL} should be selected to give a minimum output load of 3 mA.

In designs with an optocoupler, a Zener diode or reference bias current provides a 1 mA to 2 mA minimum load, preventing "pulse bunching" and increased output ripple at zero load.

Step 12 – Select X Cap Discharge Components

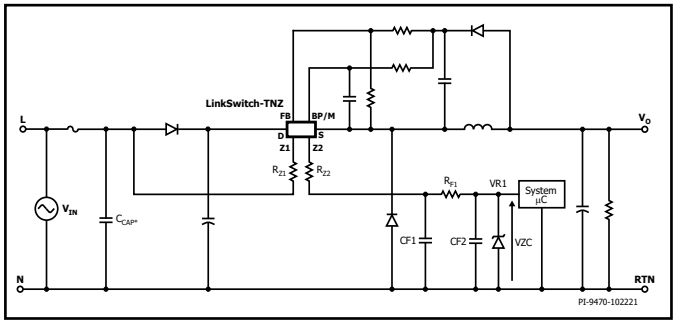
If X cap discharge is required (PIXLS line 24), enter the X cap value on line 88. By default, the software calculates the discharge resistors R_{Z1} and R_{Z2} to ensure that the X cap discharges to 60 V after AC input disconnection in less than 1 second. Change the value of R_{Z1} to change the discharge time.

87	X-CAPACITOR DISCHARGE COMPONENTS					
88	XCAP	220.0		220.0	nF	X-capacitor in the input
89	TOLERANCE_RZ	0.05		5%		Tolerance of the X-capacitor discharge resistors
90	RZ1	1.00		1.00	MOhms	X-capacitor discharge resistor connected from the input line to Z1 pin of LinkSwitch™-TNZ device
91	RZ2			1.00	MOhms	X-capacitor discharge resistor connected from the input neutral to Z2 pin of LinkSwitch™-TNZ device
92	t_XCAP_DISCHARGE			0.846	sec	Actual time (worst-case) to discharge the X-capacitor to 60 V after AC input disconnection

Table 15.F X Capacitor Discharge Section of LinkSwitch-TNZ Design Spreadsheet.

Step 13 – Select ZCD Configuration

High-Side Buck, Half-Wave Rectification, ZCD Using Zener Diode



* Xcap used on LNK-331x parts only

Figure 7. High-side Buck, Half-Wave Rectification, ZCD Using Zener Diode Schematic.

The basic implementation of the ZCD circuit is shown on Figure 7. This configuration is applicable to a high-side buck topology with half-wave input rectification in which the Neutral acts as the ground reference for the power supply.

While the AC input voltage is in positive (L > N) phase, the Z1/Z2 supply current of 22 µA flows through VR1, anode to cathode. The voltage at the microcontroller (µC) input is therefore set to the VR1 Zener voltage (V_{ZC}).

During the next half-cycle (N > L), the Z1/Z2 supply current flows through VR1 in the opposite direction, cathode to anode. The µC zero cross input voltage is clamped to one diode drop below ground (-VF of VR1).

In non-X capacitor application, resistors R_{Z1} and R_{Z2} serve two purposes. First, they act as Safety protection in case Z1 and Z2 are shorted (see section about Safety). Second, the resistors help mitigate EMI noise. Since the Source pin is floating, switching noise are coupled to both the input and output. R_{Z1} reduces the magnitude of the switching noise currents. A value of between 500 kΩ and 1 MΩ is recommended for R_{Z1} and R_{Z2} for EMI mitigation. A smaller value is possible as long as EMI is ok and as long as the current does not exceed the Z1/Z2 rating. Higher values might improve EMI further. However, they might cause more delay on the ZCD signal.

The passive filter network CF1, CF2, and RF1 decouples switching noise from the ZCD signal. Values must be chosen to ensure no switching noise is coupled while keeping the delay to a minimum. The recommended values are the following: CF1 = 100 pF, RF1 = 100 kΩ, CF2 = 100 pF.

VR1 clamps the ZCD signal to a level that is below the pin voltage specifications of the microcontroller.

High-Side Buck, Half-Wave Rectification ZCD with 2 Diodes

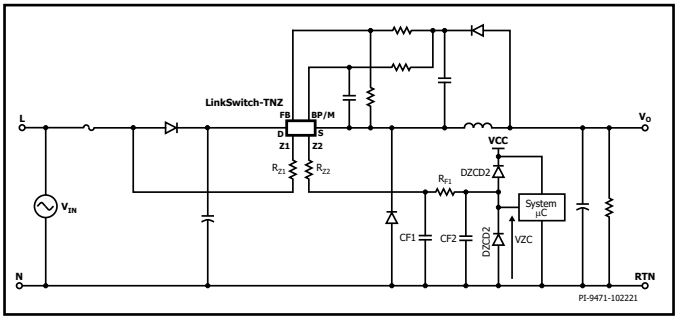


Figure 8. High-side Buck, Half-Wave Rectification, ZCD With Two Diodes Schematic.

The next configuration replaces the Zener with two diodes. The component selection is similar to previous configuration except the Zener replaced with two diodes. With this option, the ZCD logic high signal is more controlled because it is clamped to VCC + a diode drop. It also offers less delay because the Zener typically has higher capacitance compared to ordinary diode.

On the other hand, this configuration is not compatible with X capacitor discharge. To do so, replace the diode D_{ZCD1} with a Zener.

High-Side Buck, Half-Wave Rectification ZCD With MOSFET

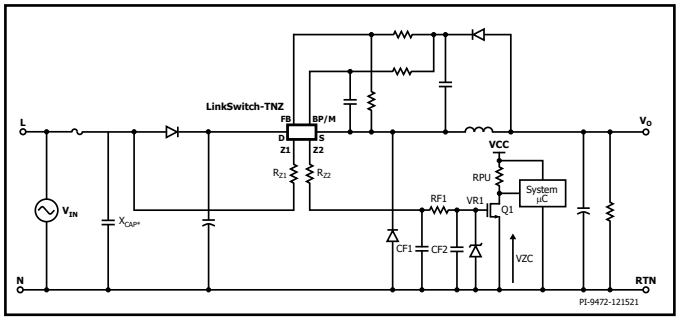


Figure 9. High-Side Buck, Half-wave Rectification, ZCD with MOSFET.

This configuration adds a MOSFET to the basic schematic on Figure 7. Here, the Zener diode VR1 clamps the gate voltage to less than the rating of MOSFT Q1. The recommended value is between 4.7 V and 10 V. The Drain of Q1 is then connected to the digital input of the microcontroller. The resistor R_{PU} is the pullup to the VCC.

This option provides sharper rising-edge and falling-edge ZCD signal. Also, the signal is limited to VCC instead of VCC + diode drop. R_{PU} can be removed if the input of the MCU is programmed to have an internal pull-up. A stronger pull-up is required to get faster slew rate.

High-Side Buck, Full-Wave Rectification ZCD With MOSFET

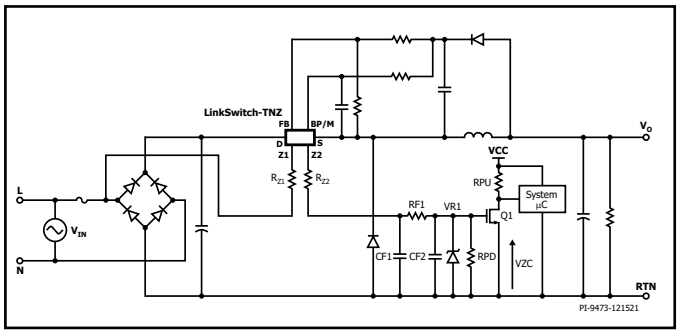


Figure 10. High-side Buck, Full-Wave Rectification, ZCD With MOSFET Schematic.

Half-wave rectification is the ideal configuration for ZCD because the current flows in either phase of the AC line. However, higher power applications may require full-wave rectification in order to minimize the value and size of the bulk capacitor. The recommended ZCD schematic is shown in Figure 10. It is similar to figure 9 except for the required pull-down resistor R_{PD}. This resistor is to ensure Q1 can be turned-OFF properly and prevent any leakage current from falsely turning it ON.

One limitation of this circuit is the sensitivity to probing that can disrupt the ZCD signal. See Tips for Design section for recommendations.

High-Side Buck-Boost, Half-Wave Rectification ZCD

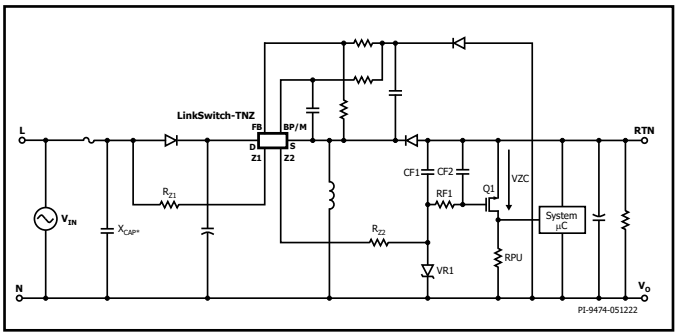


Figure 11. High-side Buck-Boost, Half-Wave Rectification, ZCD Schematic.

Figure 11 shows the typical implementation of ZCD in buck-boost converter. The circuit is also X cap discharge capable.

During the positive half-cycle, the Z1/Z2 current forward-biases VR1. The gate voltage (V_{GS}) of Q1 is equal to $V_O + V_{F(VR1)}$. For a nominal 5 V output, this gives a V_{GS} of 5.5 V, allowing Q1 to be a low cost logic level device. The 2N7000 for example has a maximum gate threshold of 3 V. Applying 5.5 V will fully enhance the device, pulling down the zero cross input of µC.

During the next half-cycle, the Z1/Z2 current flows through VR1 in the opposite direction, cathode to anode. Therefore the V_{GS} of Q1 is equal to $V_O - V_{VR1}$. For a nominal 5 V output and 6.8 V Zener, the gate is therefore at -1.8 V, turning off Q1. The value of VR1 should be selected such that $V_O - V_{VR1} \leq V_{GS(TH)}$. The 2N7000 has a maximum $V_{GS(TH)}$ value of 0.8 V and a maximum V_{GS} voltage of ±20 V.

No gate voltage clamping is required for V_O < 18 V. Above this, the voltage can be limited with a clamp Zener from gate to source or a resistor divider.

Tips for Designs

Start-Up With Non-Resistive Loads

If the total system capacitance is greater than 100 µF or the output voltage is >12 V, then during start-up the output may fail to reach regulation within 50 ms which can trigger auto-restart protection feature. This may also be true when the load is not resistive, for example, the output is supplying a motor or fan. To increase the start-up time, a soft-start capacitor can be added across the feedback resistor as shown in Figure 12. The value of this soft-start capacitor is typically in the range of 0.47 µF to 47 µF with a voltage rating of 1.25 x V_O. Addition of this capacitor can lead to instability in some designs that resembles bunching of switching cycles hence this recommendation should be carefully verified by measuring the output ripple under different operating conditions.

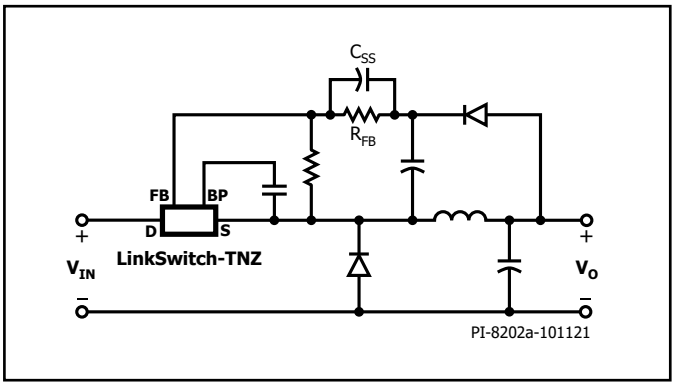


Figure 12. High-side Buck-Boost, Half-Wave Rectification ZCD Schematic.

Generating Negative and Positive Outputs

In appliance applications, there is often a requirement to generate both an AC line-referenced positive and negative output. This can be accomplished using the circuit in Figure 13. The two Zener diodes have voltage rating close to the required output voltage for each rail and ensure that regulation is maintained when one rail is lightly and the other heavily loaded. The LinkSwitch-TNZ circuit is designed as if it were a single output voltage with an output current equal to the sum of both outputs. The magnitude sum of the output voltages in this example is 12 V.

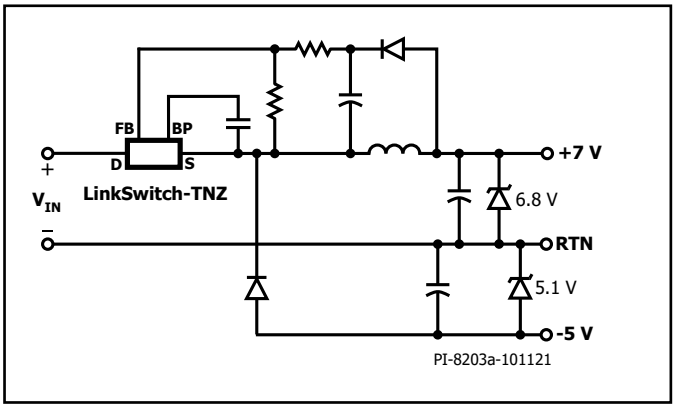


Figure 13. Example Schematic Showing Placement of Soft-Start Capacitor.

Thermal Environment

To ensure good thermal performance, the SOURCE pin temperature should be maintained below 110 °C by providing adequate heat sinking. For applications with high ambient temperature (>50 °C), it is recommended to build and test the power supply at the maximum operating ambient temperature and ensure that there is adequate thermal margin. The maximum output current specified in the data sheet is based on specific operating conditions and may need to be thermally derated. Also, it is recommended to use ultrafast (≤35 ns) low reverse recovery diodes at higher operating temperatures (>70 °C). If the device temperature exceeds 85 °C with ambient temperature of 25 °C, it is recommended the next bigger device in the family should be selected for the application.

A battery powered thermocouple meter is recommended to make measurements when the SOURCE pins are a switching node. Alternatively, the ambient temperature may be raised to indicate margin to thermal shutdown.

Design for Lowest Input Standby Current

In applications that require very low input leakage current during no-load or standby conditions (e.g., 2-wire smart switch), the following can be done to optimize the system for lowest input current:

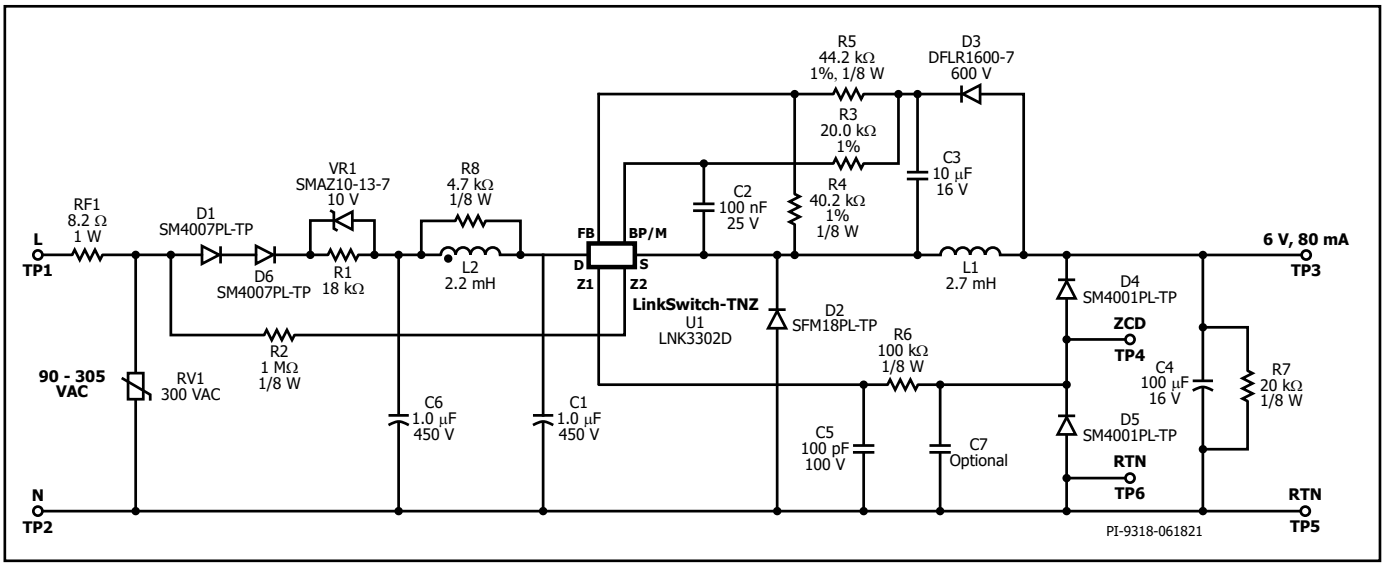


Figure 14. Example Circuit – Generating Dual Output Voltages.

R-Z Power Factor Circuit

The proprietary R-Z circuit is an important component in many 2-wire (no neutral) applications where minimizing leakage current at standby operation is critical. The circuit is formed by connecting the parallel combination of resistor and zener in series with the input (Figure 14). The resistor shapes the input current to increase the power factor at standby. When the load demands more power, the resistor itself will limit the current. This is where the Zener diode comes in. It provides a path for the current to pass through when the load demands it. At standby, it is designed to be disabled. The recommended value for the Zener is between 10 V and 20 V. Higher value may increase the effective of the power factor and reduce the input current further. However, it also limits the bulk capacitor voltage. Also, higher values would dissipate more power during line surge. Hence, a 1 W rating or higher is recommended depending on the surge requirements.

Once the Zener voltage is selected, the resistor is then tuned such that the voltage across the resistor is below the Zener voltage to ensure that the Zener is disabled. This yields the lowest current that the R-Z circuit can provide.

When used in high-power design, the dissipation across the Zener diode could impact system efficiency. Hence, the circuit is recommended for low-power design or when demand for power only happens for a short duration (such as recloser, or powering a latching relay).

Increase Feedback Resistors Resistors Value

The default feedback resistors set the lower divider resistor to a value of 2.49 kΩ. The upper resistor is then calculated in order to set the FB voltage to 2 V. This method is enough to get <30 mW of standby power. However, if standby current is more critical, or if lower standby power is desired, then one way of doing it is to reduce the dissipation from the feedback resistors. Verify load transient response to ensure that the output voltage is still within specifications after changing the feedback resistors.

Optimize BP Resistor

For output voltage >5 V, adding an external current source to BP can reduce input current substantially. The resistor is computed to supply IS1 to BP.

Optimize Pre-Load Resistor

High-side configuration usually requires a pre-load to maintain regulation at no-load. However, many applications for LinkSwitch-TNZ usually have minimum load to power microcontroller and other auxiliary circuits. Hence, the pre-load resistor can be optimized based on minimum load instead of no-load.

Zero Crossing Detection Measurement for Bridge Rectifier System

Buck and buck-boost designs with a ZCD circuit using bridge rectifier (Figure 10) may be sensitive to leakage current introduced by voltage probes or electronic loads.

The following are specific guidelines in probing and measuring the ZCD signal without compromising its signal integrity:

Current Probe Method (Recommended Setup)

While the ZCD signal being processed by the microcontroller is in terms of voltage, using a current probe to verify the signal prevents waveform distortion. Additional steps must be taken when using this technique:

- Avoid using an e-load. Use actual load or a resistive load instead
- Replace the pullup resistor RPU with lower resistance value in order to increase the current measurement resolution
- Place the current probe away from the IC or PCB to avoid switching noise coupling
- Use differential voltage probe to monitor the input voltage.

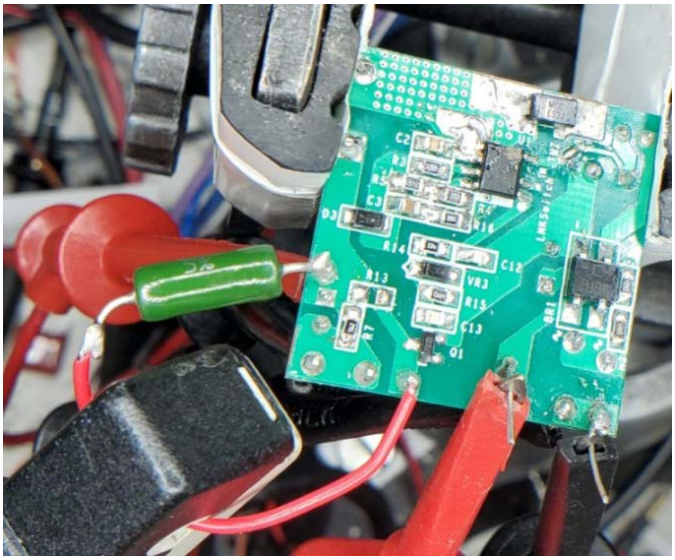


Figure 15. ZCD Signal using Current Measurement Set-up.

Voltage Probe Method (Alternative Set-up)

As an alternate set-up, the ZCD voltage can be measured using the following techniques:

- Connect input directly to AC mains line – do not use an electronic AC source
- Make sure that the oscilloscope ground (earth) line is connected
- Use differential voltage probes
- Use fixed resistor load instead of using e-load.

Figure 16. ZCD Signal using Voltage Measurement Set-up.

Conducted EMI Considerations

R_{Z1} + R_{Z2} Values

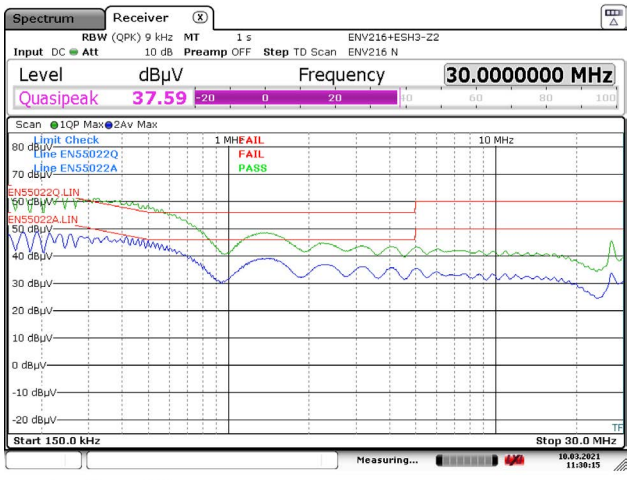
On high-side buck or buck-boost configuration where the LinkSwitch-TNZ Source is floating, noise may be coupled to the line via ZCD circuit. This is not a big concern for applications with X capacitor. However, for low power design where X capacitor is uncommon, EMI can be minimized by increasing the value of the series impedance (R_{Z1} + R_{Z2}) with the input. The total impedance of 1 MΩ provides a balance between EMI and ZCD delay.

Inductor Placement

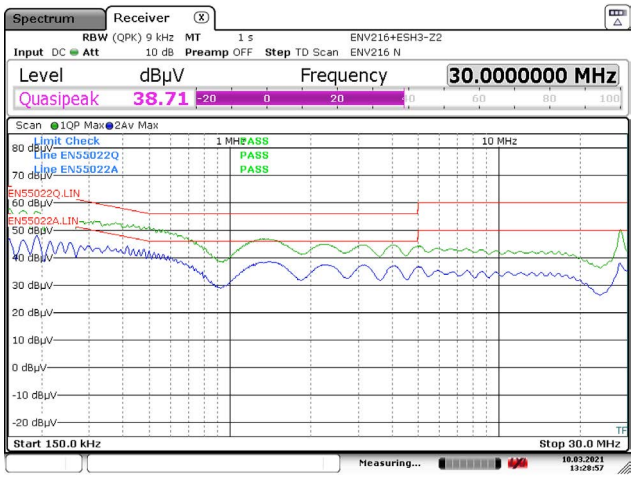
When using unshielded buck inductor, place it as far away from the AC input as possible. Comparison chart below shows how inductor placement can have significant EMI impact.

Buck inductor placed at the middle of the board closer to ac input

Buck inductor placed away from the ac input



Failed EMI when inductor placed at the middle of the board closer to ac input

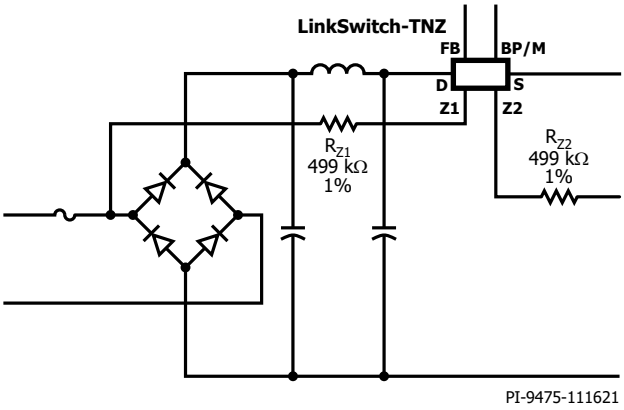


Passed EMI when buck inductor placed at the middle of the board closer to ac input

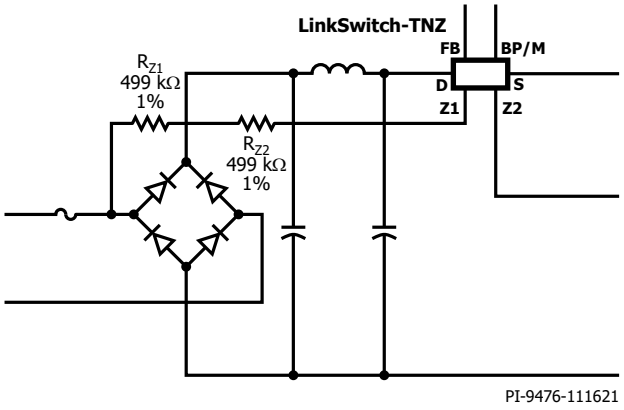
Table 16. Inductor Placement Impact on EMI.

R_{Z1}, R_{Z2} Placement

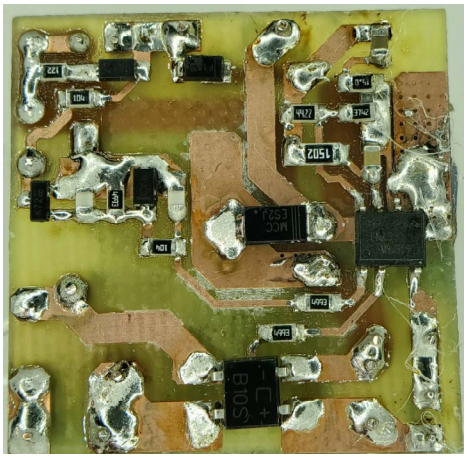
Aside from optimizing the value of R_{Z1} and R_{Z2}, their PCB mounting location also affects EMI. To get best EMI performance, place R_{Z1} resistor closer to the AC input. Some designs may also benefit by connecting R_{Z1} and R_{Z2} in series and placing them closer the AC input as shown in the example below.



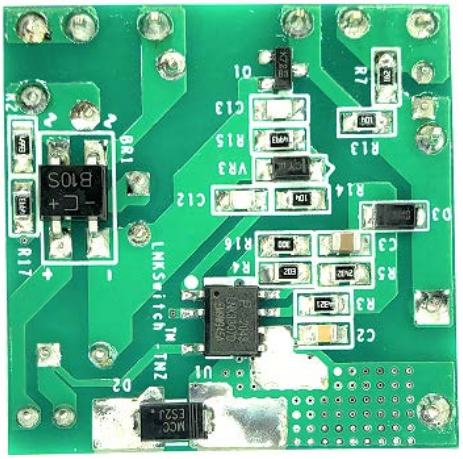
R_{Z1} and R_{Z2} split between Z1 and Z2 schematic



R_{Z1} and R_{Z2} placed in series and closer to input



Test board R_{Z1} and R_{Z2} split between Z1 and Z2



R_{Z1} and R_{Z2} placed in series and closer to input

EMI for R_{Z1} and R_{Z2} split between Z1 and Z2

Lower EMI for R_{Z1} and R_{Z2} placed in series and closer to input

Table 17. Inductor Placement Impact on EMI.

Tips for Audible Noise Reduction

- Use LNK3307D. It has a built-in current limit state machine that adjusts the current limit automatically based on load condition. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.
- Add hot melt glue around noise-inducing components like the power inductor.
- When using a "dog bone" or barrel type inductor, change orientation from vertical to horizontal mounting.
- Keep the inductor away from other large components.

Inductor Type and Mounting Orientation

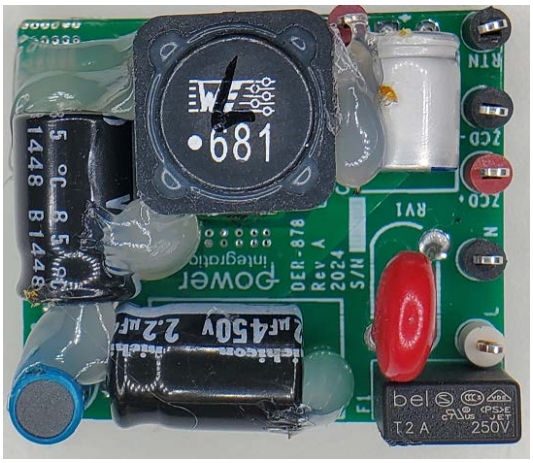
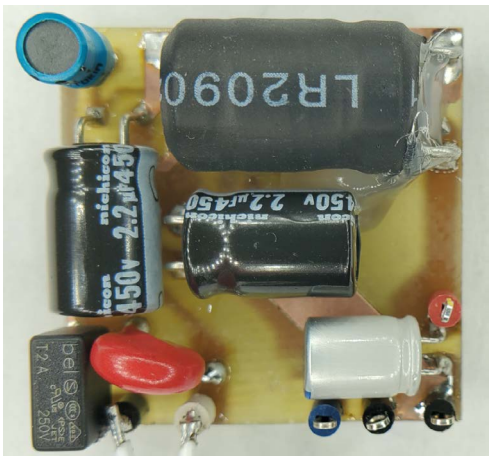
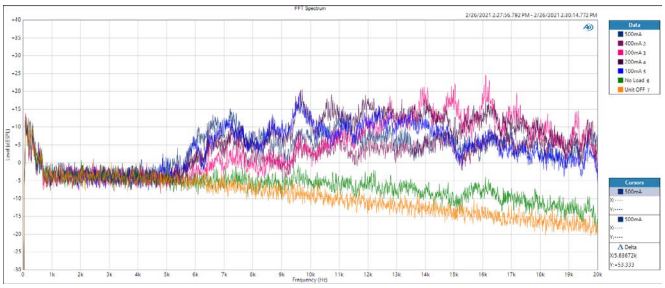
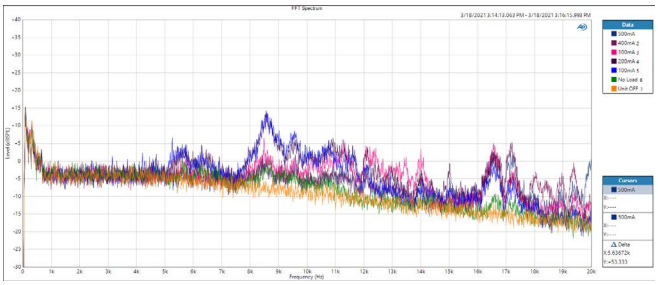
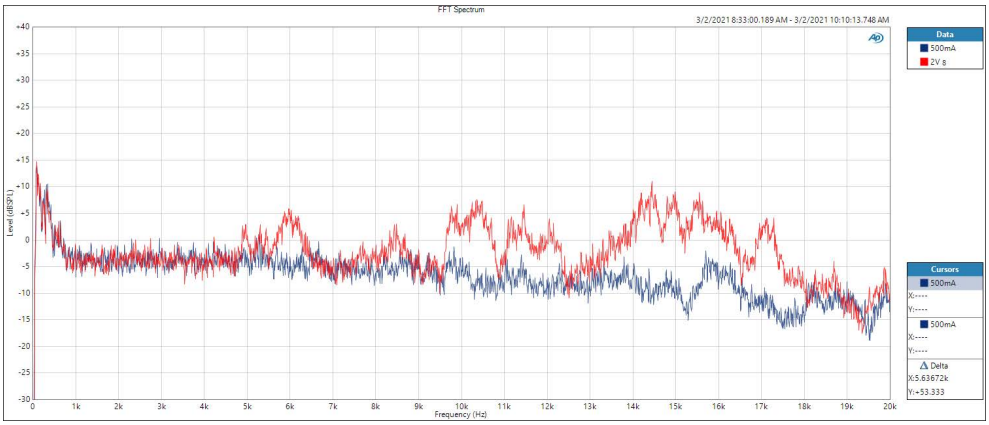
	
Shielded Buck inductor mounted vertically	Dog-bone Buck inductor mounted horizontally
	
SMD Shielded Inductor in vertical mounting generates more vibration in PCB Audible Noise < 25dBSPL	Dog Bone Type Inductor mounted horizontally Audible Noise < 10dBSPL

Table 18. Inductor Type and Orientation Impact on Audible Noise.

Type of Adhesive/Glue to Reduce Component Vibration

Table 19 shows the audible noise performance between two type of glue – hot melt glue (SDL4062-ND) and Devcon Epoxy.
The former is more elastic and acts like a cushion to minimize inductor vibration while the latter is hard and brittle which may worsen PCB vibration especially at full load.

	
Hot Melt Glue (SDL4062-ND)	Devcon Epoxy



Audible noise comparsion between two types of adhesives

Table 19. Glue Type and Impact on Audible Noise.

Special Consideration for LNK33x7D

LNK3307D and LNK3317D are the only devices in the LinkSwitch-TNZ product family that have current limit state machine (see Figures 2 to 5). As the output load is changed, the current limit also transitions to a different state. In some cases, pulse grouping may occur if the current limit is stuck from going back and forth one state change to another. This condition is more prone to happen at high line input, and with heavier or more CCM load.

Figure 17 shows the recommended circuit when using LNK33x7D in high-side buck or buck-boost applications. Resistor R6 is added and connected in series with feedback capacitor C5.

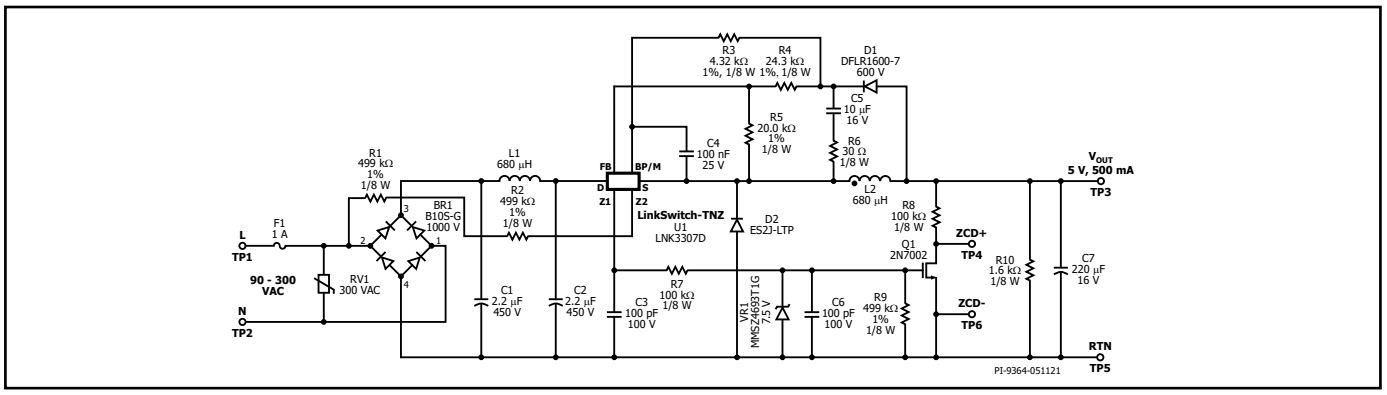
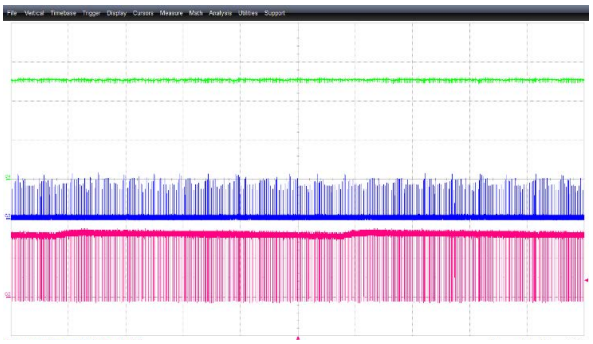


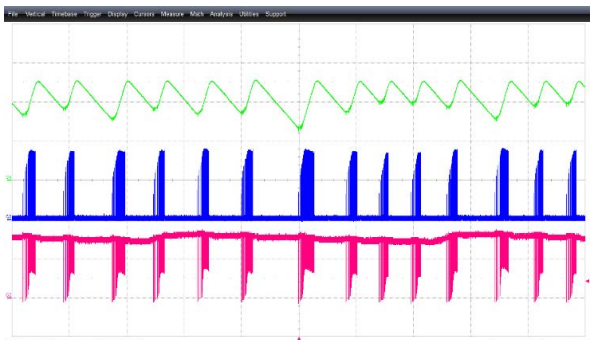
Figure 17. Glue Type and Impact on Audible Noise.

With R6 shorted, the waveforms looked normal at 300 mA load current (Figure 18). At 400 mA load (Figure 19), huge oscillation can be seen on the output voltage due to pulse grouping of the Drain current. This condition not only causes huge output voltage ripple but it can also result to higher audible noise.



CH2 (red): Drain voltage / CH3 (blue): Drain current
CH4 (green): Output voltage

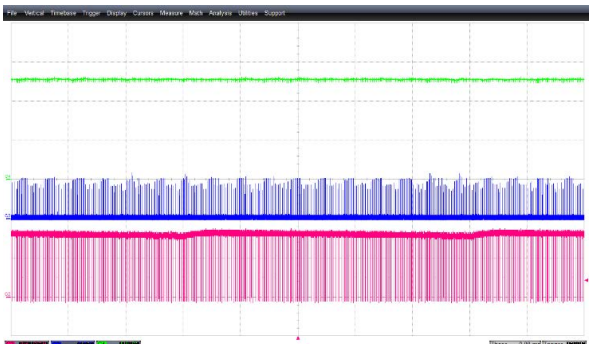
Figure 18. 230 VAC, 50 Hz, 300 mA load, R6 shorted.



CH2 (red): Drain voltage / CH3 (blue): Drain current
CH4 (green): Output voltage

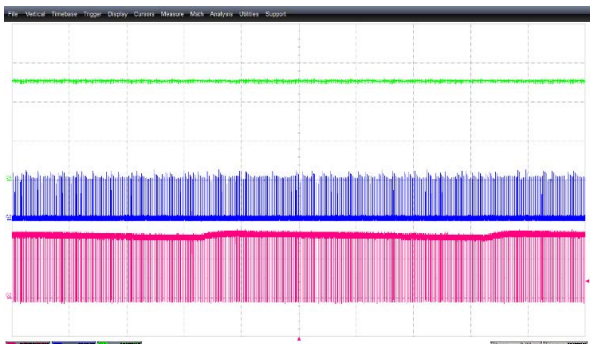
Figure 19. 230 VAC, 50 Hz, 400 mA load, R6 shorted.

With R6 connected, Figures 21 and 22 show that the oscillation is gone.



CH2 (red): Drain voltage / CH3 (blue): Drain current
CH4 (green): Output voltage

Figure 20. 230 VAC, 50 Hz, 300 mA load, R6 = 30 Ω.



CH2 (red): Drain voltage / CH3 (blue): Drain current
CH4 (green): Output voltage

Figure 21. 230 VAC, 50 Hz, 400 mA load, R6 = 30 Ω.

The drawback with this circuit is the slightly worse load regulation. Thus, choose a value between 4.7 Ω and 30 Ω to balance between regulation and output ripple.

Recommended Layout Considerations

Managing Thermals for High Power (High Current) Designs

- Use double-sided PCB with 2 oz copper
- Maximize copper area connected to SOURCE pins
- Provide enough copper heat sink on freewheeling diode.

Minimizing Noise

- Minimize the loop formed between LinkSwitch-TNZ DRAIN and SOURCE pins, freewheeling diode, and input capacitor traces carrying high current should be as short and thick as possible
- Keep output inductor away from the AC input whenever possible
- Controlling the start and end orientation of the output inductor when mounting on the board, especially for drum-core type, may help reduce EMI
- Place RZ1 and RZ2 resistors closer to AC input.

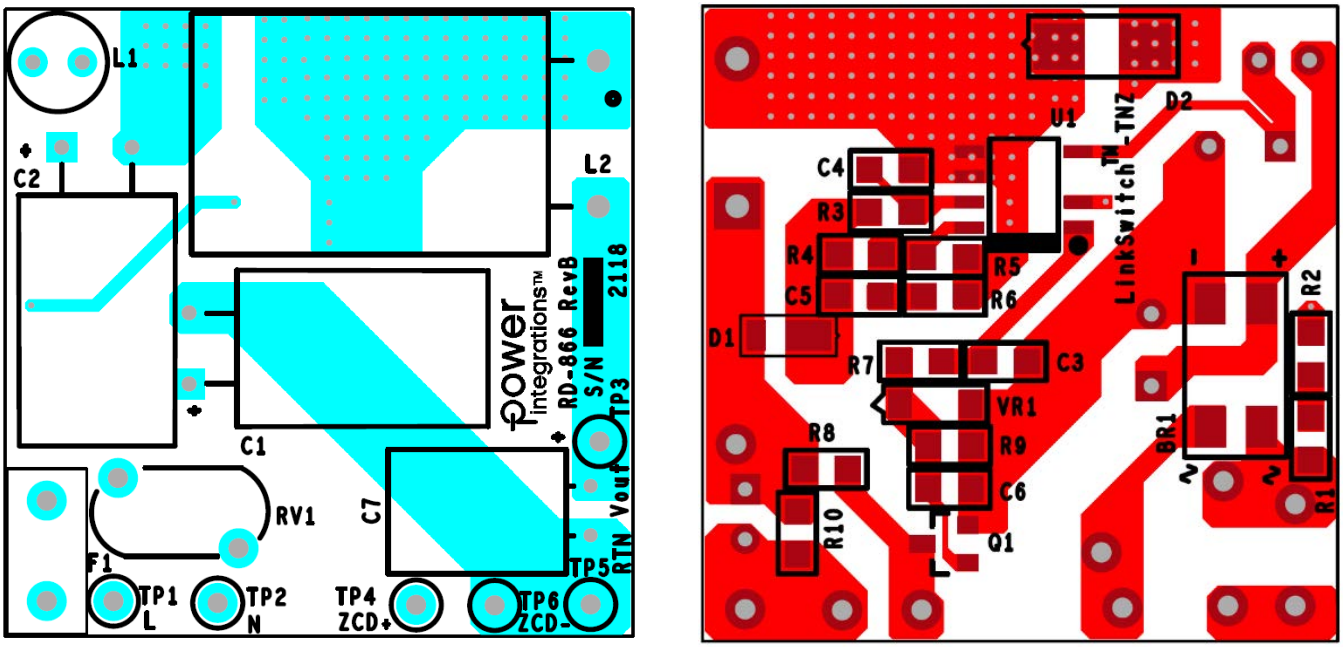


Figure 22. Recommended Printed Circuit Layout for LinkSwitch-TNZ using D Package.

Design for Safety Compliance

Z1/Z2 Creepage and Clearance
Based on UL/IEC 60950 safety standard, functional insulation can be met by satisfying any of these conditions:

1. Creepage and clearance requirements for functional insulation.
2. Withstand electric strength tests for functional insulation.
3. Short-circuited and there is no overheating of any material creating a risk of fire, no emission of molten material, no opening of PCB trace, and the temperature is within limits.

Z1 and Z2 pins functional safety compliance falls under condition 3 - i.e., even if the pins are shorted, there will be no risk of Safety violation as long as the external components (resistors, capacitors) are rated properly.

RZ1 and RZ2 Device Rating
When used as an X cap discharge, the voltage rating of the resistors should be able to handle the maximum input operating voltage. If used for ZCD only, then the resistors should not cause Safety failure when Z1 and Z2 pins are short-circuited.

Design for Surge Withstand
Power supplies are required to have capability of withstanding surge voltages which typically are a result of events such as lightning strikes. It is expected that such events do not lead to failure of any components or loss of functionality. Standards such as IEC61000-4-5 defines surge voltage and current waveforms as well as source impedance, which emulate typical worst case transients for testing of protection mechanisms for line connected power circuits and data line connected equipment.

Components of the fusible resistor, EMI filter and the capacitors used in the power supply input stage, help in limiting the voltage and current stress that the components of the power supply are subjected to during these events.

MOVs will often be required to be added at the input of the power supply if the surge level is high (DM surge >1 kV). These MOVs are placed after the input fuse and help in clamping the voltage at the input of the power supply when a surge event occurs.

Use the following checklist to ensure that the design is compliant to the applicable requirements:

- Define the target market for LinkSwitch-TNZ converter.
- Determine the equipment class to determine common-mode (CM) and differential-mode (DM) surge levels.
- If DM surge >1000 V, then you will likely need to include an MOV across the AC line at the front-end of the EMI filter
- Select a MOV for North America 115 VAC or universal input with adequate stand-off voltage during normal operation as well as adequate rated surge current and energy capacity.
- An example of selecting an MOV: Assume that you have a North America application within a Class 3 equipment installation for which you need to select a MOV for differential mode protection, connected across the AC line. The DM Spike Energy will be less than 6.9 J. A device rated for 150 VAC continuous operation would provide adequate stand-off voltage for 115 VAC nominal applications. Littlefuse part number V150LA5 provides 25 J and 2500 A surge capability with adequate margin to minimize degraded performance due to accumulated strikes over the life of the MOV. For a universal input design, the V320LA10 provides 48 J and 2500 A surge capability.
- Conduct both common-mode and differential-mode surge tests on the converter and observe voltages across key components and currents where necessary to validate SOA operation of components.
- Verify all voltage and current extremes are within the rated specification of each X and Y capacitor. If not, specify a component with a higher rating.
- Verify surge transient current rating of the diode bridge used.
- Verify MOSFET switch BV rating is greater than surge voltage on switching node. If not, you may need to increase bulk capacitor size to prevent the surge energy from increasing the capacitor voltage to objectionable levels.
- Ensure that bulk capacitor surge voltage rating is not exceeded during testing. If surge voltage rating is exceeded, you may need to increase capacitance. Some capacitors may tolerate higher than the rated surge voltage for short durations however capacitor manufacturers should be consulted for guidance.
- Select an AC line fusible resistor which has an I^2t rating that will accommodate power-on inrush current at maximum line voltage and which is rated for continuous AC line current and will not interrupt due to surge I_2t. Do not oversize the fuse more than necessary to withstand transient currents so as to ensure that the fuse will interrupt line current in the event of a line-to-line MOV failure.
- When making measurements on a power supply during a line surge or safety test, care should be taken to ensure that the test equipment is galvanically isolated. If alternate paths for the surge energy are created as a result of connection of test probes, the test result will be incorrect. Care must be taken to use voltage probes that are rated for measurement of high-voltages in excess of the voltages likely to be encountered during the test.

Half-Wave Rectifier Design Consideration
Some half-wave rectifier design has an additional diode connected to the AC return rail or Neutral. This technique is usually employed in order to reduce EMI as well as to increase surge withstand capability of the diode rectifier. On LinkSwitch-TNZ applications however, this configuration is not recommended because of the potential to disrupt the ZCD signal. Instead, follow the circuit shown on figure 23 to improve surge capability.

Appendix A – Application Example

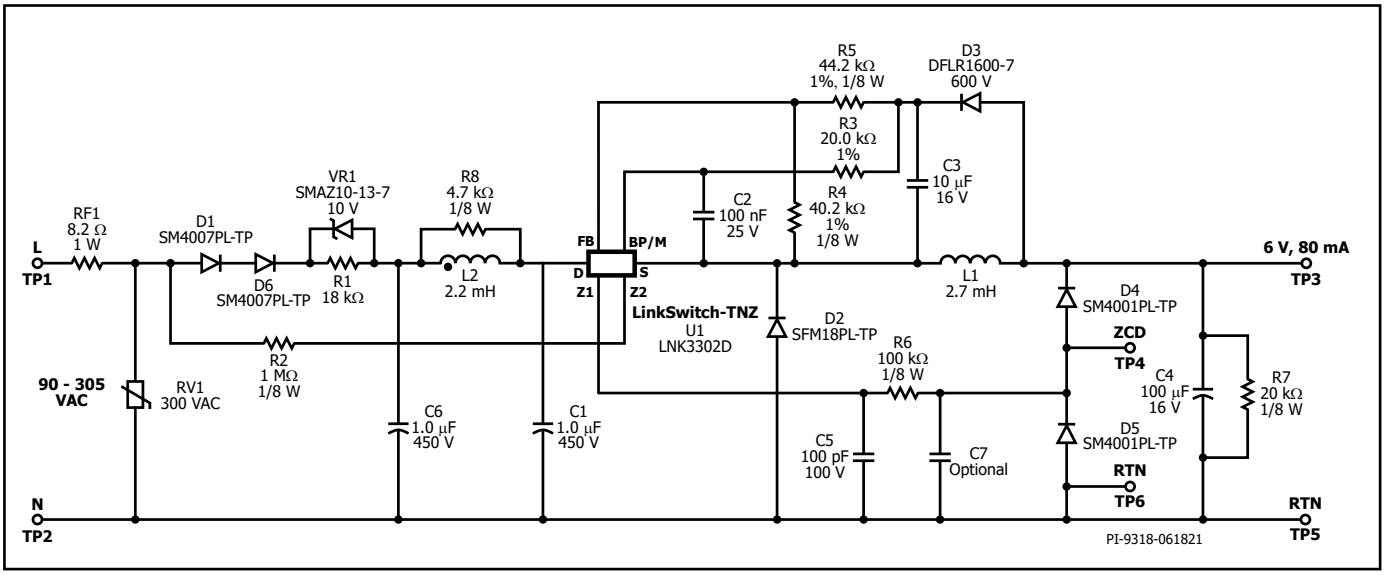


Figure 23. Universal Input, 6 V, 80 mA Constant Voltage Power Supply with Zero-Crossing Detector using LinkSwitch-TNZ.

A 0.48 W Universal Input Buck Converter

The circuit shown in Figure 23 is a typical implementation of a 6 V, 80 mA non-isolated power supply used in 2-wire smart switch applications.

The input stage comprises of fusible resistor RF1, varistor RV1, diodes D1 and D6, capacitors C1 and C6, inductor L2 with resistor R8, and the R-Z circuit R1 and VR1. Resistor RF1 is a flame-proof, fusible, wire-wound resistor. It accomplishes several functions:

A. Inrush current limitation to safe levels for rectifiers D3 and D4;
B. Differential mode noise attenuation;
C. Acts as an input fuse in the event any other component fails short-circuit (component fails safely open-circuit without emitting smoke, fire or incandescent material).

RV1 is added for surge protection. The R-Z circuit minimizes the no-load input current by putting a large series resistance R1 which increases the system power factor. The Zener diode clamps the voltage across R1 during startup and at higher output load.

D1 and D6 provide rectification as well as protection during ring-wave surge which is typically tested above 2 kV. In order to avoid a phase shift during ZCD measurement, it is not recommended to place one of the diodes on the Neutral side.

The power processing stage is formed by LinkSwitch-TNZ U1, freewheeling diode D2, output choke L1, and output capacitor C4. LNK3302 was selected such that the power supply operates in mostly continuous conduction mode (CCM). Diode D2 is an ultrafast diode with a reverse recovery time (t_{RR}) of 35 ns recommended for CCM operation. For mostly discontinuous conduction mode (MDCM) designs, a diode with a tRR of 75 ns is acceptable. Inductor L1 is a standard off-the-shelf inductor with appropriate RMS current rating. Capacitor C4 is a low-ESR electrolytic capacitor to minimize the output voltage ripple. A small pre-load R7 is required to limit the output voltage to about 110% of the rated voltage during light load or no-load condition.

Capacitor C2 with a value of 100 nF sets the current limit to Standard mode. Resistor R5 provides an external current supply to the BYPASS (BP) pin to lower the no-load input power.

To a first order, the forward voltage drops of D2 and D3 are identical. Therefore, the voltage across C3 tracks the output voltage. The voltage developed across C3 is sensed and regulated via the resistor divider R4 and R5 connected to U1's FEEDBACK pin. The values of R4 and R5 are selected such that, at the desired output voltage, the voltage at the FEEDBACK pin is 2 V.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds IFB then subsequent cycles will be skipped until the current reduces below IFB. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped.

To provide overload protection if no cycles are skipped during a 50 ms period, LinkSwitch-TNZ will enter auto-restart, limiting the average output power to approximately 3% of the maximum overload power.

Z1 and Z2 pins are configured to provide a lossless (<5 mW) zero crossing detection (ZCD) circuit. Z2 is connected to one of the input AC lines through resistor R2 while Z1 forms the ZCD signal output. When the AC voltage is more positive with respect to Neutral, D4 is forward-biased and clamps ZCD output to VOUT + 0.7 V. At the negative-going phase of the AC input, D5 is forward-biased and clamps ZCD output to -0.7 V.

The passive components comprised of R2, C5, R6, and optional C7 provide noise filtering to ensure clean ZCD signal. The values are chosen such that the overall ZCD delay is kept below 200 µs. C7 is a placeholder for the additional filter if needed. D5 has capacitance that helps avoid adding the extra capacitor. However, care must be taken when selecting the diode since too much capacitance will cause more delay.

Appendix B

Calculations for Inductor Value for Buck and Buck-Boost Topologies

There is a minimum value of inductance that is required to deliver the specified output power, regardless of line voltage and operating mode.

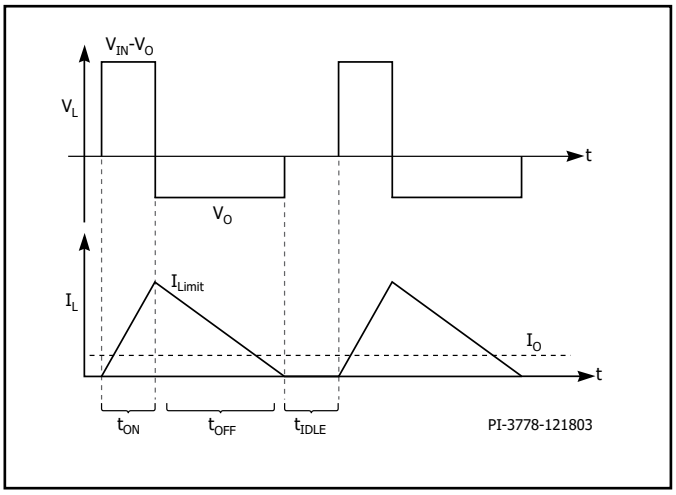


Figure 24. Inductor Voltage and Inductor Current of a Buck Converter in DCM.

As a general case, Figure 10 shows the inductor current in discontinuous conduction mode (DCM). The following expressions are valid for both CCM as well as DCM operation. There are three unique intervals in DCM as can be seen from Figure 10. Interval t_{ON} is when the LinkSwitch-TNZ IC is ON and the freewheeling diode is OFF. Current ramps up in the inductor from an initial value of zero. The peak current is the current limit I_{LIMIT} of the device. Interval t_{OFF} is when the LinkSwitch-TNZ IC is OFF and the freewheeling diode is ON. Current ramps down to zero during this interval. Interval t_{IDLE} is when both the LinkSwitch-TNZ IC and freewheeling diode are OFF, and the inductor current is zero.

In CCM, this idle state does not exist and thus $t_{IDLE} = 0$.

We can express the current swing at the end of interval t_{ON} in a buck converter as:

$$\Delta I(t_{ON}) = I_{RIPPLE} = \frac{V_{MIN} - V_{DS} - V_O}{L_{MIN}} \times t_{ON} \quad (C1)$$

$$I_{RIPPLE} = 2 \times (I_{LIMIT\_MIN} - I_O) \quad t_{IDLE} = 0 (for\ CCM) \quad (C2)$$

$$I_{RIPPLE} = (I_{LIMIT\_MIN,}) \quad t_{IDLE} > 0 (for\ MDCM) \quad (C3)$$

where
I_{RIPPLE} = Inductor ripple current
I_{LIMIT_MIN} = Minimum current limit
V_{MIN} = Minimum DC bus voltage
V_{DS} = On-state Drain to Source voltage drop
V_O = Output voltage
L_{MIN} = Minimum inductance

Similarly, we can express the current swing at the end of interval t_{OFF} as:

$$\Delta I(t_{OFF}) = I_{RIPPLE} = \frac{V_O + V_{FD}}{L_{MIN}} \times t_{OFF} \quad (C4)$$

The initial current through the inductor at the beginning of each switching cycle can be expressed as:

$$I_{INITIAL} = I_{LIMIT\_MIN} - I_{RIPPLE} \quad (C5)$$

The average current through the inductor over one switching cycle is equal to the output current I_O. This current can be expressed as:

$$I_O = \frac{1}{T_{SW\_MAX}} \left(\frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times t_{ON} + \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times t_{OFF} + 0 \times t_{IDLE} \right) \quad (C6)$$

Where
I_O = Output current.
T_{SW_MAX} = The switching interval corresponding to minimum switching frequency F_{SMIN}.

Substituting for t_{ON} and t_{OFF} from equations (C1) and (C4) we have:

$$I_O = \frac{1}{T_{SW\_MAX}} \left(\frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times \frac{I_{RIPPLE} \times L_{MIN}}{V_{MIN} - V_{DS} - V_O} + \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times \frac{I_{RIPPLE} \times L_{MIN}}{V_O + V_{FD}} + t_{IDLE}) \right) \quad (C7)$$

$$L_{MIN} = \frac{2 \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{(I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad (C8)$$

For MDCM design, $I_{INITIAL} = 0$, $I_{RIPPLE} = I_{LIMIT\_MIN}$.

$$L_{MIN} = \frac{2 \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{I_{LIM\_MIN}^2 \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad (C9)$$

For CCM design, $t_{IDLE} = 0$.

$$I_O = \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \quad (C10)$$

$$I_{INITIAL} = I_{LIM\_MIN} \quad (C11)$$

$$L_{MIM} = \frac{(V_O + V_{FD}) \times (V_{MIN} - V_{DS} - V_O)}{2 \times (I_{LIM\_MIN} - I_O) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad (C12)$$

For output voltages greater than 20 V, use V_{MAX} for calculation of L_{MIN} (Equation C8). For output voltages less than 20 V, use V_{MIN} for calculation of L_{MIN} to compensate for current limit delay time over-shoot.

This however does not account for the losses within the inductor (resistance of winding and core losses) and the freewheeling diode, which will limit the maximum power delivering capability and thus reduce the maximum output current. The minimum inductance must compensate for these losses in order to deliver specified full load power. An estimate of these losses can be made by estimating the total losses in the power supply, and then allocating part of these losses to the inductor and diode. This is done by the loss factor K_{LOSS} which increases the size of the inductor accordingly. Furthermore, typical inductors for this type of application are bobbin core or dog bone chokes. The specified current rating refer to a temperature rise of 20 °C or 40 °C and to an inductance drop of 10%. We must

incorporate an inductance tolerance factor K_{L_TOL} within the expression for minimum inductance, to account for this manufacturing tolerance. The typical inductance value thus can be expressed as:

$$L_{TYP} = \frac{(1+K_{L\_TOL}) \times L_{MIN}}{K_{LOSS}} \quad \text{(C13)}$$

where
K_{LOSS} is a loss factor, which accounts for the off-state total losses of the inductor.

K_{L_TOL} is the inductor tolerance factor and can be between 10% and 20%. A typical value is 0.15. With this typical inductance we can express maximum output power as:

$$P_{O\_MAX} = L_{TYP} \times FS_{MIN} \times (I_{LIMIT\_MIN}^{2} - I_{INITIAL}^{2}) \times \frac{V_O \times (V_{MIN} - V_{DS} + V_{FD})}{2 \times (V_{MIN} - V_{DS} - V_O) \times (V_O + V_{FD})} \times \frac{K_{LOSS}}{(1 + K_{L\_TOL})} \quad \text{(C14)}$$

Similarly for buck-boost topology the expressions for L_{TYP} and P_{O_MAX} are:

$$L_{TYP} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIMIT\_MIN}^{2} - I_{INITIAL}^{2}) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)} \quad \text{(C15)}$$

$$P_{O\_MAX} = L_{TYP} \times FS_{MIN} \times (I_{LIMIT\_MIN}^{2} - I_{INITIAL}^{2}) \times \frac{V_O \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}{2 \times (V_{MIN} - V_{DS}) \times (V_O + V_{FD})} \times \frac{K_{LOSS}}{(1 + K_{L\_TOL})} \quad \text{(C16)}$$

Average Switching Frequency

Since LinkSwitch-TNZ uses an on-off type of control, the frequency of switching is non-uniform due to cycle skipping. We can average this switching frequency by substituting the maximum power as the output power in Equation C14. Simplifying, we have:

$$FS_{AVG} = 2 \times (1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIMIT\_MIN}^{2} - I_{INITIAL}^{2}) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD})} \quad \text{(C17)}$$

Similarly for buck-boost converter, simplifying Equation C16 we have:

$$FS_{AVG} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIMIT\_MIN}^{2} - I_{INITIAL}^{2}) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)} \quad \text{(C18)}$$

Calculation of RMS Currents

The RMS current value through the inductor is mainly required to ensure that the inductor is appropriately sized and will not overheat. Also, RMS currents through the LinkSwitch-TNZ IC and freewheeling diode are required to estimate losses in the power supply. Assuming CCM operation, the initial current in the inductor in steady state is given by:

$$I_{INITIAL} = I_{LIM\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t_{OFF} \quad \text{(C19)}$$

t_{OFF} is when MOSFET is off.
For DCM operation this initial current will be zero.

The current through the LinkSwitch-TNZ as a function of time is given by:

$$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS} - V_O}{L_{TYP}} \times t, 0 < t \leq t_{ON} \quad \text{(C20)}$$

$$i_{SW}(t) = 0, t_{ON} < t \leq T \quad \text{(C21)}$$

t_{ON} is when MOSFET is on.
The current through the freewheeling diode as a function of time is given by:

$$i_D(t) = 0, 0 < t \leq t_{ON} \quad \text{(C22)}$$

$$i_D(t) = I_{ILIM\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF} \quad \text{(C23)}$$

$$i_D(t) = 0, t_{OFF} < t \leq T \quad \text{(C24)}$$

t_{OFF} is when freewheeling diode is on.
And the current through the inductor as a function of time is given by:

$$i_L(t) = i_{SW}(t) + i_D(t) \quad \text{(C25)}$$

From the definition of RMS currents we can express the RMS currents through the switch, freewheeling diode and inductor as follows:

$$i_{SW\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T i_{SW}(t)^2 \times dt} \quad \text{(C26)}$$

$$i_{D\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T i_D(t)^2 \times dt} \quad \text{(C27)}$$

$$i_{L\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T (i_{SW}(t) + i_D(t))^2 \times dt} \quad \text{(C28)}$$

Since the switch and freewheeling diode currents fall to zero during the turn-off and turn-on intervals respectively, the RMS inductor current is simplified to:

$$i_{L\_RMS} = \sqrt{i_{SW}^{2} + i_D^{2}} \quad \text{(C29)}$$

Table C1 lists the design equations for important parameters using the buck and buck-boost topologies.

Parameter	Buck	Buck-Boost
L_{TYP}	$L_{TYP} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})}$	$L_{TYP} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}$
FS_{AVG}	$FS_{AVG} = 2 \times (1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD})}$	$FS_{AVG} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}$
$i_{SW}(t)$ LinkSwtich-TN2 Current	$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS} - V_O}{L_{TYP}} \times t, 0 < t \leq t_{ON}$ $i_{SW}(t) = 0, t_{ON} < t \leq T$	$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS}}{L_{TYP}} \times t, 0 < t \leq t_{ON}$ $i_{SW}(t) = 0, t_{ON} < t \leq T$
$i_D(t)$ Diode Forward Current	$i_D(t) = 0, 0 < t \leq t_{ON}$ $i_D(t) = I_{LIMIT\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF}$ $i_D(t) = 0, t_{OFF} < t \leq T$	$i_D(t) = 0, 0 < t \leq t_{ON}$ $i_D(t) = I_{LIMIT\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF}$ $i_D(t) = 0, t_{OFF} < t \leq T$
$i_L(t)$ Inductor Current	$i_L(t) = i_{SW}(t) + i_D(t)$	$i_L(t) = i_{SW}(t) + i_D(t)$
Max Drain Voltage	V_{MAX}	$V_{MAX} + V_O$

Table 20. Circuit Characteristics for Buck and Buck-Boost Topologies.

Appendix C – Protection Feature for Flyback Applications

Hysteretic Output Overvoltage Protection

In flyback topology, the output overvoltage protection provided by the LinkSwitch-TNZ IC uses auto-restart that is triggered by a current >$I_{BP(SD)}$ into the BYPASS pin. To prevent inadvertent triggering of this feature, in addition to an internal filter, the BYPASS pin capacitor provides external filtering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS pins of the device.

The OVP function can be realized in a non-isolated flyback converter by connecting a Zener diode from the output to the BYPASS pin. The circuit example shown in Figure 11 describes a simple method for implementing the output overvoltage protection. Additional filtering for the OVP detection feature, can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode and the BYPASS pin voltage will cause a current in excess of $I_{BP(SD)}$ injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter configuration, during the power MOSFET on-time, the LinkSwitch-TNZ IC can sense indirectly the DC bus overvoltage condition by monitoring the current flowing into the FEEDBACK pin depending on circuit configuration. Figure 12 shows one possible circuit implementation. During the power MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. The current flowing through emitter and base of transistor Q3 is therefore directly proportional to the V_{BUS} voltage.

$$V_{PRI} = V_{BUS} - V_{DS} \quad \text{(D1)}$$

V_{DS} is much smaller compared to the bus voltage which can be neglected.

The voltage across the secondary winding is proportional to the voltage across the primary winding.

$$V_{SEC} = \frac{V_{PRI}}{n} \quad \text{(D2)}$$

$$-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3} = V_{SEC} \quad \text{(D3)}$$

The voltage across the Zener diode VR3 is therefore dependent on V_{BUS}. When the line voltage is higher than its threshold and the Zener diode VR3 is turned on, transistor Q3 is turned on and current will flow into FEEDBACK pin from the BYPASS pin capacitor through transistor Q3. When the fed current is higher than FEEDBACK pin

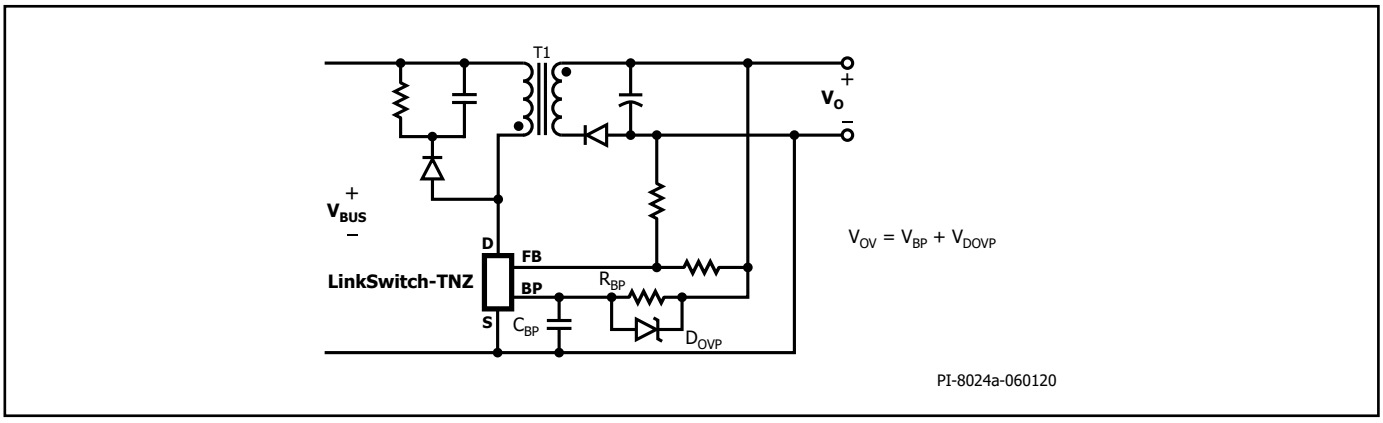


Figure 25. Non-Isolated Flyback Converter with Output Overvoltage Protection.

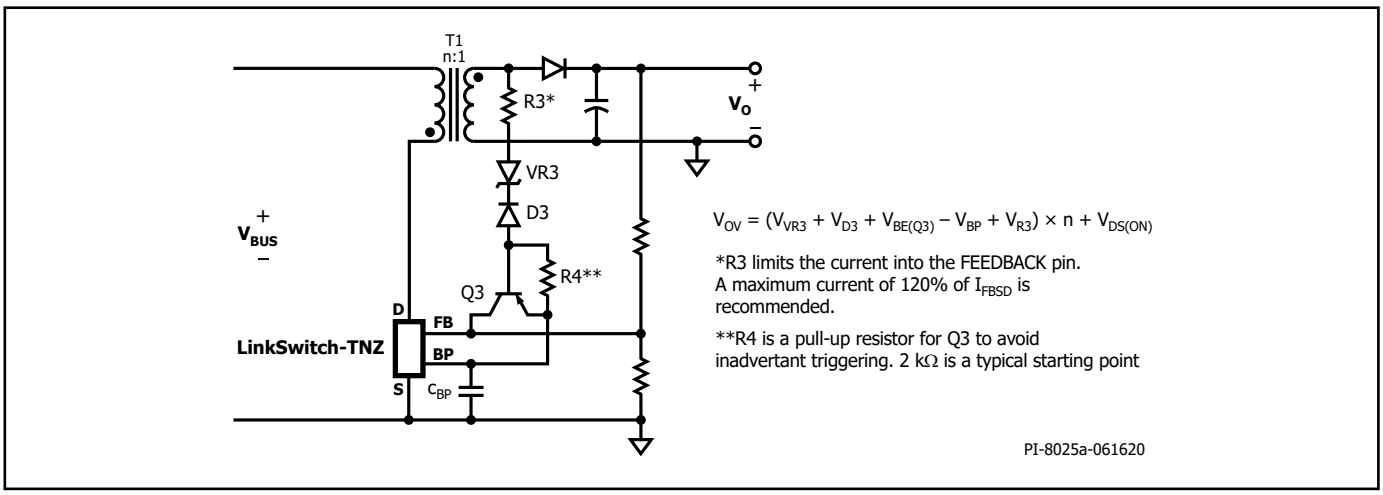


Figure 26. Line-Sensing for Overvoltage Protection by using FEEDBACK Pin..

instant shutdown current $I_{FB(SD)}$ for at least 2 consecutive switching cycles, the line overvoltage protection will be triggered and the LinkSwitch-TNZ IC will go into auto-restart mode.

The threshold for the bus overvoltage is:

$$V_{OV} = (-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3}) \times n + V_{DS} \quad \text{(D4)}$$

Indirect line sensing minimizes power dissipation otherwise incurred in a typical primary side line overvoltage detection circuit.

Resistor R4 is used as a weak pull-down resistor to help avoid inadvertent conduction of Q3 during normal operation. A 2 kΩ resistor can be used for R4. Based on the selection of the zener diode and transistor, the value of R4 may need to be adjusted. R3 is used to limit the current into the FEEDBACK pin. The current through resistor R3 is equal to the sum of current through R4 and current through emitter and base of Q3, which is:

$$I_{R3} = I_{Q3(EB)} + I_{R4} \quad \text{(D5)}$$

From equation D4:

$$I_{R3} = \frac{V_{R3}}{R3} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(EB)} - V_{D3} - V_{VR3}}{R_3} \quad \text{(D6)}$$

And

$$I_{R4} = \frac{V_{BE(Q3)}}{R_4} \quad \text{(D7)}$$

From the equation D6 and D7:

$$I_{Q3(EB)} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3}}{R3} - \frac{V_{BE(Q3)}}{R4} \quad \text{(D7)}$$

The current into FEEDBACK pin is the collector current of Q3 if the transistor is not saturated, which is calculated as:

$$I_{Q3(EC)} = h_{FE} \times I_{Q3(EB)} = h_{FE} \times \left[\frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3} - V_{VR3}}{R3} - \frac{V_{BE(Q3)}}{R4} \right] \quad \text{(D8)}$$

The current of $I_{Q3(EC)}$ should not exceed 120% of $I_{FB(SD)}$ in order to limit the current into the FEEDBACK pin.

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding and provide accurate line OVP detection. The current into the FEEDBACK pin is sampled and compared to $I_{FB(SD)}$ typically 280 ns after the high-voltage power MOSFET is turned on.

In some designs if the ringing at the secondary winding is longer than 280 ns, a RC snubber across the rectifier diode may be needed to damp the ringing to ensure precise detection of line voltage.

Below is an example with 33 V Zener (VR3) BZX74-C33, and the threshold is at 308 V. When the bus voltage is higher than the threshold, the power supply goes into auto-restart. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ – first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

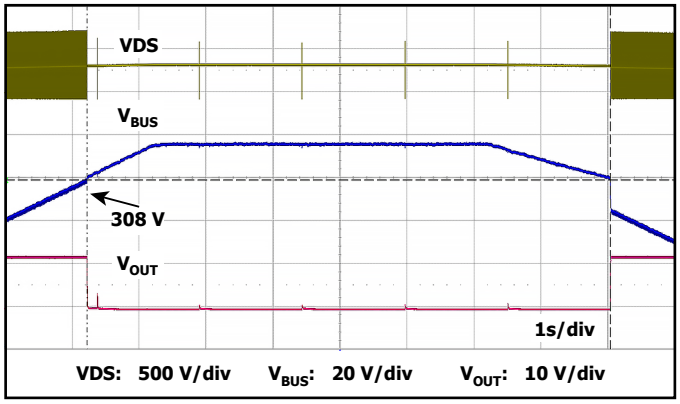


Figure 27. Indirect Line-Sensing for Overvoltage Protection Result.

Revision	Notes	Date
A	Code A release.	04/22
B	Updated Figure 11 on page 14.	05/22

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