2SM0120D2C1C
SCALE-iFlex™ Family

Module Adapted Gate Driver (MAG) for Half-Bridge Power Modules Electrical Interface

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for LV100 and XHP2 power modules up to 3300 V blocking voltage
- Optimized for different Half-Bridge Power Modules from different suppliers
- Applicable for paralleling of up to 4 power modules
- -40 °C to +85 °C operating ambient temperature
- Optical status indicators

Protection / Safety Features

- Short-circuit protection with Advanced Soft Shut Down (ASSD)
- Undervoltage lock-out (UVLO)
- NTC temperature sensing with reinforced isolated digital output signal (PWM-coded signal provided by associated Isolated Master Control (IMC))
- DC-link voltage measurement with reinforced isolated digital output signal (PWM-coded signal provided by associated IMC)
- Applied double sided conformal coating
- RoHS compliant

Applications

- Wind and photo-voltaic power
- Traction inverter
- Industrial drives
- Other industrial applications

Description

This datasheet describes the Module Adapted Gate Driver (MAG) of the SCALE-iFlex gate driver family which works conjointly with a central Isolated Master Control (IMC) and a cable set.

The IMC is designed for operation of power modules with a blocking voltage of up to 3300 V, whereas the MAGs are available in various variants optimized for different power modules of different suppliers and chip technologies in the voltage classes up to 3300 V.

SCALE-iFlex enables easy paralleling of up to four power modules providing high flexibility and system scalability with minimum development effort.

Integrated NTC temperature and DC-link voltage signals with reinforced isolation are available as a substitution for discrete system-level sensors.

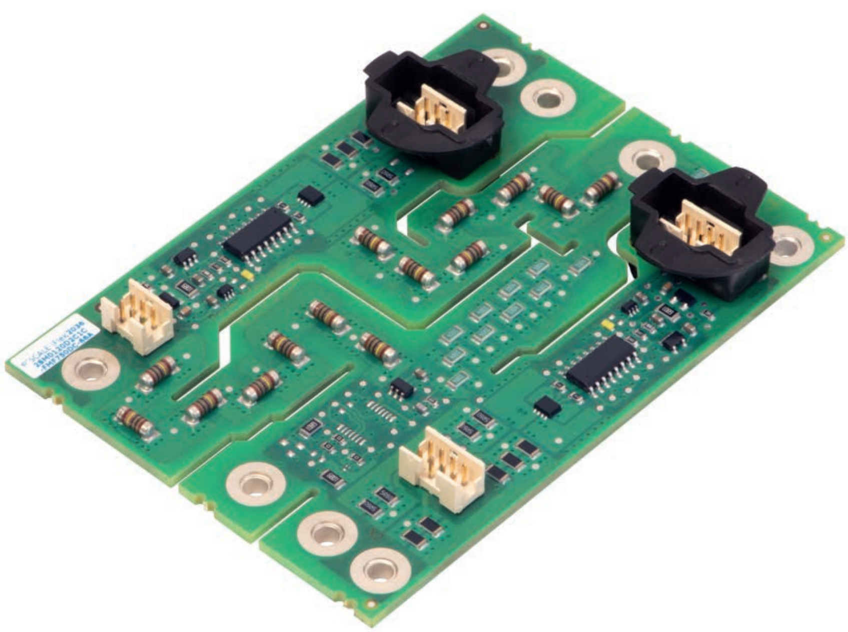

Figure 1. Board Photo of 2SM0120D2C1C.

This Product is Covered by Patents and/or Pending Patent Applications.

Pin Functional Description

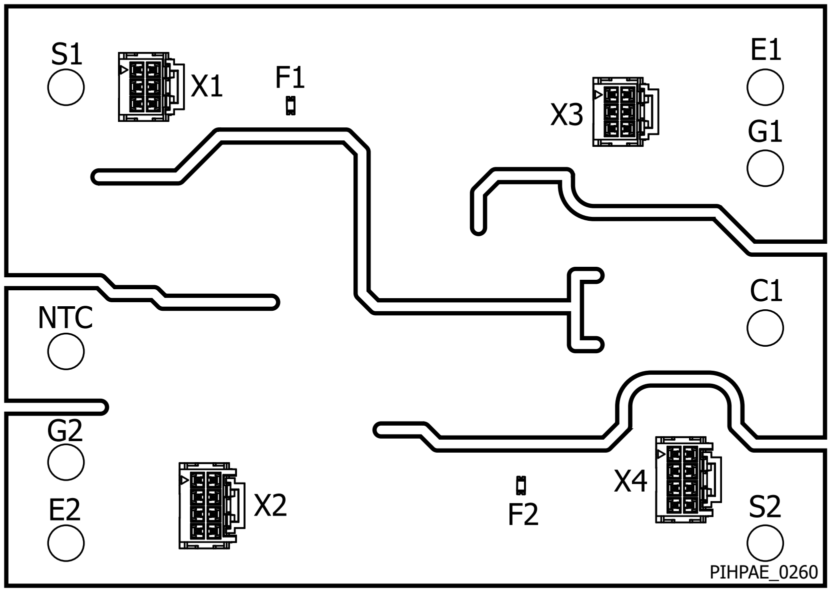

Figure 2. Pin Configuration of 2SM0120D2C1C.

Connection to IMC or another MAG

Connector X1

Interface of channel 1 to either IMC or to previous MAG (X3) in case of parallel connection of power modules.

Part number: Amphenol FCI, 10075025-G02-06ALF

Connector X2

Interface of channel 2 to either IMC or to previous MAG (X4) in case of parallel connection of power modules.

Part number: Amphenol FCI, 10075025-G02-08ALF

Connector X3

Interface of channel 1 to other MAG (X1) in case of paralleled power modules.

Part number: Amphenol FCI, 10075025-G02-06ALF

Connector X4

Interface of channel 2 to other MAG (X2) in case of paralleled power modules.

Part number: Amphenol FCI, 10075025-G02-08ALF

Note: Connectors X1 and X3 resp. X2 and X4 cannot be inverted

Connections to Power Module

Terminal G1
Gate contact of channel 1 switch.

Terminal E1
Auxiliary emitter contact of channel 1 switch.

Terminal C1
Auxiliary collector contact of channel 1 switch.

Terminal G2
Gate contact of channel 2 switch.

Terminal E2
Auxiliary emitter contact of channel 2 switch.

Optical Indicator F1
White optical indicator for status feedback signal of channel 1. During a fault condition the indicator is OFF.

Optical Indicator F2
White optical indicator for status feedback signal of channel 2. During a fault condition the indicator is OFF.

Screw holes S1, S2
Screw holes for mechanical fixation of the board to the power module.

NTC
Contacts to module internal NTC.

Functional Description

The 2SM0120D2C1C (MAGs) are dual channel plug-and-play gate drivers for XHP2/LV100 power modules. The MAGs are fully mechanically and electrically adapted to the IGBT modules (XHP 2, LV100). They work in conjunction with the IMC to drive up to 4 parallel connected power modules (one MAG per power module is necessary).

Connector Terminals (X1 and X2)
The MAGs have two connector terminals per channel which cannot be mixed up.

The channel assignment must not be mixed up. Channel 1 from the IMC (X1) must be connected to channel 1 of the MAG (X1). Similarly, channel 2 of the IMC (X2) with channel 2 of the MAG (X2).

In case more than one MAG is used, i.e. paralleling of two to four power modules, the first MAG needs to be connected with the second MAG. Similarly, the second MAG with the third MAG and so on. Also in this case the channel assignment must not be mixed, i.e. terminal X1 has to be connected with X3 and terminal X2 with X4.

Screw Terminals (S1, S2)
The MAG is mounted on top of the power module and fixed by screws.

Optical Indicators
The MAGs have optical indicators to signal the following operating conditions:

One white LED per driver channel (F1 for channel 1 and F2 for channel 2 in Figure 2) which is ON during normal operation and OFF during short-circuit or UVLO condition.

Cables
SCALE-iFlex gate drivers require a set of cables to establish the electrical connection between the IMC and the first MAG as well as between paralleled MAGs. The usage of cables allows flexible positioning of the IMC within the application.

Furthermore, it allows adapting to various pitches between paralleled power modules. For instance, forced air-cooled systems require a larger pitch than liquid-cooled systems due to the difference in heat spreading.

Gate Voltage
SCALE-iFlex possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage of the power semiconductor equals in steady-state the positive supply voltage V_{VISO}.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady-state the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no-load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under-voltage lock-out condition, the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection
The SCALE-iFlex gate driver uses the semiconductor desaturation effect to detect short-circuits and protects the device against damage by employing an Advanced Soft Shut Down (ASSD) technique.

The desaturation is monitored on each MAG by using a resistor or resistor/capacitor sensing network. The collector-emitter voltage is checked after the response time t_{RES} at turn-on to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(SAT)}$, the driver detects a short-circuit condition. The monitored semiconductor is switched off immediately and a fault signal is transmitted to the IMC. Paralleled MAGs detect desaturation conditions with minimum time delays and turn off the corresponding power semiconductor with ASSD.

It should be noted that the response time t_{RES} is dependent on the DC-link voltage. It typically remains constant between about 50% to 100% of the maximum DC-link voltage and increases at lower DC-link voltages. Please refer to the relevant datasheet section.

The desaturation function is for short-circuit detection only and cannot provide overcurrent protection. However, overcurrent detection has a lower time priority and can be easily provided by the application.

Gate Clamping
In the event of a short-circuit condition, the gate voltage is increased due to the high dv_{CE}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{CE}/dt drives a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor. To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage each MAG features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{VISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. This is shown in Figure 3 in the time period from 0.5us to 6.2us, where the short-circuit current asymptotically increases toward a flat plateau. As a consequence, the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enabling a safe turn-off of the device.

Advanced Soft Shut Down (ASSD) Function

The ASSD function reduces the turn-off di/dt to limit the collector-emitter overvoltage as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the power semiconductor is turned off within its safe operating area.

The ASSD function is realized with a closed-loop scheme, which is activated as soon as a short-circuit event is detected. The MAG then measures the gate-emitter voltage and current and adjusts them according to the three following phases:

- In the first step, the gate-emitter voltage is decreased to a defined level which is controlled by the closed-loop feedback (Figure 3, from t_1 to t_2).
- The defined level of the gate-emitter voltage is kept steady to ramp down the collector current smoothly, i.e. with lower di_C/dt, until the gate charge profile of the power semiconductor has reached the end of the Miller plateau. The end of the Miller plateau is detected by evaluating the gate current (Figure 3, from t_2 to t_3).
- The gate-emitter voltage is then reduced to its end value, following a given reference value (Figure 3, from t_3 to t_4).

The ASSD function is only active under short-circuit conditions and not under normal operating conditions (e.g. at nominal current or in overcurrent conditions).

Conformal Coating

The electronic components in the gate driver are protected by a layer of acrylic conformal coating on both sides of the PCB with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters. This coating layer increases product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer must be prevented. This water will diffuse through the layer over time. If allowed to remain, it will eventually form a thin film between the PCB surface and coating layer, which will cause leakage currents to increase. Such currents will interfere with the performance of the gate driver.

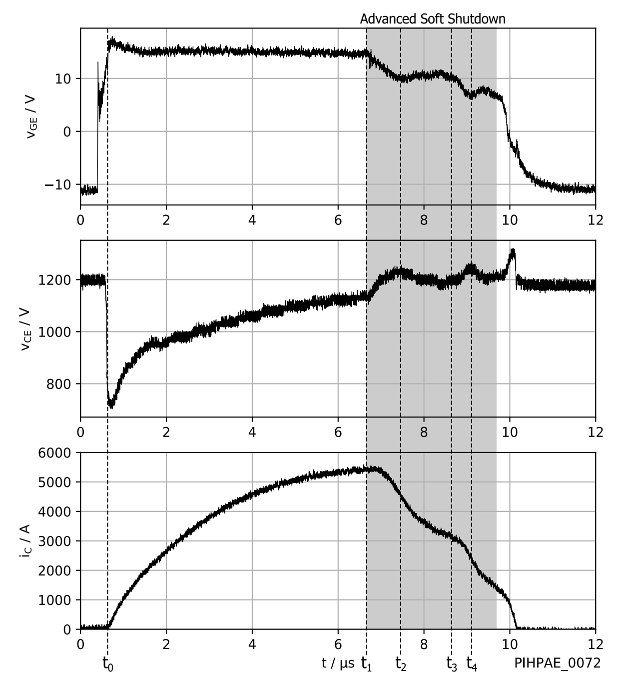

Figure 3. Example waveform of Advanced Soft Shut Down (ASSD)

Absolute Maximum Ratings

Parameter	Symbol	Conditions TA = -40°C to 85°C	Min	Max	Units
Absolute Maximum Ratings[1]					
Gate Output Power per Channel[2]	P_{Gx}			1	W
Switching Frequency[3]	f_{SW}			25	kHz
Common-Mode Transient Peak Voltage	$\|dv_E\|$	Between parallel connected emitters		50	V
Common-Mode time-Voltage-Area	$\int\|dv_E\|\cdot dt$	Between parallel connected emitters		15	µVs
Common-Mode Current	$\|I_{CMrms}\|$	Between parallel connected MAGs		1.2	A_{RMS}
	$\|I_{CMpk}\|$			15	A_{pk}
DC-link Voltage	$V_{DC\text{-}Link}$	Continuous operation (3.3 kV driver versions)		2200	V_{DC}
		Limited to 60 s[4] (3.3 kV driver versions)		2500	
		Continuous operation (1.7 kV driver versions)		1200	
		Limited to 60 s[4] (1.7 kV driver versions)		1300	
Operating Voltage	V_{CE}	3.3 kV driver versions		3300	V
		1.7 kV driver versions		1700	
Storage Temperature[5]	T_{st}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Component Surface Temperature[6]	T			125	°C
Relative Humidity	H_r	No condensation		93	%
Altitude of Operation[7]	A_{op}			2000	m

NOTES:
1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Actual achievable maximum power depends on several parameters and may be lower than the given value. It has to be validated in the final system. It is mainly limited by the maximum allowed surface temperature.
3. This limit applies to the whole product family. The actual achievable switching frequency may be lower for specific gate driver variants and has to be validated in the final system as it is additionally limited by the maximum gate output power in conjunction with the maximum allowed surface temperature.
4. This limit is given by the gate driver itself. Lower values may be possible due to limitation given by the RBSOA of the used IGBTs.
5. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
6. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value to ensure long-term reliability of the product.
7. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Characteristics

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Units
Power Supply							
Total idle Power Consumption	$P_{MAG,idle}$	No load, both MAG channels, V_{VISO} - V_{COM} = 25 V			0.6		W
Power Supply Monitoring Threshold	$UVLO_{VISO}$	Referenced to respective terminal E1 or E2	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	
			Hysteresis	0.35			
	$UVLO_{COM}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		
			Hysteresis		0.3		
Gate Output							
Gate Turn-on Voltage	$V_{GE(on)}$	IMC supplied with 36 V, all load conditions, referenced to E1 or E2			15		V
Gate Turn-off Voltage	$V_{GE(off)}$	IMC supplied with 36 V, without load, referenced to E1 or E2			-9.6		V
		IMC supplied with 36 V, P_{Gx} = 1 W per channel, 4 MAGs, referenced to E1 or E2			-8.8		
Short-Circuit Protection							
Static V_{CE}-Monitoring Threshold	$V_{CE(SAT)}$	(3.3 kV driver versions)			114		V
		(1.7 kV driver versions)			30		
Response Time (10% V_{GE} to 90% V_{GE})	t_{RES}	10% to 90% of V_{GE} (with 3.3 kV IGBT modules)	DC-link voltage = 2500 V		6.7		µs
			DC-link voltage = 1500 V		6.8		
			DC-link voltage = 1000 V		7.7		
		10% to 90% of V_{GE} (with 3.3 kV SiC modules)	DC-link voltage = 2500 V		2.9		
			DC-link voltage = 1500 V		3.3		
			DC-link voltage = 1000 V		5.6		
		10% to 90% of V_{GE} (with 1.7 kV IGBT modules)	DC-link voltage = 1200 V		5.0		
			DC-link voltage = 1000 V		5.0		
			DC-link voltage = 800 V		5.4		
Delay to Power Semiconductor Turn-off After Short-Circuit Detection	$t_{pd,SC}$				0.2		µs
Electrical Isolation							
Creepage Distance	CPG_{S-S}	Secondary side to secondary side		22			mm
Clearance Distance	CLR_{S-S}	Secondary side to secondary side		8			mm
Mounting							
Mounting Holes	D_{HOLE}	Diameter of screw holes			3.3		mm
Screw Header/Washer Diameter	D_{M3}	Terminals G1, E1, C1, G2, E2, S1, S2 and NTC				8.0	mm
Terminal Connection Torque	M_{MAG}	Refer to the datasheet of the respective power modules					Nm
Bending	I_{BEND}	According to IPC				0.75	%

Reliability and EMC Qualification Items

Test Item	Test Methods and Conditions
Environmental Tests	
Dry heat	IEC 60068-2-2, 85 °C, 240 h, DUT operated
Cold	IEC 60068-2-1, -40 °C, 96 h, DUT operated
Thermal cycling	IEC 60068-2-14, -40 °C and 85 °C, ramp: 5 °C/min, dwell: 30 min, DUT operated, 10 cycles
Endurance Tests	
High temperature operating lifetime	IEC 60068-2-2, 85 °C, test duration 1000 h, DUT operated
Damp heat	IEC 60068-2-78, 85 °C / 85% R.H., 56d, DUT operated
Thermal cycling	IEC 60068-2-14, -40 °C, 125 °C (5 K/min, 100 cycles, DUT unpowered)
EMC Tests	
Burst immunity	IEC 61000-4-4, 5 kHz, ± 4 kV (60s), 15 ms per package, 300 ms per period
Conducted noise immunity	IEC 61000-4-6, frequency range 0.15 – 80 MHz and 27 – 68 MHz, log 1%, 80% AM (1 kHz), 20 V
Conducted disturbances	IEC 61000-4-3, 80 - 6000 MHz, log 1%; 10V/m (2 s), vertical and horizontal
Radiated disturbances	EN 55016-2-1, frequency range 0.15 - 0.5 MHz, limit 99 dBµV QP and 0.5 - 30 MHz, limit 93 dBµV QP
Magnetic field immunity	IEC 61000-4-8, 1000 A/m (3 s), 3 axis
	IEC 61000-4-8, 100 A/m (60 s), 3 axis
	IEC 61000-4-9, 1000 A/m, (5 pulses), 3 axis
	IEC 61000-4-10, 100 kHz , 100 A/m (60s), 40/s
	IEC 61000-4-10, 1 MHz , 100 A/m (60s), 400/s
	IEC 61000-4-18, 100 kHz (60s), 40/s, 1 kV line to line, 2 kV lines to ground
	IEC 61000-4-18, 1 MHz (60s), 40/s, 1 kV line to line, 2 kV lines to ground
Mechanical Tests	
Mechanical vibrations (sinusoidal)	IEC 60068-2-6, frequency range 200 - 500 Hz (± 3.3 mm displacement, 15 m/s², 10 sweep cycles), according to EN 60721-3-5, Cat. 5M2
Mechanical shock	IEC 60068-2-27, acceleration 300m/s², half sine, 3 axis, ±100 shocks per axis, according to EN 60721-3-5, Cat. 5M2
	IEC 61373, Class 1B, acceleration 30 m/s², duration 30 ms, vertical and transversal, half sine, ±100 shocks per axis
	IEC 61373, Class 1B, acceleration 50 m/s², duration 30 ms, longitudinal, half sine, ±100 shocks per axis
Mechanical vibration (random)	IEC 61373, Class 1B, 5 Hz - 150 Hz, 1 h, 3 axis
Mechanical vibrations (long-life)	5 Hz - 150 Hz, 5 h, 3 axis

Product Dimensions

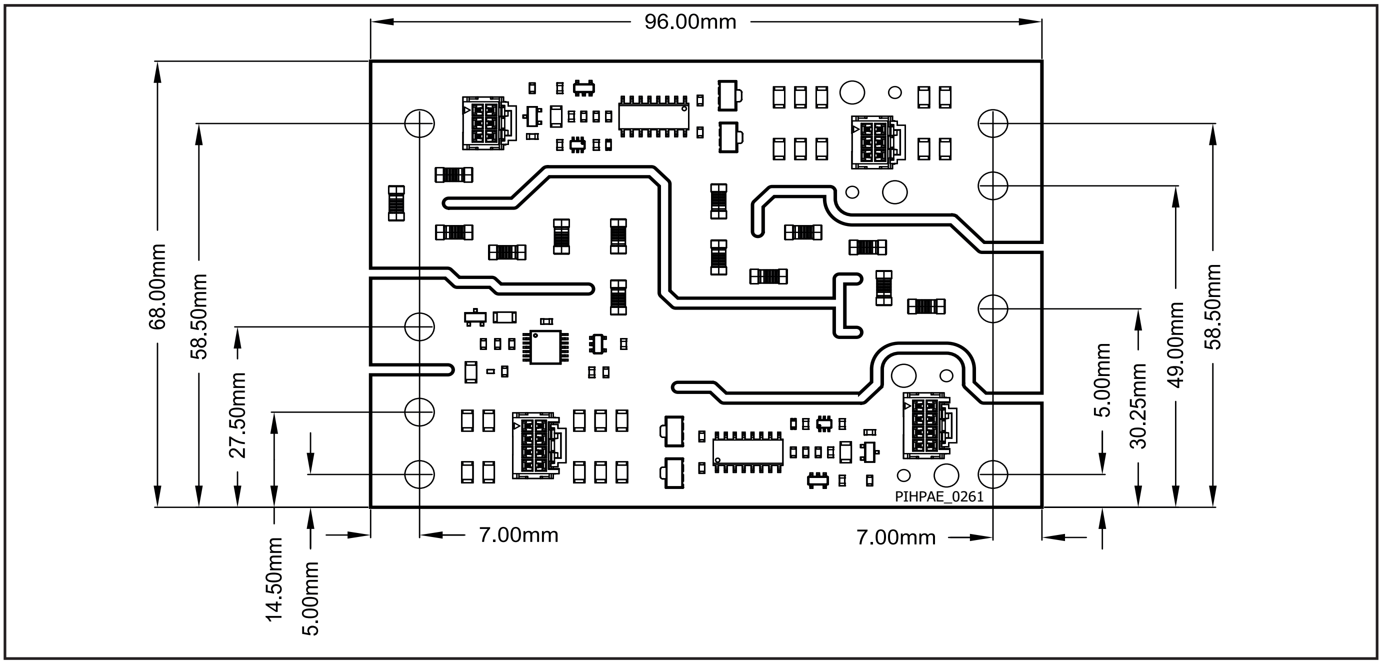

Figure 4. Top View of 2SM0120D2C1C.

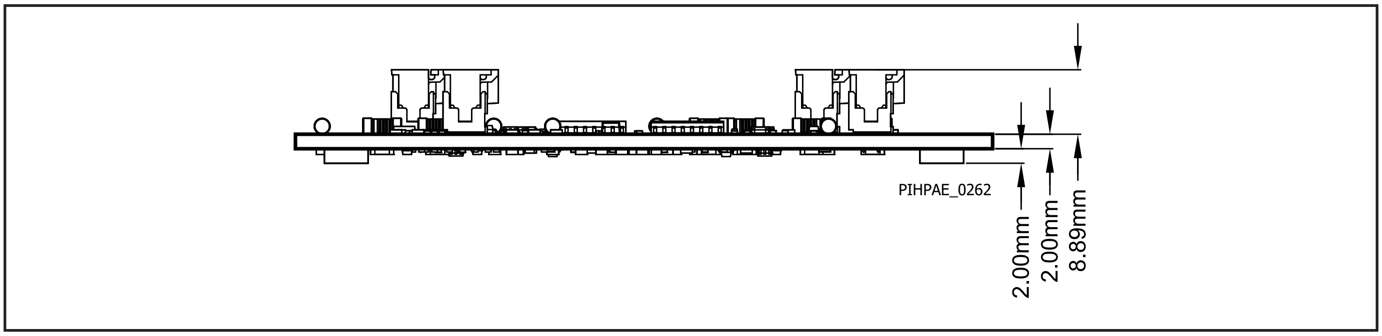

Figure 5. Side View of 2SM0120D2C1C.

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Product details

Part Number	Power Module	Voltage Class	Current Class	Package	IGBT Supplier	$R_{G(ON)}$	$R_{G(OFF)}$	C_{GE}
2SM0120D2C1C-FMF750DC-66A	FMF750DC-66A	3300 V	750 A	LV100	Mitsubishi	0.4 Ω	1.4 Ω	Not assembled
2SM0120D2C1C-CM600DA-66X	CM600DA-66X	3300 V	600 A	LV100	Mitsubishi	2.275 Ω	55 Ω	33 nF
2SM0120D2C1C-CM450DA-66X	CM450DA-66X	3300 V	450 A	LV100	Mitsubishi	2.75 Ω	67.5 Ω	33 nF
2SM0120D2C1C-CM1200DA-34X	CM1200DA-34X	1700 V	1200 A	LV100	Mitsubishi	1.175 Ω	7.5	33 nF

Revision	Notes	Date
A	Final Datasheet	11/22

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