Design Example Report

Title	***100 W Low Profile TV Power Supply by Using PFS7524L and LNK6777V***
Specification	90 VAC – 264 VAC Input; 12 V / 3.7 A and 24 V / 2.32 A Outputs
Application	LCD TV
Author	Applications Engineering Department
Document Number	DER-393
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Revision	3.2

Summary and Features

- Integrated PFC stage using
  - PFS7524L from HiperPFS family of ICs
- Integrated flyback stage using
  - LNK6777V from LinkSwitch-HP family of ICs
  - Primary side regulated isolated flyback converter with ±5% regulation
- Meeting light load consumption requirement without using CAPZero
- Very low no-load consumption
- PFC turn off circuit turns on and off PFC stage smoothly

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 12 V, 3.7 A and 24 V, 2.32 A power supply for 90 VAC to 264 VAC LCD TV applications. This design can also serve as a general purpose evaluation board for the combination of a HiperPFS-3 power factor stage with LinkSwitch-HP output stage using devices from the Power Integration's HiperPFS-3 and LinkSwitch-HP device families.

The design is based on the PFS7524L IC for the PFC front end, with a LNK6777V utilized in an isolated flyback output stage.

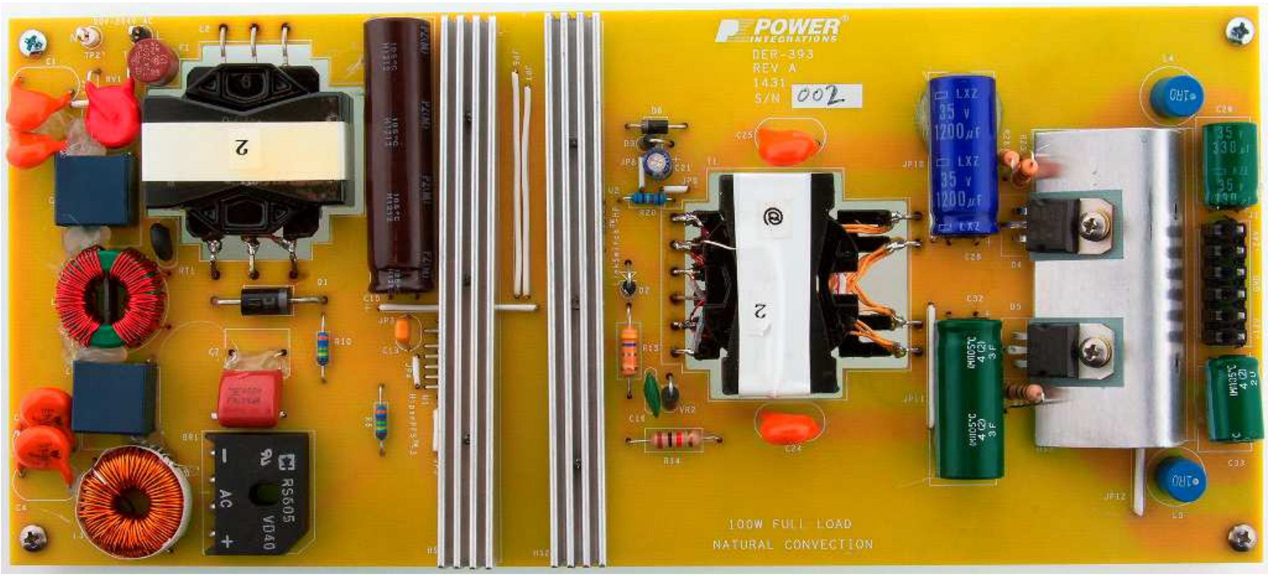

Figure 1 – DER-393 Photograph, Top View.

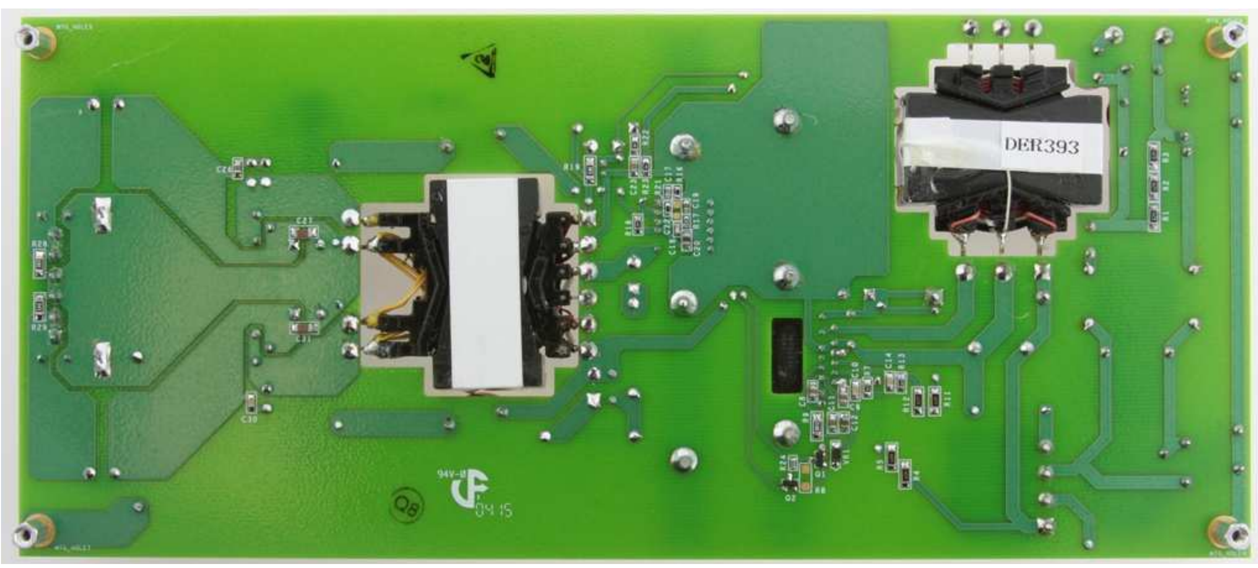

Figure 2 – DER-393 Photograph, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	2 Wire Input
Frequency	f_{LINE}	47	50/60	63	Hz	
Output 1						
Output Voltage	V_M	11.4	12	12.6	V	12 VDC ±5%
Output Ripple	$V_{RIPPLE(M)}$			120	mV P-P	20 MHz Bandwidth
Output Current	I_M	0.00	3.7	N/A	A	
Output 2						
Output Voltage	V_{SB}	21.6	24	26.4	V	24 VDC ±10%
Output Ripple	$V_{RIPPLE(SB)}$			240	mV P-P	20 MHz Bandwidth
Output Current	I_{SB}	0.00	2.32	N/A	A	
Total Output Power						
Continuous Output Power	P_{OUT}		100		W	

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3 Schematic

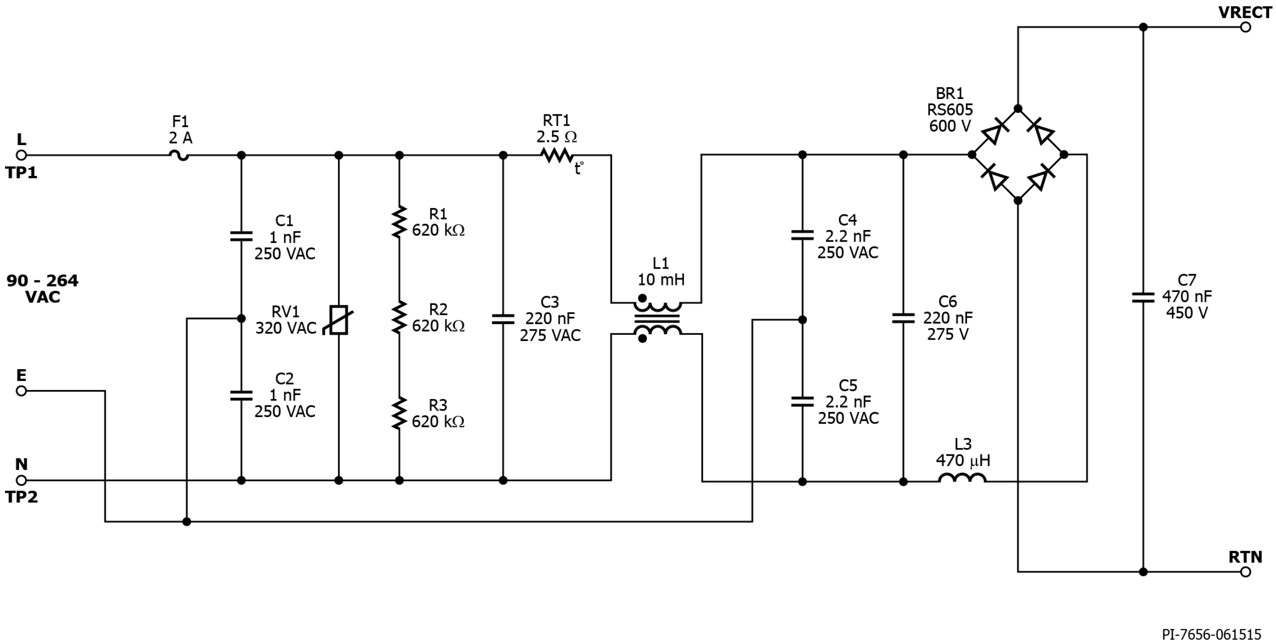

Figure 3 – Schematic. LCD TV Power Supply Application Circuit - Input EMI Filter and Rectifier Section.

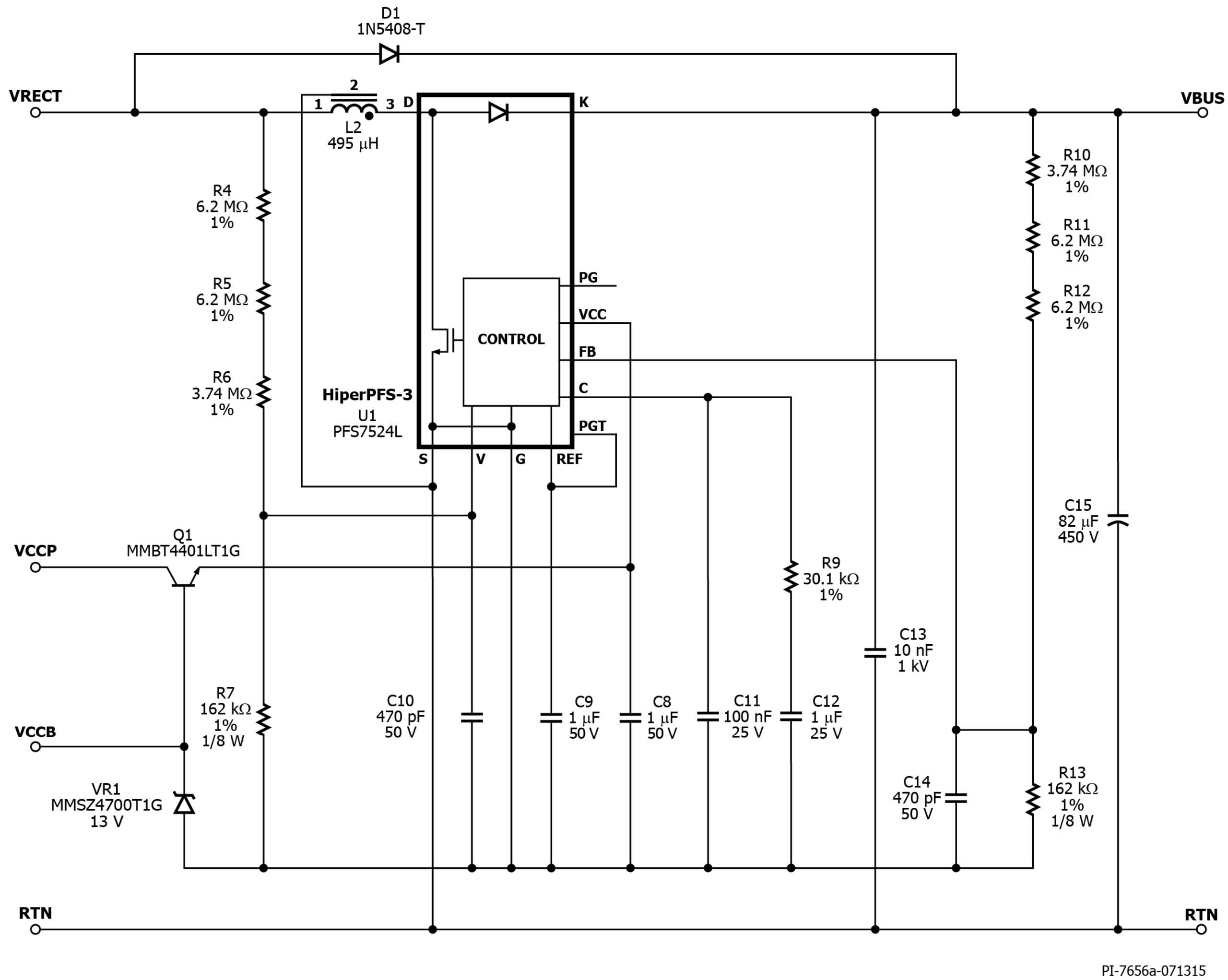

Figure 4 – Schematic. LCD TV Power Supply Application Circuit - PFC Section.

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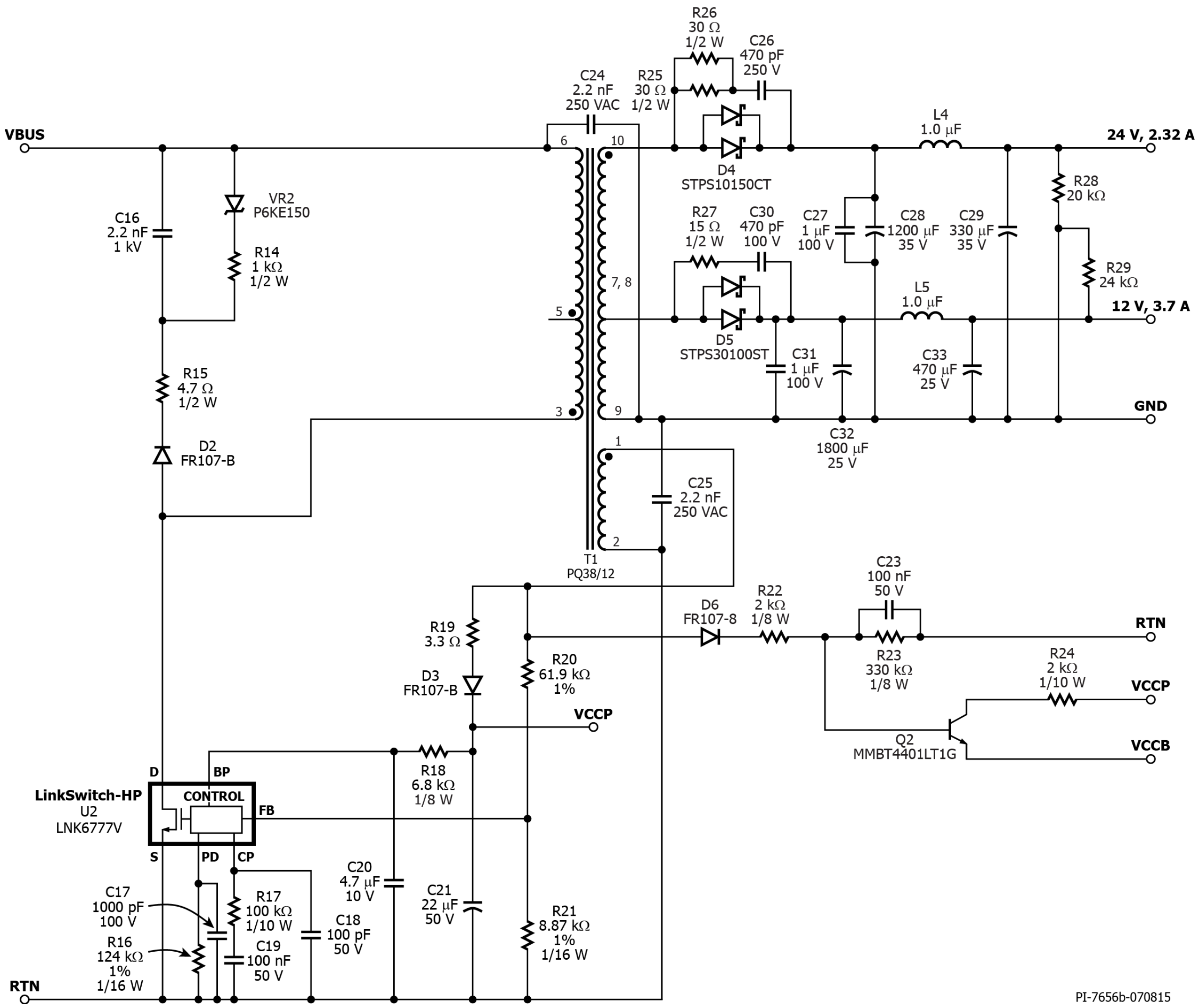

Figure 5 – Schematic DER-393 LCD TV Power Supply Application Circuit – DC/DC Section.

4 Circuit Description

The circuit shown in Figures 3, 4 and 5 utilizes the PFS7524L, the LNK6777V devices from Power Integrations in a 12/24 V, 100 W power factor corrected isolated flyback power supply intended to power a LCD TV power supply.

4.1 *Input EMI Filter and Rectifier (Figure 3)*

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, C4, C5 and C6 in conjunction with inductors L1 and L3, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitor C7 provides input decoupling charge storage to reduce input ripple current at the switching frequencies and harmonics.

Resistors R1, R2 and R3 are provided to discharge the EMI filter capacitors after line voltage has been removed from the circuit.

NTC thermistor RT1 limits inrush current of the supply when line voltage is first applied.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 *PFS7524L Boost Converter (Figure 4)*

The boost converter stage consists of the boost inductor L2 and the PFS7524L IC U1. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

During start-up, diode D1 provides an inrush current path to the output capacitor C15, bypassing the switching inductor L2 and switch U1 in order to prevent a resonant interaction between the switching inductor and output capacitor.

Capacitor C13 provides a short, high-frequency return path to RTN for improved EMI results and to reduce U1 MOSFET drain voltage overshoot during turn-off. Capacitor C8 decouples and bypasses the U1 VCC pin.

Capacitor C9 on the REF pin of U1 bypasses noise for the internal reference and also programs the output power for either full mode, 100% of rated power [C9 = 1 μF], as in this design, or efficiency mode, 80% [C9 = 0.1 μF] of rated power.

4.3 *PFC Input Feed Forward Sense Circuit*

The input voltage of the power supply is sensed by the IC U1 using resistors R4, R5, R6 and R7. The capacitor C10 bypasses the V pin on IC U1.

4.4 *PFC Output Feedback*

An output voltage resistive divider network consisting of resistors R10, R11, R12, and R13 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U1 setting the PFC output at 385 V. Capacitor C14 bypasses the U1 FB pin.

Resistor R9 and capacitor C12 provide the control loop dominant pole-zero combination. Capacitor C11 attenuates line frequency ripple.

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4.5 *PFC Turn-off Circuit*

By sensing the drain voltage/frequency of LinkSwitch-HP device, the PFC stage can be powered down during light load in order to meet light load efficiency requirements.

As the 12 V and/or 24 V loads increase, the voltage generated across winding 1-2 of transformer T1 increases. VCC will increase and eventually turn on the HiperPFS-3 IC when the voltage on C8 exceeds the device turn-on threshold. During no-load or light load conditions the circuit consisting of D6, R22, R23, C23, Q2 and R24 will keep the PFC stage in the off condition.

4.6 *LinkSwitch-HP Primary (Figure 5)*

The schematic in Figure 5 depicts a 12/24 V, dual-output, 100 W LinkSwitch-HP based flyback DC-DC converter implemented using the LNK6777V.

The LNK6777V device (U2) integrates an oscillator, error amplifier, multi-mode control circuit, start-up and protection circuitry, and a high-voltage power MOSFET all in one monolithic IC.

One side of the power transformer is connected to the high-voltage bus and the other side is connected to the DRAIN (D) pin of U2. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, which is set by the output of an internal error amplifier (COMPENSATION (CP) pin voltage), the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

Capacitor C20 (4.7 μF) connected to the BYPASS (BP) pin sets overvoltage protection (OVP) and over-temperature protection (OTP) to latching and the lost regulation protection to automatic restart (auto-restart) after a given off-period (typ. 1500 ms).

4.7 *Primary RZCD Clamp*

Diode D2, transient voltage suppressor VR2, capacitor C16, and resistors R14 and R15 form a RZCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is thereby limited to typically less than 540 V at 265 VAC input providing significant margin to the maximum 725 V drain voltage (BV_{DSS}) specification.

Transient voltage suppressor VR2 prevents capacitor C16 from fully discharging every switching cycle to reduce power consumption during standby operation.

4.8 *Output Rectification*

Output rectification of the 12 V output is provided by diode D5 and filtering is provided by capacitors C31 and C32, inductor L5 and capacitor C33. The snubber formed by R27 and C30 provides high frequency filtering for improved EMI.

Output rectification of the 24 V output is provided by diode D4 and filtering is provided by capacitors C27 and C28, inductor L4 and capacitor C29. The snubber formed by R25, R26 and C26 provides high frequency filtering for improved EMI.

4.9 External Current Limit Setting

The maximum cycle-by-cycle current limit is set by resistor R16 connected to the PROGRAM (PD) pin. A 124 kΩ resistor in the design sets the maximum current limit to 100% of the LNK6777V's default current limit.

4.10 Feedback and Compensation Network

The output voltage is sensed through the bias winding 1-2 of T1 and resistor divider (R20 and R21) during the flyback period. The sensed output voltage is compared to the FEEDBACK (FB) pin threshold to regulate the output or to stop switching in case an overvoltage condition is detected (OVP). This primary side regulation solution not only reduces the power supply cost, but also significantly improves the expected life as no optocoupler is necessary for power supplies designed with LinkSwitch-HP.

Voltage divider R20 and R21 is also used to indirectly monitor the bus voltage during the integrated power MOSFET on-time. At start-up, the IC enables switching only if the bus voltage has typically reached 100 V (brown-in threshold). If the bus voltage drops, for instance during a brown-out condition, below typically 40 V the device stops switching (brown-out protection). In case the bus voltage reaches excessive levels (e.g. caused by line surge) the device also stops switching. Additionally the cycle-by-cycle current limit is compensated over line to limit the available overload power. See the device datasheet for further details.

The voltage sensed at the FB pin produces a control voltage at the CP pin. Resistor R17 and capacitors C18 and C19 are used for control loop compensation. The operating peak primary current and the operating switching frequency are determined by the CP pin voltage.

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5 PCB Layout

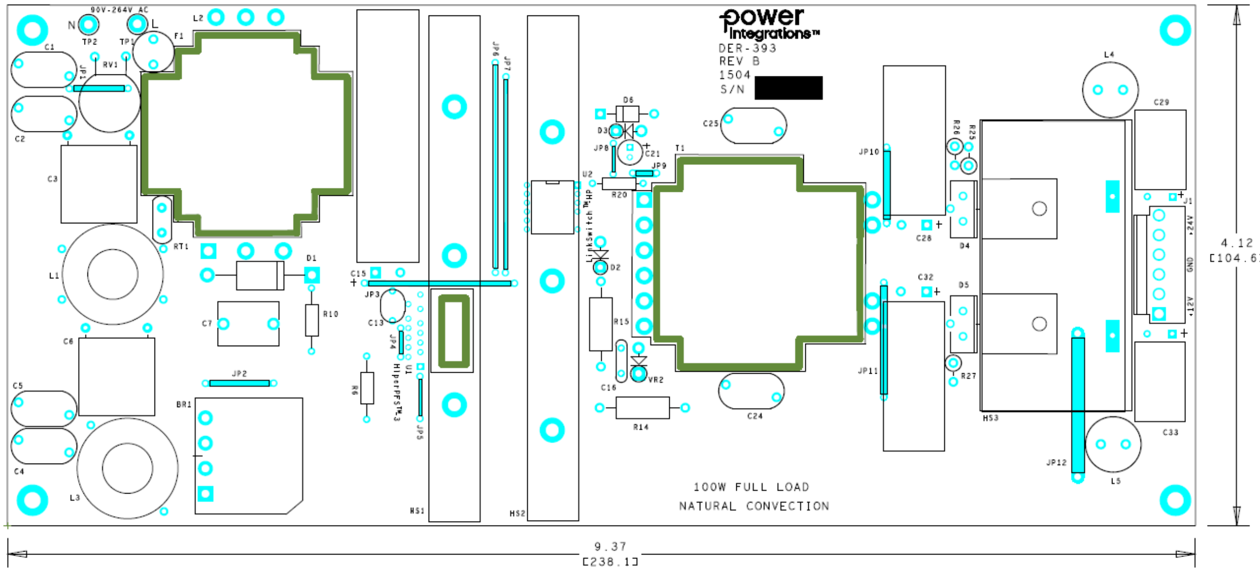

Figure 6 – Printed Circuit Layout – Top Side.

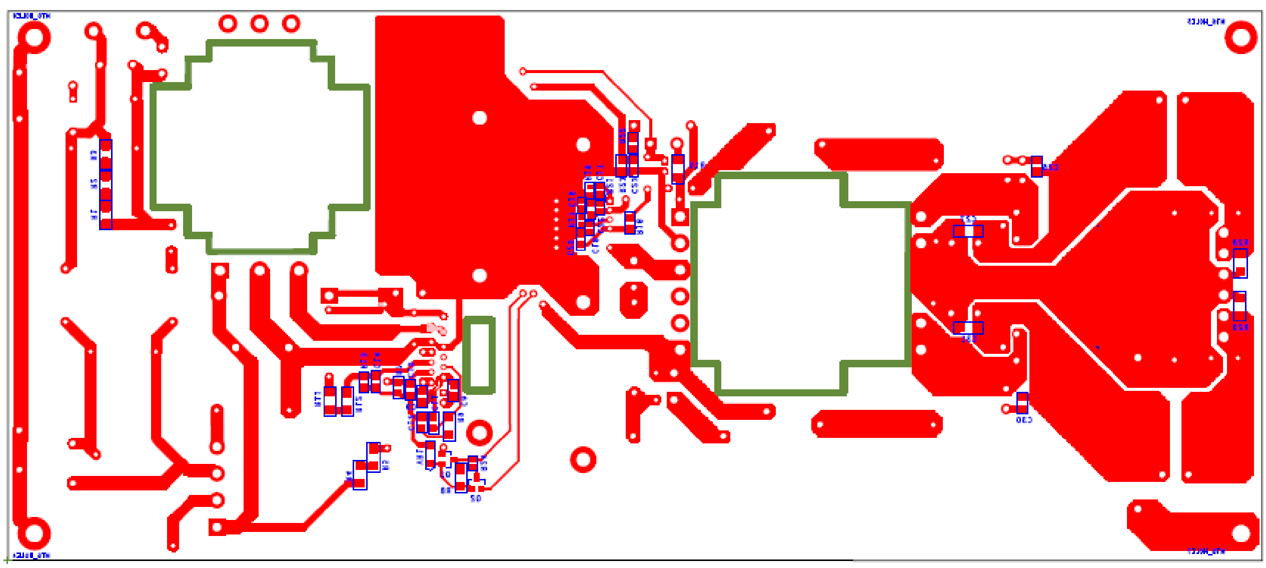

Figure 7 – Printed Circuit Layout – Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 6 A, Bridge Rectifier	RS605	Rectron Semi
2	2	C1 C2	1 nF, Ceramic, Y1	440LD10-R	Vishay
3	2	C3 C6	220 nF, 275VAC, Film, X2	LE224-M	OKAYA ELECT
4	4	C4 C5 C24 C25	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
5	1	C7	470 nF, 450 V, METALPOLYPRO	ECW-F2W474JAQ	Panasonic
6	2	C8 C9	1 μF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
7	2	C10 C14	470 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB471	Yageo
8	1	C11	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
9	1	C12	1 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
10	1	C13	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
11	1	C15	82 μF, 450 V, Electrolytic, (12.5 x 52)	UPZ2W820MNY9	
12	1	C16	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC Components
13	1	C17	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
14	1	C18	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
15	1	C19	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K	TDK
16	1	C20	4.7 μF, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
17	1	C21	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
18	1	C23	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
19	1	C26	470 pF, 250 V, Ceramic,GCM, 0805	GCM21A7U2E471JX01D	Murata
20	2	C27 C31	1 μF,100 V, Ceramic, X7R, 1206	HMK316B7105KL-T	Taiyo Yuden
21	1	C28	1200 μF, 35 V, Electrolytic, Low ESR, 25 mΩ, (12.5 x 30)	ELXZ350ELL122MK30S	Nippon Chemi-Con
22	1	C29	330 μF, 35 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE350ELL331MJ16S	Nippon Chemi-Con
23	1	C30	470 pF, 100 V, Ceramic, X7R, 0805	08051C471KAT2A	AVX
24	1	C32	1800 μF, 25 V, Electrolytic, Very Low ESR, 16 mΩ, (12.5 x 30)	EKZE250ELL182MK30S	Nippon Chemi-Con
25	1	C33	470 μF, 25 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE250ELL471MJ16S	Nippon Chemi-Con
26	1	D1	1000 V, 3 A, Rectifier, DO-201AD	1N5408-T	Diodes, Inc.
27	3	D2 D3 D6	1000 V, 1 A, Fast Recovery Diode, DO-41	FR107-B	Rectron
28	1	D4	150 V, 5 A, Dual Schotkky, TO-220AB	STPS10150CT	ST Micro
29	1	D5	100 V, 30 A, Schottky, TO-220AB	STPS30100ST	ST
30	1	F1	2 A,250 V, Slow, TR5	37212000411	Wickman
31	2	HS1 HS2	FAB, HEATSINK,PFS-LNKHP 110W		Custom
32	1	HS3	FAB, HEATSINK,PFS-LNKHP 100W		Custom
33	1	J1	CONN HEADER 6POS (1x6).156 VERT TIN	26-60-4060	Molex
34	1	JP1	Wire Jumper, Non insulated, 22 AWG, 0.5 in	298	Alpha
35	1	JP2	Wire Jumper, Insulated, #24 AWG, 0.6 in	C2003A-12-02	Gen Cable
36	1	JP3	Wire Jumper, Insulated, #24 AWG, 1.2 in	C2003A-12-02	Gen Cable
37	3	JP4 JP8 JP9	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
38	1	JP5	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
39	1	JP6	Wire Jumper, Insulated, #24 AWG, 1.7 in	C2003A-12-02	Gen Cable
40	1	JP7	Wire Jumper, Insulated, #24 AWG, 1.6 in	C2003A-12-02	Gen Cable
41	1	JP10	Wire Jumper, Insulated, #24 AWG, 0.7 in	C2003A-12-02	Gen Cable
42	1	JP11	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable
43	1	JP12	Wire Jumper, Insulated, TFE, #18 AWG, 1.2 in	C2052A-12-02	Alpha
44	1	L1	10 mH, Common Mode Choke		Custom
45	1	L2	Bobbin, PQ38, Vertical, 6pins	BQ35/35-1112CPFR	Pin Shine
46	1	L3	470 μH, 1.6A, Vertical Toroidal	2120-V-RC	Bourns
47	2	L4 L5	1.0 μH, 5 A, Radial	TSL0709RA-1R0M5R0-PF	TDK

48	4	MTG_HOLE4 MTG_HOLE5 MTG_HOLE6 MTG_HOLE7	Mounting Hole No 4		
49	2	Q1 Q2	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
50	3	R1 R2 R3	620 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ624V	Panasonic
51	4	R4 R5 R11 R12	6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
52	2	R6 R10	3.74 MΩ, 1%, 1/4 W, Metal Film	MFR-25FBF52-3M74	Yageo
53	2	R7 R13	162 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1623V	Panasonic
54	1	R9	30.1 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3012V	Panasonic
55	1	R14	1 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-1K0	Yageo
56	1	R15	4.7 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-4R7	Yageo
57	1	R16	124 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1243V	Panasonic
58	1	R17	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
59	1	R18	6.8 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ682V	Panasonic
60	1	R19	3.3 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ3R3V	Panasonic
61	1	R20	61.9 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-61K9	Yageo
62	1	R21	8.87 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF8871V	Panasonic
63	1	R22	2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ202V	Panasonic
64	1	R23	330 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ334V	Panasonic
65	1	R24	2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ202V	Panasonic
66	2	R25 R26	30 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-30R	Yageo
67	1	R27	15 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-15R	Yageo
68	1	R28	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
69	1	R29	24 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ243V	Panasonic
70	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
71	1	RTV2	Thermally conductive Silicone Grease	120-SA	Wakefield
72	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
73	6	SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
74	4	STDOFF1 STDOFF2 STDOFF3 STDOFF4	Standoff Hex, 4-40, 0.375" L, Al, F/F	1892	Keystone
75	1	T1	Bobbin, Vertical, 10 pins		
76	2	TO-220 PAD1 TO-220 PAD2	THERMAL PAD, BER103, 0.009" Thk, TO-220	SP600-54	Bergquist
77	1	TP1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
78	1	TP2	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
79	1	U1	HiperPFS-3, L-Bend eSIP	PFS7524L	Power Integrations
80	1	U2	LinkSwitch-HP, eDIP-12P	LNK6777V	Power Integrations
81	1	VR1	13 V, 5%, 500 Mw, SOD-123	MMSZ4700T1G	ON Semi
82	1	VR2	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	LittleFuse
83	2	WASHER1 WASHER2	Washer Nylon Shoulder #4	3049	Keystone
84	4	WASHER3 WASHER4 WASHER5 WASHER6	WASHER FLAT #4 SS	FWSS 004	Building Fasteners

7 HiperPFS-3 Design Spreadsheet

Hiper_PFS-3_Boost_012815; Rev.0.6; Copyright Power Integrations 2015	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Hiper_PFS-3_Boost_012815_Rev0-6.xls; Continuous Mode Boost Converter Design Spreadsheet**
Enter Application Variables					
Input Voltage Range	**Universal**		**Universal**		Input voltage range
VACMIN	90		90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other voltages, enter here, but enter fixed value for LPFC_ACTUAL.
VACMAX	264		264	VAC	Maximum AC input voltage
VBROWNIN			76	VAC	Expected Minimum Brown-in Voltage
VBROWNOUT			72	VAC	Specify brownout voltage.
VO			385	VDC	Nominal load voltage
PO	110		110	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	°C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
VO_MIN			366	VDC	Minimum Output voltage
VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
tHOLDUP			20	ms	Holdup time
VHOLDUP_MIN	300		300	VDC	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**No**		**No**		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core auto pick core size
KP and INDUCTANCE					
KP_TARGET	0.720		0.720		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
LPFC_TARGET (0 bias)			496	uH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
LPFC_DESIRED (0 bias)	495		495	uH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
KP_ACTUAL			0.696		Actual KP calculated from LPFC_ACTUAL
LPFC_PEAK			495	uH	Inductance at VACMIN, 90°. For Ferrite, same as LPFC_DESIRED (0 bias)
Basic current parameters					
IAC_RMS			1.31	A	AC input RMS current at VACMIN and Full Power load
IO_DC			0.29	A	Output average current/Average diode current
PFS Parameters					
PFS Part Number	**PFS7524L**		**PFS7524L**		If examining brownout operation, over-ride auto pick with desired device size
Operating Mode	**Full Power**		**Full Power**		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
IOCP min			4.5	A	Minimum Current limit
IOCP typ			4.8	A	Typical current limit
IOCP max			5.1	A	Maximum current limit
IP			2.74	A	MOSFET peak current
IRMS			1.16	A	PFS MOSFET RMS current
RDSON			0.92	Ohms	Typical RDSon at 100 'C

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FS_PK			82	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			61	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
PCOND_LOSS_PFS			1.2	W	Estimated PFS conduction losses
PSW_LOSS_PFS			1.2	W	Estimated PFS switching losses
PFS_TOTAL			2.5	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			17.00	°C/W	Maximum thermal resistance of heatsink
INDUCTOR DESIGN					
Basic Inductor Parameters					
LPFC (0 Bias)			495	uH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
IL_RMS			1.35	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
Material and Dimensions					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	**PC44/PC95**		**PC44/PC95**		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
Core Geometry	**PQ**		**PQ**		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
Core	**Auto**		**PQ26/20**		Core part number
Ae	129.70		129.70	mm^2	Core cross sectional area
Le	43.50		43.50	mm	Core mean path length
AL	4000.00		4000.00	nH/t^2	Core AL value
Ve	5.64		5.64	cm^3	Core volume
HT (EE/PQ) / ID (toroid)	7.50		7.50	mm	Core height/Height of window; ID if toroid
MLT	7.3		7.3	mm	Mean length per turn
BW	4.70		4.70	mm	Bobbin width
LG			0.99	mm	Gap length (Ferrite cores only)
Flux and MMF calculations					
BP_TARGET (ferrite only)	3550		3550	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
B_OCP (or BP)			3524	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
B_MAX			1911	Gauss	peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance
µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
µ_MAX (powder only)			N/A	%	mu_max greater than 75% indicates a very large core. Please verify
µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
I_TEST			4.8	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
B_TEST			3316	Gauss	Flux density at I_TEST and maximum tolerance inductance
µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
Wire					
TURNS			58		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
ILRMS			1.35	A	Inductor RMS current
Wire type	**Litz**		**Litz**		Select between "Litz" or "Magnet" for double

					coated magnet wire
AWG	40	Info	40	AWG	!!! Info. Selected wire gauge is too thick and may cause increased losses due to skin effect. Consider using multiple strands of thinner wires or Litz wire
Filar	40		40		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
OD (per strand)			0.079	mm	Outer diameter of single strand of wire
OD bundle (Litz only)			0.70	mm	Will be different than OD if Litz
DCR			0.50	ohm	Choke DC Resistance
P AC Resistance Ratio			1.71		Ratio of total Cu loss including HF ACR loss vs. assuming only DCR (uses Dowell equations)
J		Warning	6.93	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
FIT			80%	%	Percentage fill of winding window for EE/PQ core. Full window approx. 90%
Layers			7.74		Estimated layers in winding
Loss calculations					
BAC-p-p			1379	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
LPFC_CORE_LOSS			0.27	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			1.55	W	Estimated Inductor copper losses
LPFC_TOTAL_LOSS			1.82	W	Total estimated Inductor Losses
Built-in PFC Diode					
PFC Diode Part Number			INTERNAL1		PFC Diode Part Number
Type			SPECIAL		PFD Diode Type
Manufacturer			PI		Diode Manufacturer
VRRM			530	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
Qrr			57		high temperature
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			0.42	W	Estimated Diode conduction losses
PSW_DIODE			0.14	W	Estimated Diode switching losses
P_DIODE			0.56	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			17.00	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
Output Capacitor	**82**		82	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			11.9	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			19.4	ms	Expected holdup time with selected Output capacitor
ESR_LF			1.66	ohms	Low Frequency Capacitor ESR
ESR_HF			0.66	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.19	A	Low Frequency Capacitor RMS current
IC_RMS_HF			0.53	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.06	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.18	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.25	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
I^2t Rating			5.72	A^2*s	Minimum I^2t rating for fuse
Fuse Current rating			1.95	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			1.21	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			373	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			2.13	W	Estimated Bridge Diode conduction loss
CIN			0.3	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating

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RT			9.33	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
PFS3 small signal components					
C_REF			1.0	uF	REF pin capacitor value
RV1			4.0	MOhms	Line sense resistor 1
RV2			6.0	MOhms	Line sense resistor 2
RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
C_VCC			1.0	uF	Supply decoupling capacitor
C_C			100	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
PGT set resistor			333.0	kohm	Power good threshold setting resistor
Feedback Components					
R1			4.0	Mohms	Feedback network, first high voltage divider resistor
R2			6.0	Mohms	Feedback network, second high voltage divider resistor
R3			6.0	Mohms	Feedback network, third high voltage divider resistor
R4			161.6	kohms	Feedback network, lower divider resistor
C1			0.495	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
R5			29.4	kohms	Feedback network: zero setting resistor
C2			1000	nF	Feedback component- noise suppression capacitor
Loss Budget (Estimated at VACMIN)					
PFS Losses			2.47	W	Total estimated losses in PFS
Boost diode Losses			0.56	W	Total estimated losses in Output Diode
Input Bridge losses			2.13	W	Total estimated losses in input bridge module
Inductor losses			1.82	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.25	W	Total estimated losses in Output capacitor
EMI choke copper loss			0.50	W	Total estimated losses in EMI choke copper
Total losses			7.23	W	Overall loss estimate
Efficiency			0.94		Estimated efficiency at VACMIN, full load.
CAPZero component selection recommendation					
CAPZero Device			CAP002DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
Total Series Resistance (R1+R2)			1.5	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN_RECOMMENDED	470		470	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2	220		220	nF	X capacitor after differential mode choke and before bridge, ratio with Po
LDM_calc			367	uH	estimated minimum differential inductance to avoid <10kHz resonance in input current
CX1	220		220	nF	X capacitor before common mode choke, ratio with Po
LCM			10	mH	typical common mode choke value
LCM_leakage			30	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
LDM_Actual			337	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.

DCR_LCM	0.10		0.10	Ohms	total DCR of CM choke for estimating copper loss
DCR_LDM	0.10		0.10	Ohms	total DCR of DM choke(or CM #2) for estimating copper loss

Note:
The Inductor design uses a PQ38/13 core. The core parameters were manually added in the core materials and dimensions section.

If the current density is higher than 6 A / mm^2 a “warning” will be generated. Selection of a higher cross section wire should be made based on thermal test results. With sufficient cooling, higher current densities can be acceptable.

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8 Transformer Design Spreadsheet

ACDC_LinkSwitch-HP_101714; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchHP_101714 Rev 2-0.xls: LinkSwitch-HP Flyback Continuous/Discontinuous Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	220		220	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC Input Voltage
fL	50		50	Hz	AC Mains Frequency
VO	12		12	V	Output Voltage (main)
PO	100	**Info**	100	W	Maximum power limit for selected enclosure reached
n	0.90		0.90		Efficiency Estimate
Z			0.50		Loss Allocation Factor
VB	16		16	V	Bias Voltage
tC			3	ms	Bridge Rectifier Conduction Time Estimate
CIN			100	uF	Input Filter Capacitor
Package					
Enclosure	**Open Frame**		Open Frame		Open Frame type enclosure
Heatsink	**Metal**		Metal		
ENTER LinkSwitch-HP VARIABLES					
LinkSwitch-HP	**LNK6777V**		**LNK6777V**		
ILIMITMIN			2.418	A	Minimum Current limit
ILIMITMAX			2.782	A	Maximum current limit
ILIMITMIN_EXT			2.418	A	External Minimum Current limit
ILIMITMAX_EXT			2.782	A	External Maximum current limit
KI	**1**		1.000		Current limit reduction factor
Rpd			124.00	k-ohm	Program delay Resistor
Cpd			33.00	nF	Program delay Capacitor
Total programmed delay			0.86	sec	Total program delay
fS			132	kHz	LinkSwitch-HP Switching Frequency
fSmin			120	kHz	LinkSwitch-HP Minimum Switching Frequency
fSmax			136	kHz	LinkSwitch-HP Maximum Switching Frequency
KP	0.73		0.73		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	108.90		108.90	V	Reflected Output Voltage
Voltage Sense					
VUVON			313.54	V	Undervoltage turn on
VUVOFF			127.07	V	Undervoltage turn off
VOV			1434.85	V	Overvoltage threshold
FMAX_FULL_LOAD			136.00	kHz	Maximum switching frequency at full load
FMIN_FULL_LOAD			120.00	kHz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD			5.31	us	Minimum available Diode conduction time at full load. This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD			2.16	us	Minimum available Diode conduction time at light load. This should be greater than 1.4 us
VDS			2.52	V	LinkSwitch-HP on-state Drain to Source Voltage.
VD			0.50	V	Output Winding Diode Forward Voltage Drop
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
FEEDBACK SENSING SECTION					
RFB1			191.00	k-ohms	Feedback divider upper resistor
RFB2			26.10	k-ohms	Feedback divider lower resistor
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Select Core Size	**Custom**	Info	Custom		Manual Core Selected

Core			Custom		Selected Core
Custom Core					Enter name of custom core is applicable
AE	1.29		1.29	cm^2	Core Effective Cross Sectional Area
LE	4.35		4.35	cm	Core Effective Path Length
AL	4000		4000	nH/T^2	Ungapped Core Effective Inductance
BW	4.5		4.5	mm	Bobbin Physical Winding Width
M	0.00		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3		Number of Primary Layers
NS	3		3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			285	V	Minimum DC Input Voltage
VMAX	385		385	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.28		Maximum Duty Cycle
IAVG			0.39	A	Average Primary Current
IP			2.21	A	Peak Primary Current
IR			1.61	A	Primary Ripple Current
IRMS			0.78	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_TYP			410	uH	Typical Primary Inductance
LP_TOL	5		5	%	Primary inductance Tolerance
NP			26		Primary Winding Number of Turns
NB			4		Bias Winding Number of Turns
ALG			601	nH/T^2	Gapped Core Effective Inductance
BM			2685	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3555	Gauss	Peak Flux Density (BP<3700)
BAC			980	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1073		Relative Permeability of Ungapped Core
LG			0.23	mm	Gap Length (Lg > 0.1 mm)
BWE			13.5	mm	Effective Bobbin Width
OD			0.52	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.45	mm	Bare conductor diameter
AWG			26	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			256	Cmils	Bare conductor effective area in circular mils
CMA			329	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			19.22	A	Peak Secondary Current
ISRMS			10.93	A	Secondary RMS Current
IO			8.33	A	Power Supply Output Current
IRIPPLE			7.07	A	Output Capacitor RMS Ripple Current
CMS			2185	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			16	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			1.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.50	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.10	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			634	V	Peak voltage across drain to source of Linkswitch-HP
PIVS			56	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB			75	V	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					

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VO1	12.00		12.00	V	Output Voltage
IO1	3.70		3.70	A	Output DC Current
PO1			44.40	W	Output Power
VD1			0.5	V	Output Diode Forward Voltage Drop
NS1			3.00		Output Winding Number of Turns
ISRMS1			4.851	A	Output Winding RMS Current
IRIPPLE1			3.14	A	Output Capacitor RMS Ripple Current
PIVS1			56	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1			970	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			20	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.81	mm	Minimum Bare Conductor Diameter
ODS1			1.50	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2	24.00		24.00	V	Output Voltage
IO2	2.32		2.32	A	Output DC Current
PO2			55.68	W	Output Power
VD2			0.7	V	Output Diode Forward Voltage Drop
NS2			5.93		Output Winding Number of Turns
ISRMS2			3.042	A	Output Winding RMS Current
IRIPPLE2			1.97	A	Output Capacitor RMS Ripple Current
PIVS2			111	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2			608	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			0.65	mm	Minimum Bare Conductor Diameter
ODS2			0.76	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3			0.00	V	Output Voltage
IO3			0.00	A	Output DC Current
PO3			0.00	W	Output Power
VD3			0.7	V	Output Diode Forward Voltage Drop
NS3			0.17		Output Winding Number of Turns
ISRMS3			0.000	A	Output Winding RMS Current
IRIPPLE3			0.00	A	Output Capacitor RMS Ripple Current
PIVS3			2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			100.08	W	!!! Warning: total output power not equal to PO (PO= 100 W)
Negative Output	N/A		N/A		If negative output exists enter Output number; e.g.: If VO2 is negative output, select 2
Note: Power Supply can only support 90 W at start-up.					

9 Magnetics

9.1 Common Mode Choke Specification

9.1.1 Electrical Diagram

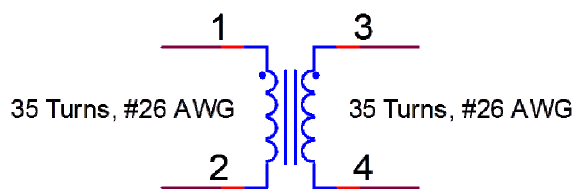

Figure 8 – Common Mode Choke Electrical Diagram.

9.1.2 Electrical Specifications

Inductance	Pins 1-2, 3-4 measured at 10 kHz.	10 mH, ±25%

9.1.3 Materials

Item	Description
[1]	Core: JL15 (JLW ELECTRONICS (HONG KONG) LIMITED). AL = 9000 nH/N2. Mfg. P/N: T18x10x7C-JL15*.
[2]	Divider - Fish paper, insulating cotton rag, 0.010” thick. Cut to size 0.383”x0.293”.
[3]	Magnetic Wire: #26 AWG.
[4]	Number of Turns: 35 each section.

*T18x10x7C is the physical size, JL15 is the core type

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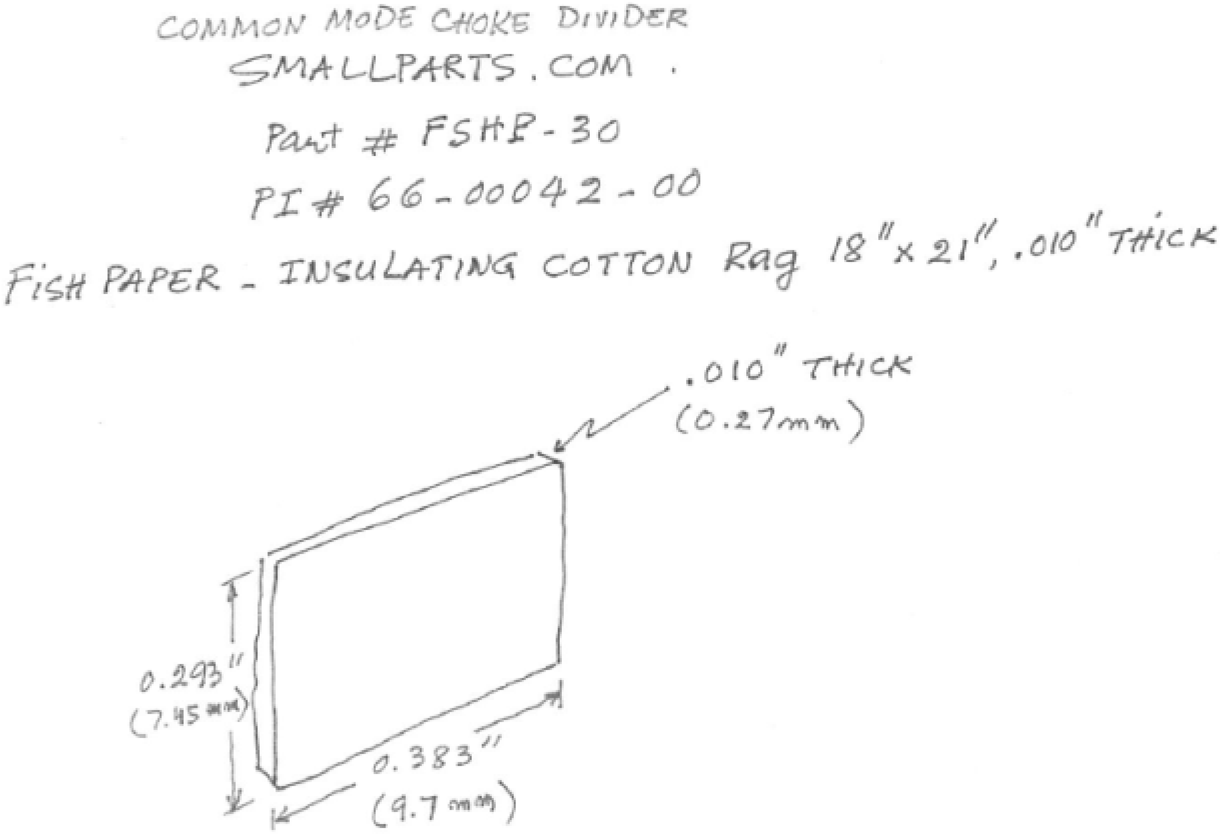
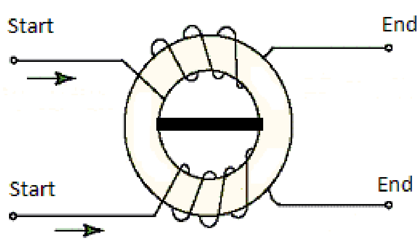
9.1.4 Winding Instruction

1. Insert the divider (see details below) in the core to divide it into 2 sections equally.



2. Start winding on one section with 28 turns or completely fill up the section for the 1st layer, then equally spread the remaining turns for the 2nd layer.

3. Repeat step 2 for the other section winding. Make sure it starts from the SAME side and winding direction as step 2. See picture below.



9.2 PFC Choke Specification

9.2.1 Electrical Diagram

58T, 40 x 40 Served Litz

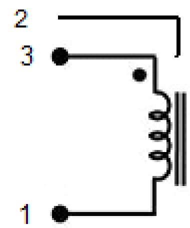


Figure 9 – PFC Choke Electrical Diagram.

9.2.2 Electrical Specifications

Inductance	Pins 1-3 measured at 100 kHz, 0.4 RMS.	495 µH +5%

9.2.3 Materials

Item	Description
[1]	Core: TDG Core, PC40 ±25%.
[2]	Bobbin: PQ38, from TDG. P/N: PQ38/13.
[3]	Wire: Served Litz 40/40.
[4]	Tape, Polyester Web 3M, 4.5 mm wide, 5 mil thick.
[5]	Bus Wire, #24 AWG (connect to pin 2).
[6]	Varnish: Dolph BC-359 or equivalent.

9.2.4 Inductor Construction

Winding preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 1, wind 58 turns of served Litz wire item [3], finish at pin 3.
Insulation	Apply 3 layers of tape item [4].
Assembly	Grind both cores to specified inductance.
Final Assembly	Solder a wire of item [5] at pin 2, and then attach the other end of the wire to the bottom side of the core. Secure the wire and the core halves with tape. Varnish [6].

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9.3 *Transformer Specification*

9.3.1 Electrical Diagram

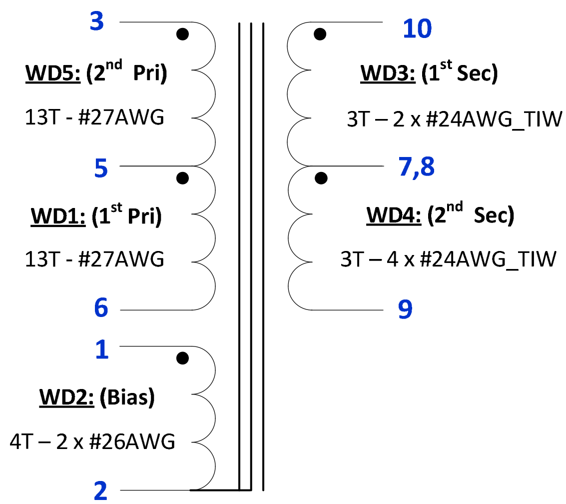

Figure 10 – Transformer Electrical Diagram.

9.3.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3-6 and pins 7-10.	3000 VAC
Primary Inductance	Pins 3-6, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	410 ±5%
Resonant Frequency	Pins 3-6, all other windings open.	2500 kHz (Min.)
Primary Leakage Inductance	Pins 3-6, with leads 7-10 shorted, measured at 100 kHz, 0.4 V_{RMS}.	5 μH (Max.)

9.3.3 Materials List

Item	Description
[1]	Core: TDKPC40-PQ38/12 and gapped ALG 606 nH/T^2.
[2]	Bobbin: PQ38/12-Vertical, 10pins (6/4), PI#: 25-01035-00; or equivalent.
[3]	Magnet Wire: #27 AWG, Solderable Double Coated.
[4]	Magnet Wire: #26 AWG, Solderable Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 5.0 mm wide, 2.0 mils thick.
[7]	Bus Bare Wire: #24 AWG, Belden Electronics Division.
[8]	Varnish: Dolph BC-359 or equivalent.

9.3.4 Transformer Build Diagram

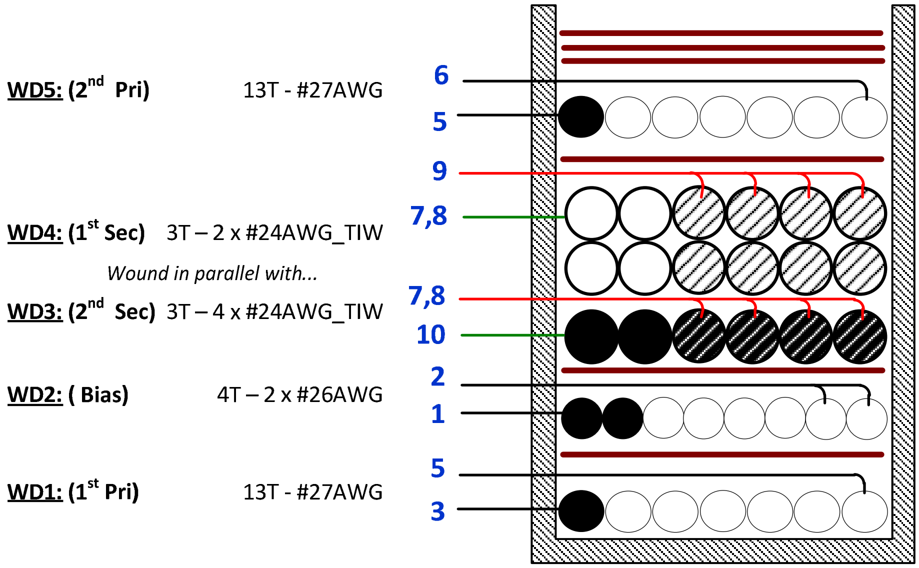

Figure 11 – Transformer Build Diagram.

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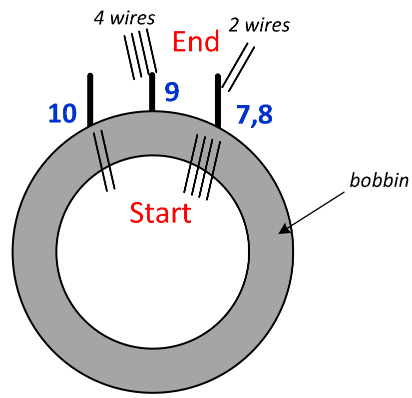


Figure 12 – Shows Wire Terminations for Secondary Winding.

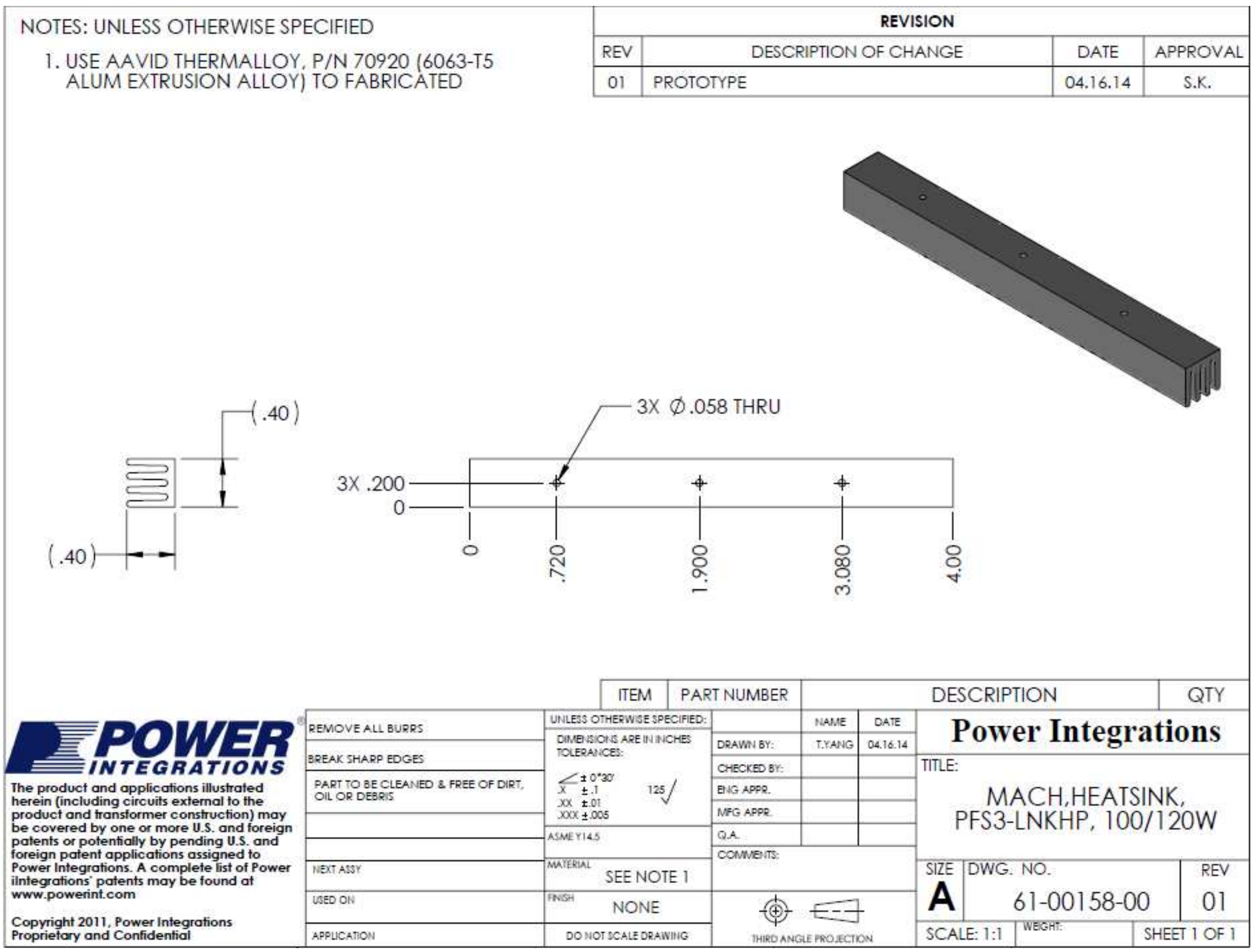
9.3.5 Transformer Build Instructions

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction. Note: Primary pin-pitch is wider than secondary, see picture below.
WD1 1st Primary	Start at pin 3, wind 13turns of wire item [3] in 1 layer with tight tension, and finish at pin 5.
Insulation	Place 1 layer of tape item [6].
WD2 1st Bias	Start at pin 1, wind 4 bi-filar turns of wire item [4] in 1 layer with tight tension, and end with pin 2.
Insulation	Place 1 layer of tape item [6].
WD3 & WD4 1st Secondary & 2nd Secondary	These 2 windings are going to be wound at same time and in parallel. Use 2 wires item [5], start at pin 10 for WD3, and 4 wires also item [5] start at pin 7, 8 (2 wires for each pin) for WD4. Wind 3 turns in parallel, finish 2 wires at pin 7, 8 (1 wire for each pin) for WD3, and finish 4 wires at pin 9 for WD4. (See fig. 3 above for reference for easier when terminating wires to pins).
Insulation	Place 1 layer of tape item [6].
WD5 2nd Primary	Start at pin 5, wind 13turns of wire item [3] in 1 layer with tight tension, and finish at pin 6.
Final Assembly	Connect pin 2 to core halves with wire item [7]. Grind, assemble, and secure core halves with tape. Vanish item [8].

10 Heat Sink Assemblies

10.1 HiperPFS-3 and LinkSwitch-HP Heat Sink

10.1.1 HiperPFS-3 and LinkSwitch-HP Heat Sink Fabrication Drawing



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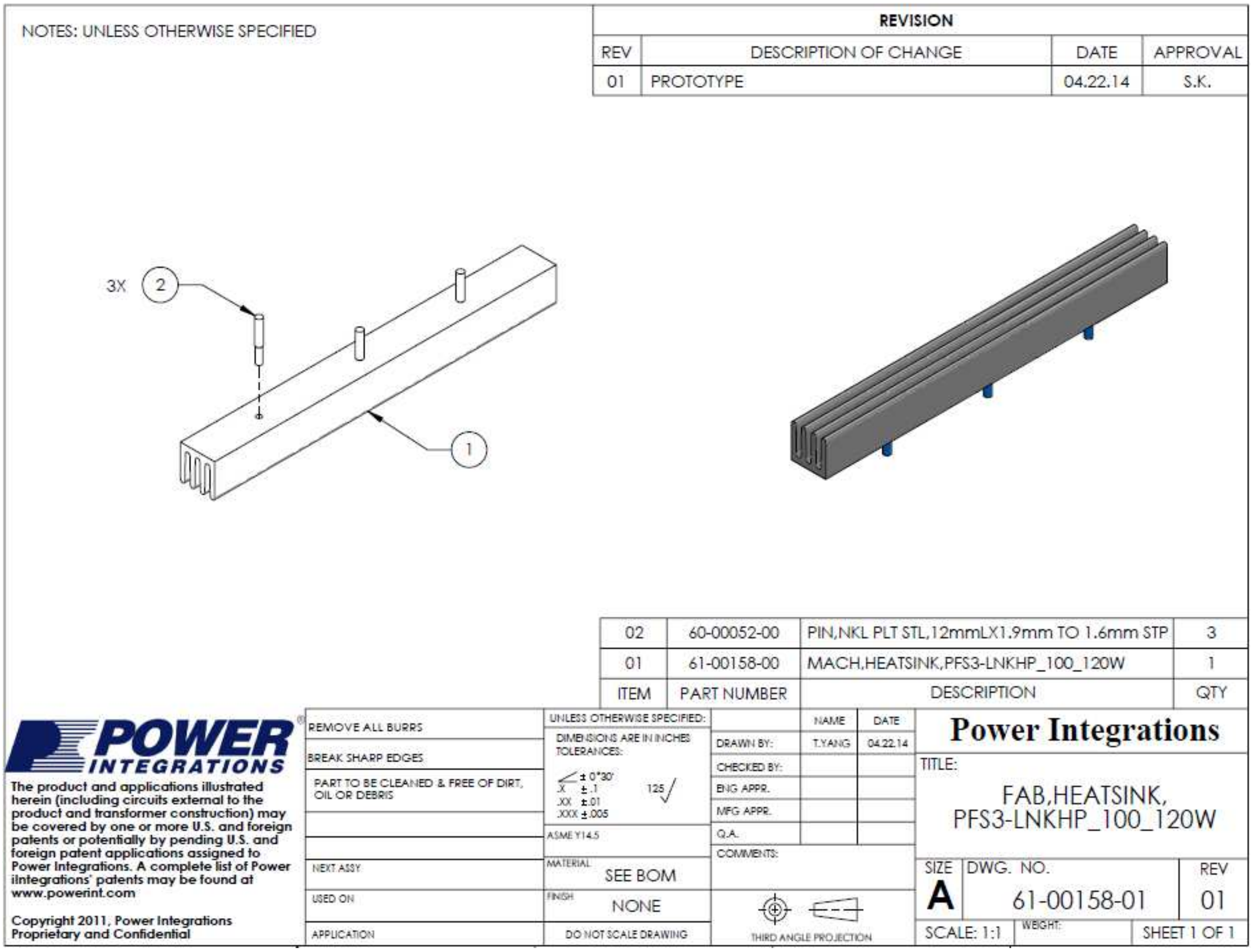
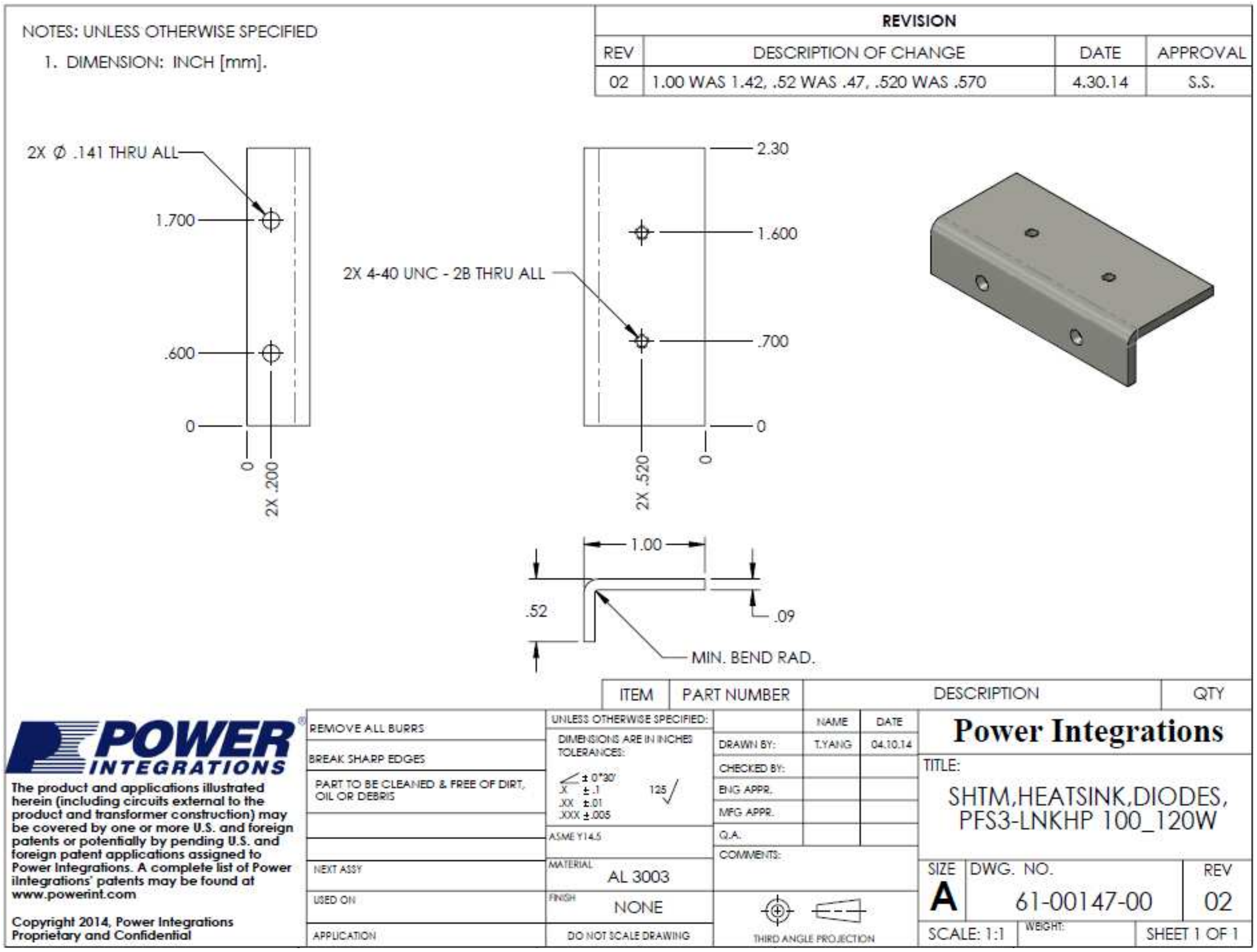
10.1.2 HiperPFS-3 and LinkSwitch-HP Heat Sink Assembly Drawing

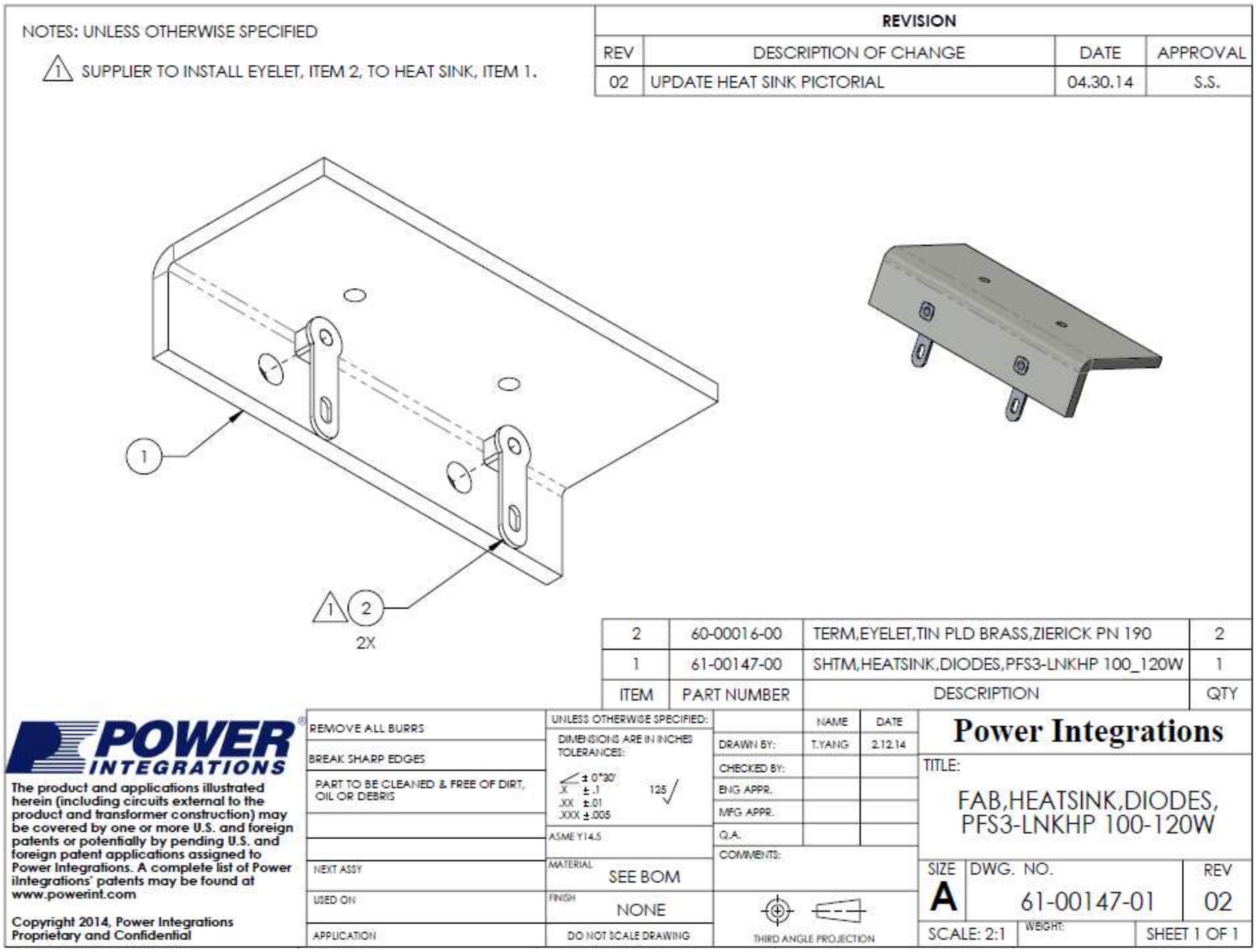


10.2 *Diode Heat Sink*

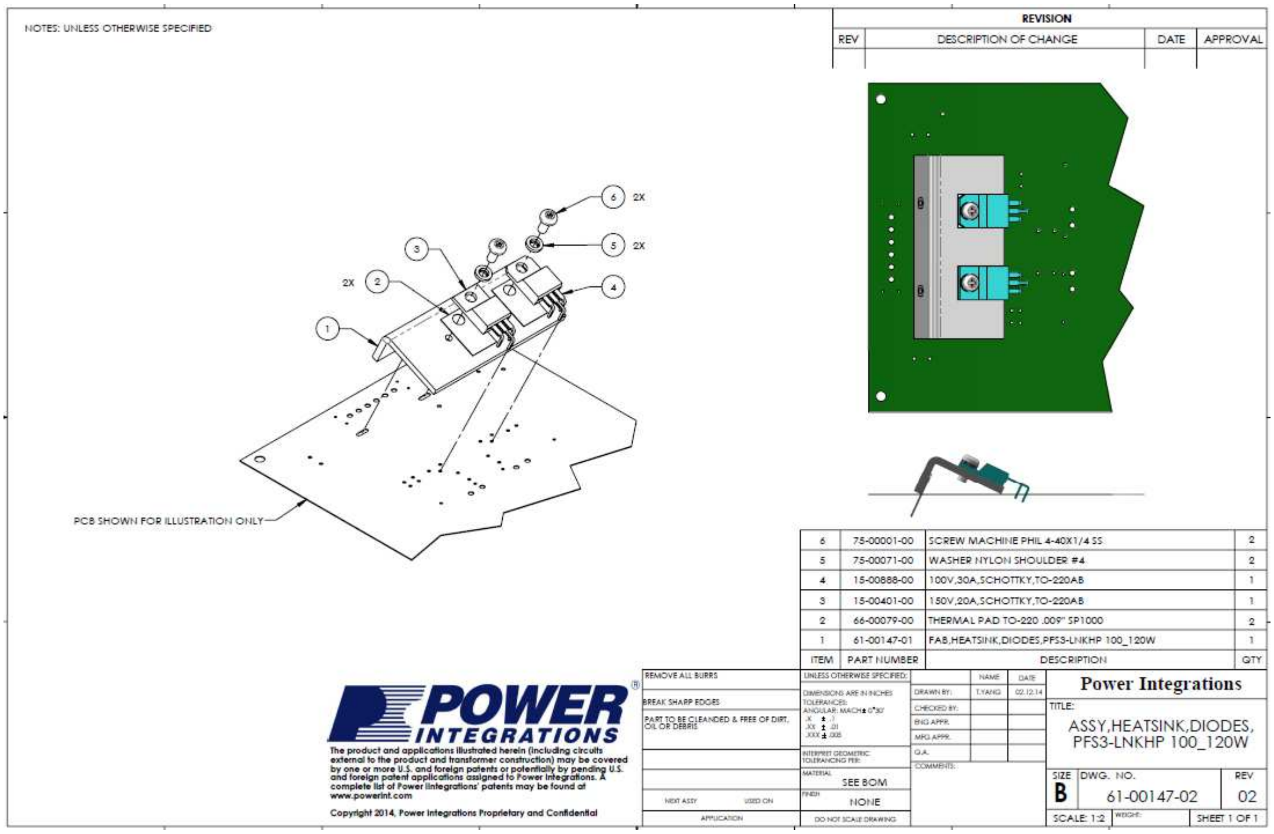
10.2.1 Diode Heat Sink Fabrication Drawing



10.2.2 Diode Heat Sink Assembly Drawing



10.2.3 Diode and Heat Sink Assembly Drawing



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11 Performance Data

All measurements were taken at room temperature and 50/60 Hz input frequency unless otherwise specified, Output voltage measurements were taken at the output connectors.

11.1 Output Regulation

Table below shows the output regulation w.r.t line and load variations. AC input was supplied using a sine wave source.

V_{IN} (VAC)	P_{IN} (W)	12 V (V)	12 I (A)	24 V (V)	24 I (A)	P_{OUT} (W)	Efficiency (%)	12 V Regulation (%)	24 V Regulation (%)
90	0.07	12.252	0	24.42	0	0	0.00	2.10	1.75
	7.42	12.235	0.0374	24.16	0.2325	6.074789	81.87	1.96	0.67
	6.258	11.952	0.3704	25.49	0.0234	5.023487	80.27	-0.40	6.21
	58.87	11.897	3.701	25.56	0.2322	49.96583	84.87	-0.86	6.50
	69.93	12.067	0.3701	23.83	2.321	59.77543	85.48	0.56	-0.71
	117.84	11.82	3.701	23.99	2.321	99.42661	84.37	-1.50	-0.04
115	0.077	12.223	0	24.41	0	0	0.00	1.86	1.71
	7.37	12.247	0.0374	24.17	0.2322	6.070312	82.37	2.06	0.71
	6.257	11.953	0.37	25.48	0.0232	5.013746	80.13	-0.39	6.17
	57.81	11.855	3.701	25.5	0.2322	49.79646	86.14	-1.21	6.25
	68.96	12.065	0.3703	23.82	2.322	59.77771	86.68	0.54	-0.75
	115.26	11.82	3.7	23.99	2.321	99.41479	86.25	-1.50	-0.04
230	0.135	12.227	0	24.39	0	0	0.00	1.89	1.63
	7.874	12.255	0.0371	24.14	0.2322	6.059969	76.96	2.13	0.58
	6.52	11.95	0.3701	25.49	0.0233	5.016612	76.94	-0.42	6.21
	57.11	11.872	3.702	25.52	0.2322	49.87589	87.33	-1.07	6.33
	67.81	12.062	0.37	23.82	2.32	59.72534	88.08	0.52	-0.75
	112.75	11.823	3.702	23.99	2.323	99.49752	88.25	-1.48	-0.04
264	0.16	12.229	0	24.39	0	0	0.00	1.91	1.63
	7.624	12.24	0.0371	24.16	0.2322	6.064056	79.54	2.00	0.67
	6.427	11.951	0.3701	25.47	0.0235	5.02161	78.13	-0.41	6.12
	57.174	11.894	3.703	25.56	0.2321	49.97596	87.41	-0.88	6.50
	67.8	12.074	0.3706	23.85	2.324	59.90202	88.35	0.62	-0.62
	112.46	11.823	3.703	23.99	2.321	99.46136	88.44	-1.48	-0.04

11.2 System Efficiency

Figures below show the total supply efficiency (PFC and LinkSwitch-HP stages). AC input was supplied using a sine wave source.

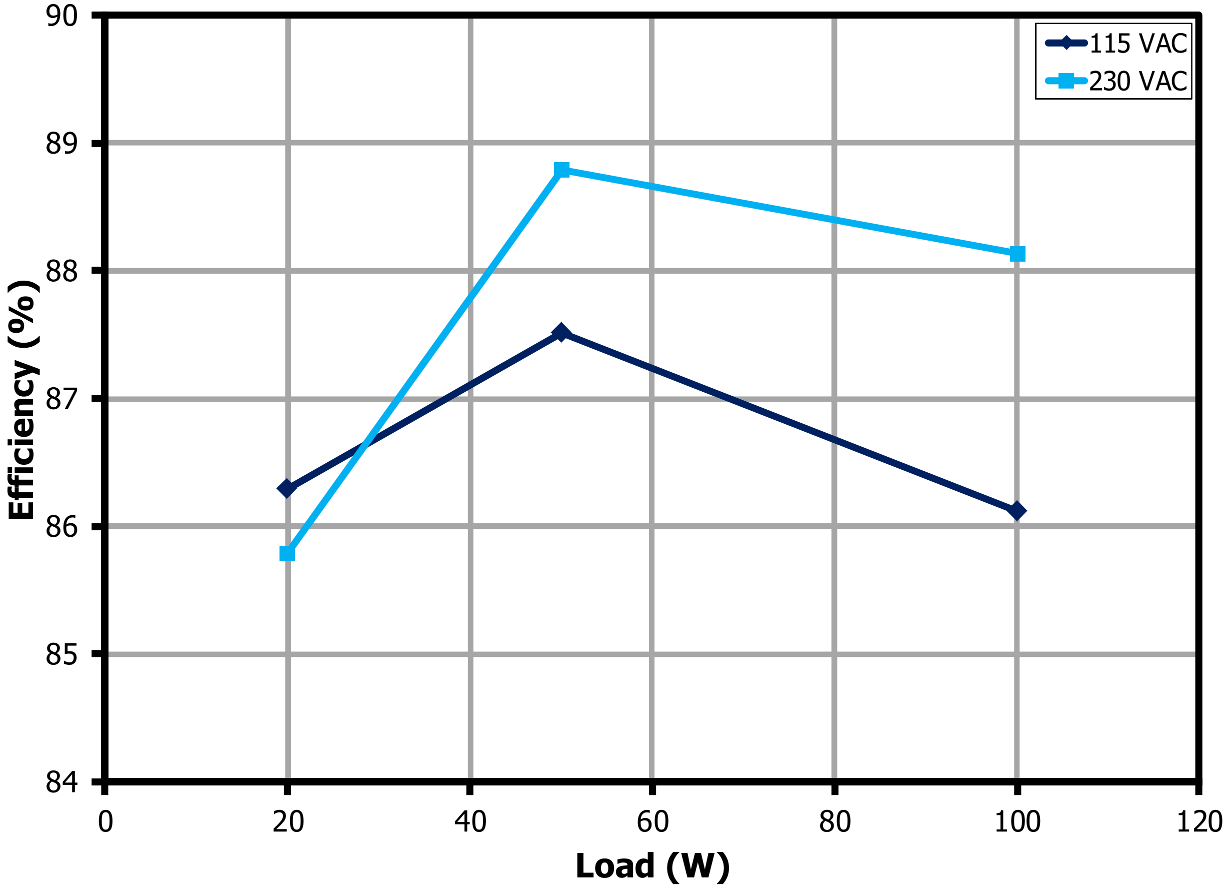

Figure 13 – System Efficiency vs. Load.

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11.3 Power Factor

Power factor measurements were made using a sine wave AC source.

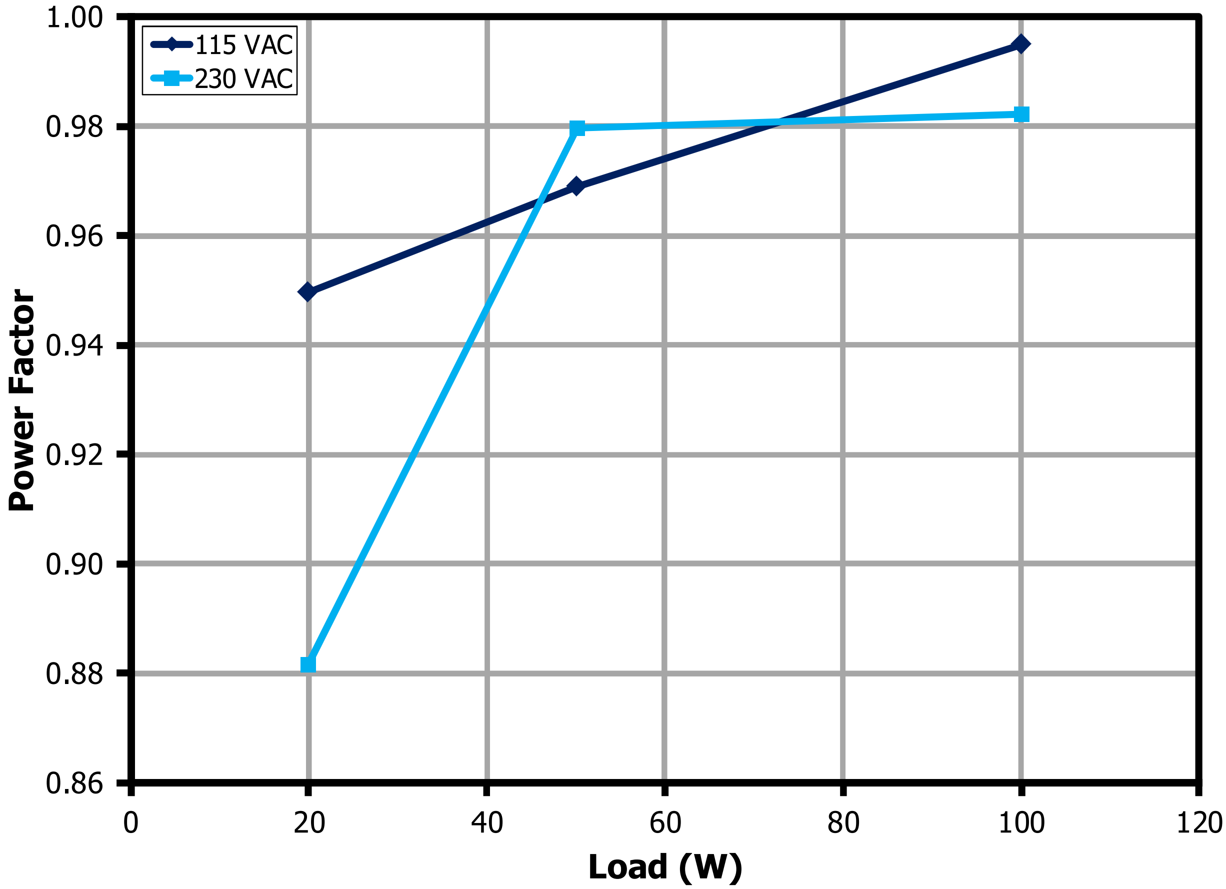

Figure 14 – Power Factor vs. Load.

11.4 Light Load Consumption

Light load consumption data is measured by loading 12 V output while keeping 24 V output unloaded.

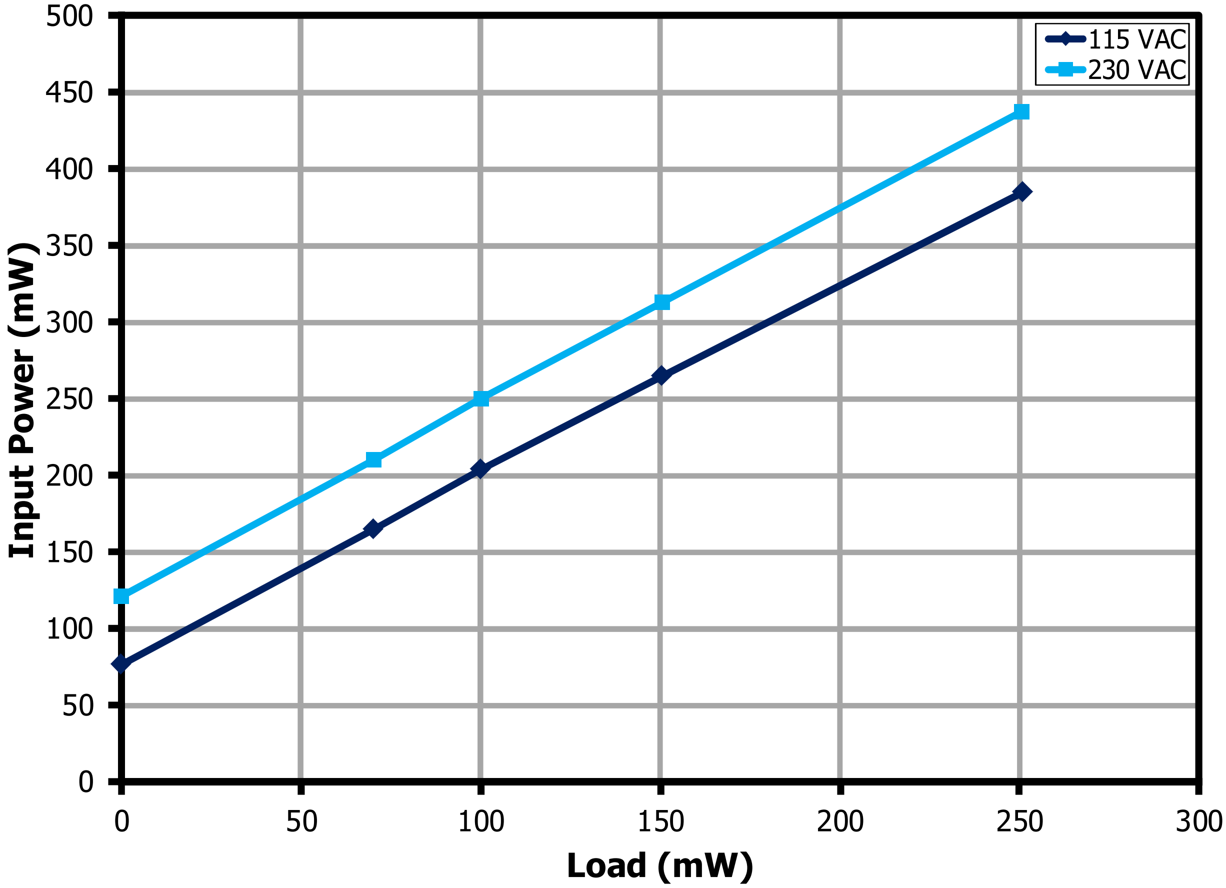

Figure 15 – Input power vs. Load.

V_{IN} (Vac)	P_{IN} (mW)	V12 (V)	I12 (mA)	V24 (V)	I24 (mA)	P_{OUT} (mW)
115	77	12.15	0.0	24.24	0	0
115	165	11.91	5.9	24.44	0	70
115	204	11.94	8.4	24.69	0	100
115	265	12.00	12.5	25.11	0	150
115	385	12.02	20.9	25.6	0	251
230	121	12.13	0.0	24.21	0	0
230	210	11.87	5.9	24.4	0	70
230	250	11.84	8.5	24.5	0	100
230	313	11.93	12.6	24.99	0	150
230	437	11.99	20.9	25.6	0	251

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12 Thermal

Test result after 2 hours running continuously at full-load at 90 VAC on bench with a card board box enclosed at 23 ºC ambient temperature.

Input: 90 VAC, Ambient: 23°C	
Device	**Temperature (°C)**
RT1 (Thermistor)	101
L2 (PFC Choke)	59.5
L1 (CM Choke)	70.5
BR1 (Bridge Rectifier)	82.2
U1 (PFS7524L)	85
U1 Heatsink	79.4
U8 (LNK6777V)	86
U8 Heatsink	84
L3 (DM Choke)	67.1
T1 (Transformer)	81.5
D9 (Primary Clamp Diode)	70.3
D14 (24 V Output Rectifier Diode)	70.2
D2 (12 V Output Rectifier Diode)	68.5
D2, D14 Heat Sink	65.4
R1 (24 V Output Diode Snubber Resistor)	73.5
R49 (24 V Output Diode Snubber Resistor)	72.2
R2 (12 V Output Diode Snubber Resistor)	62.7

13 Waveforms

13.1 *Input Voltage and Current*

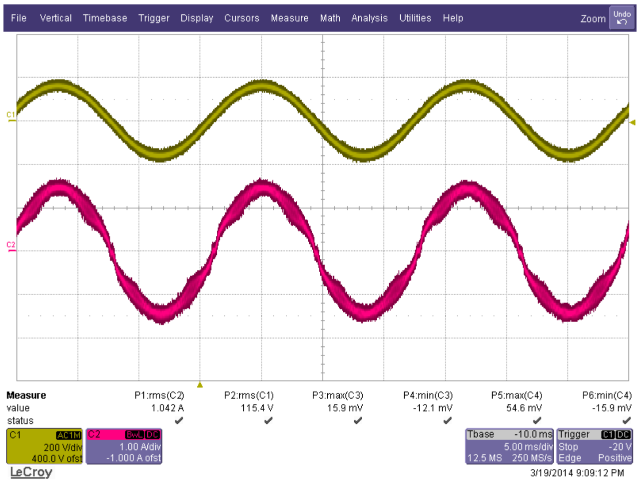

Figure 16 – 115 VAC, 100 W Load.
Upper: V_{IN}, 200 V / div., 5 ms / div.
Lower: I_{IN}, 1 A / div.

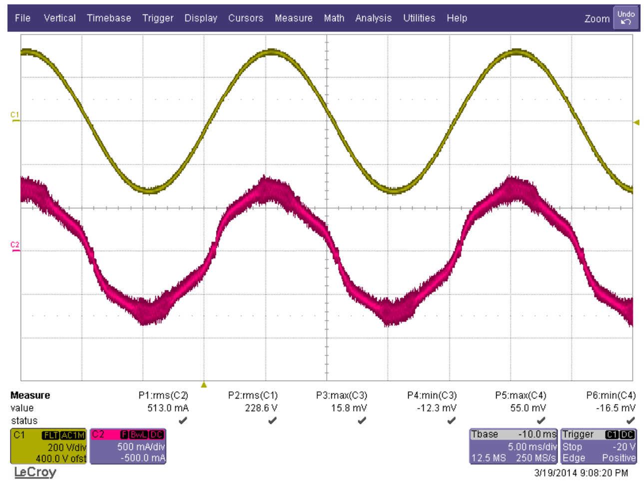

Figure 17 – 230 VAC, 100 W Load.
Upper: V_{IN}, 200 V / div., 5 ms / div.
Lower: I_{IN}, 0.5 A / div.

13.2 *LinkSwitch-HP Switch Primary Drain Voltage and Current*

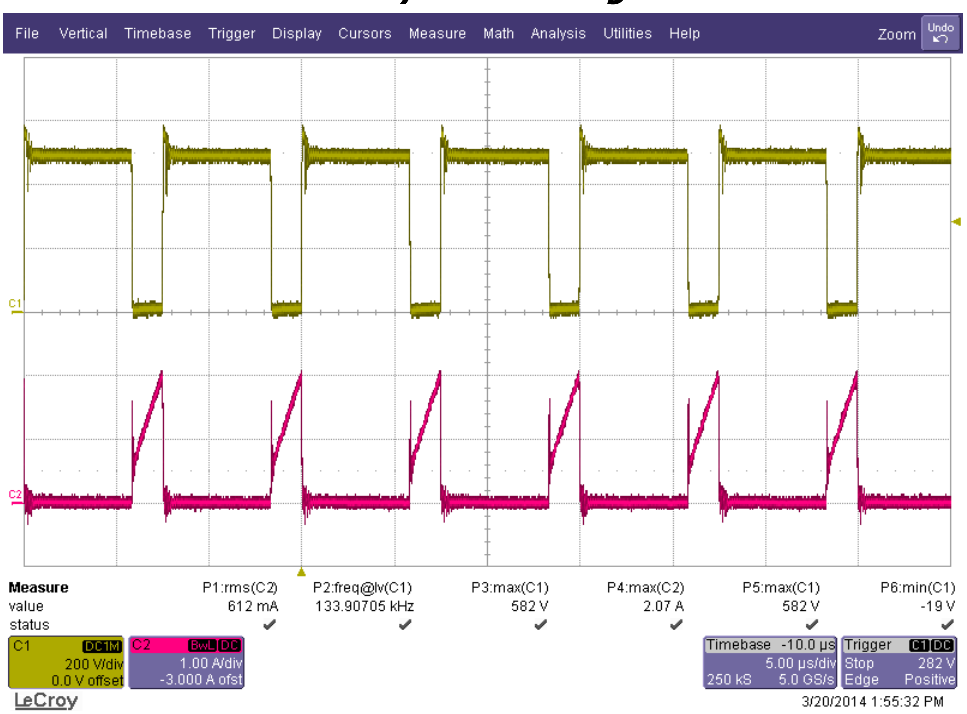

Figure 18 – LinkSwitch-HP Primary Drain Voltage and Current.
Upper: Voltage, 200 V / div., 5 µs / div.
Lower: Current, 1 A / div.

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13.3 *PFC Switch Voltage and Current - Normal Operation*

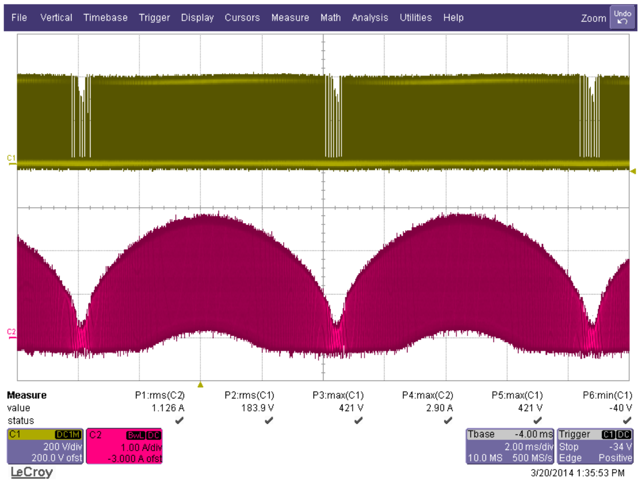

Figure 19 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC
Upper: V_{DRAIN}, 200 V / div., 2 ms / div.
Lower: Inductor Current, 1 A / div.

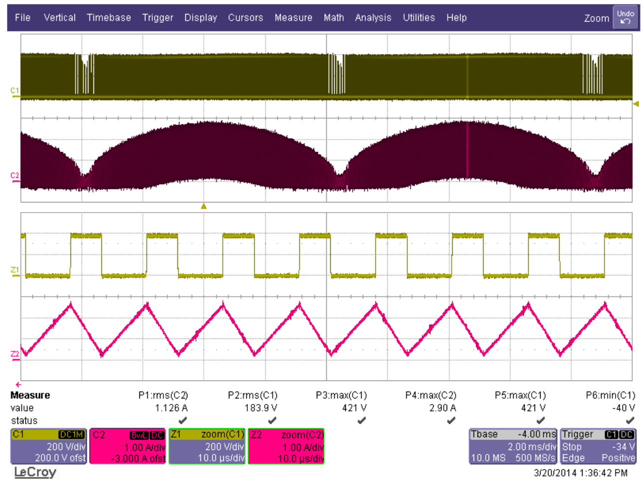

Figure 20 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC.
Upper: V_{DRAIN}, 200 V / div., 10 µs / div.
(Zoom in on Top of Sine Wave)
Lower: Inductor Current, 1 A / div.

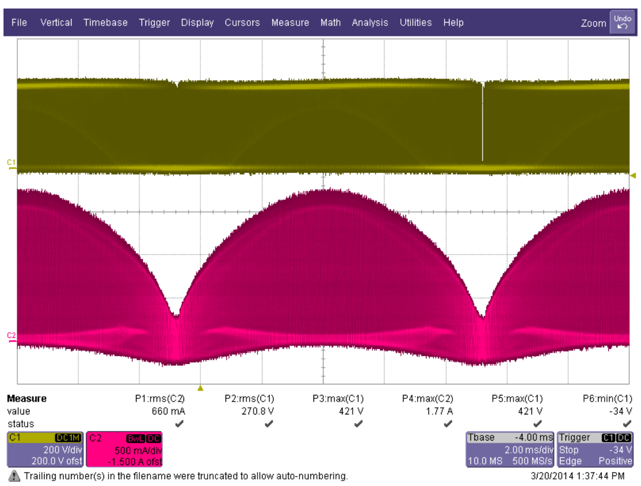

Figure 21 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: V_{DRAIN}, 200 V / div., 2 ms / div.
Lower: Inductor Current, 0.5 A / div.

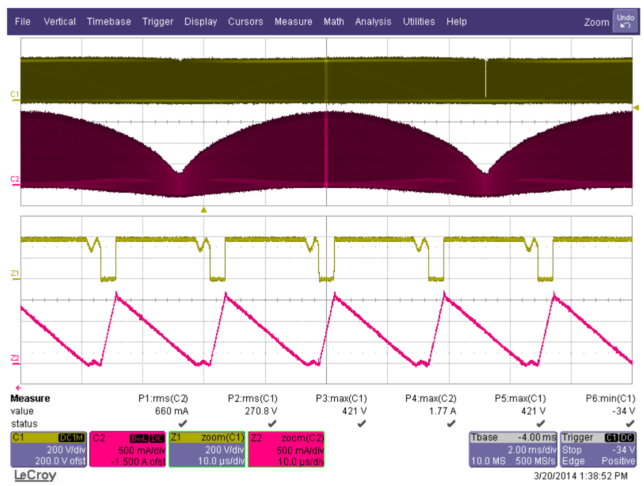

Figure 22 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: V_{DRAIN}, 200 V / div., 10 µs / div.
(Zoom in on Top of Sine Wave)
Lower: Inductor Current, 0.5 A / div.

13.4 *AC Input Current and PFC Output Voltage During Start-up*

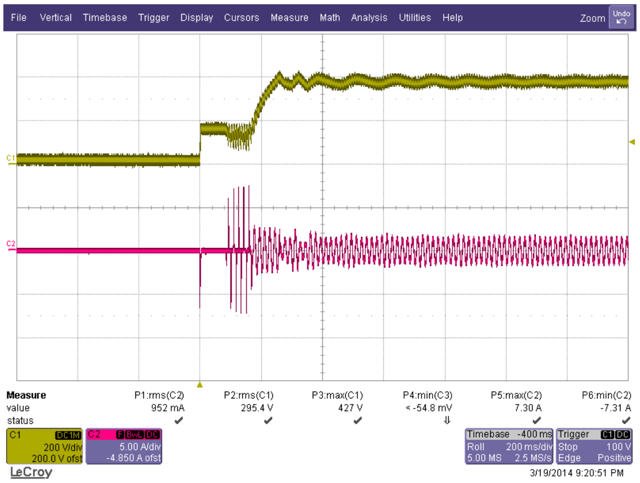

Figure 23 – AC Input Current vs. PFC Output Voltage at Start-up, 90% Load, 115 VAC.
Upper: PFC V_{OUT}, 200 V / div., 200 ms / div
Lower: AC I_{IN}, 5 A / div.

Figure 24 – AC Input Current vs. PFC Output Voltage at Start-up, 90% Load, 230 VAC.
Upper: PFC V_{OUT}, 200 V / div., 200 ms / div.
Lower: AC I_{IN}, 5 A / div.

13.5 *LinkSwitch-HP Drain Voltage and Current During Start-up*

Figure 25 – LinkSwitch-HP Start-up.
115 VAC, 90% Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div., 50 ms / div.

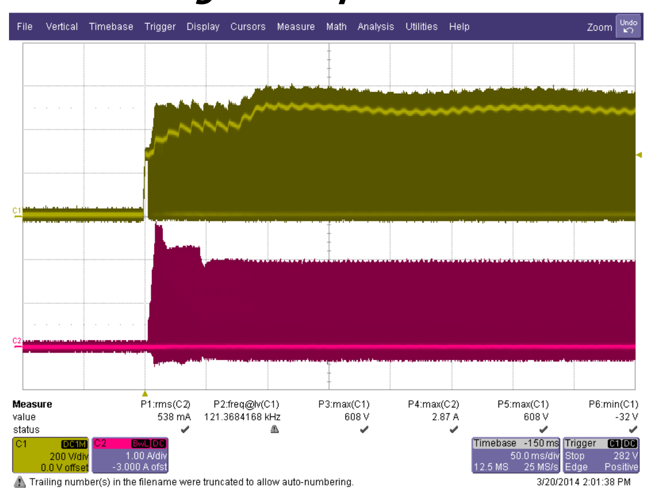

Figure 26 – LinkSwitch-HP Start-up.
230 VAC, 90% Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div., 50 ms / div.

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13.6 *Output Voltage Start-up*

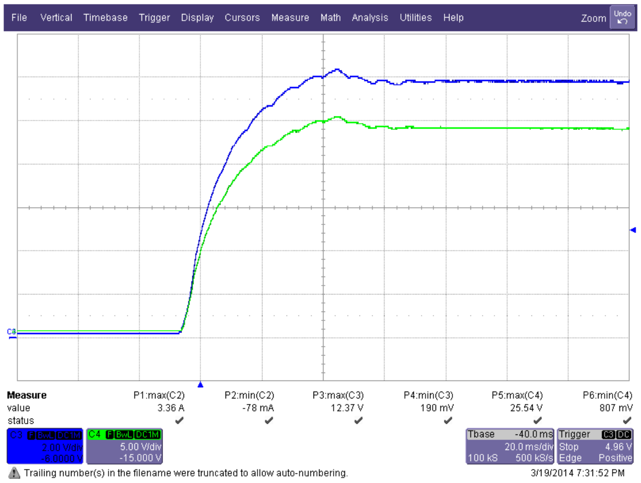

Figure 27 – Output Start-up. 115 VAC, 90% Load.
Upper: 12 V_{OUT}, 2 V / div.
Lower: 24 V_{OUT}, 5 V / div., 20 ms / div.

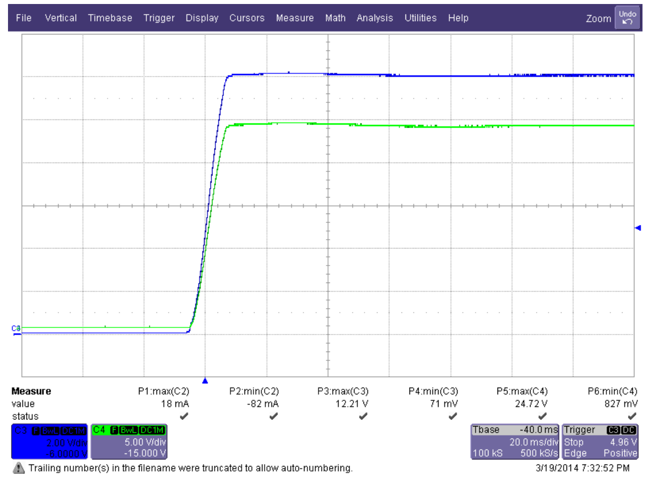

Figure 28 – Output Start-up. 115 VAC, 0% Load.
Upper: 12 V_{OUT}, 2 V / div.
Lower: 24 V_{OUT}, 5 V / div., 20 ms / div.

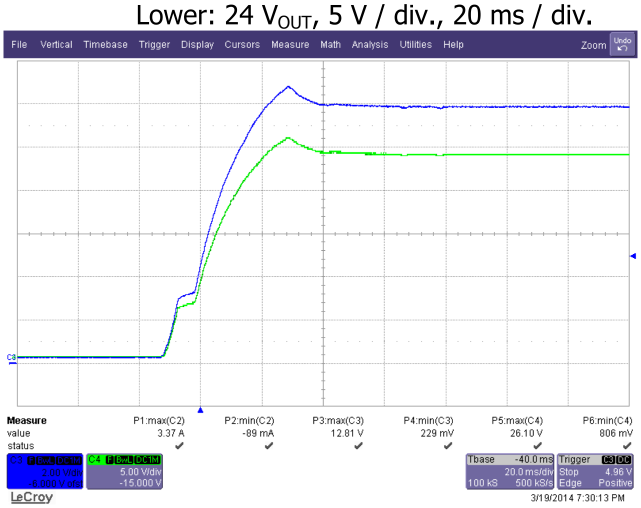

Figure 29 – Output Start-up. 230 VAC, 90% Load.
Upper: 12 V_{OUT}, 2 V / div.
Lower: 24 V_{OUT}, 5 V / div., 20 ms / div.

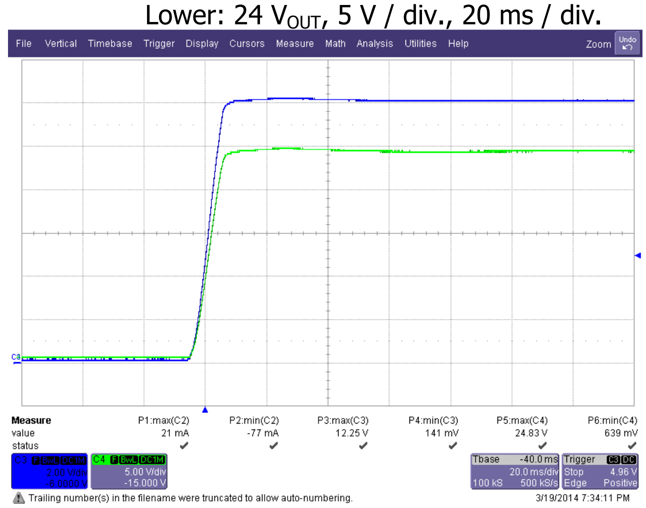

Figure 30 – Output Start-up. 230 VAC, 0% Load.
Upper: 12 V_{OUT}, 2 V / div.
Lower: 24 V_{OUT}, 5 V / div., 20 ms / div.

13.7 *Output Rectifier Diode Voltage Waveforms*

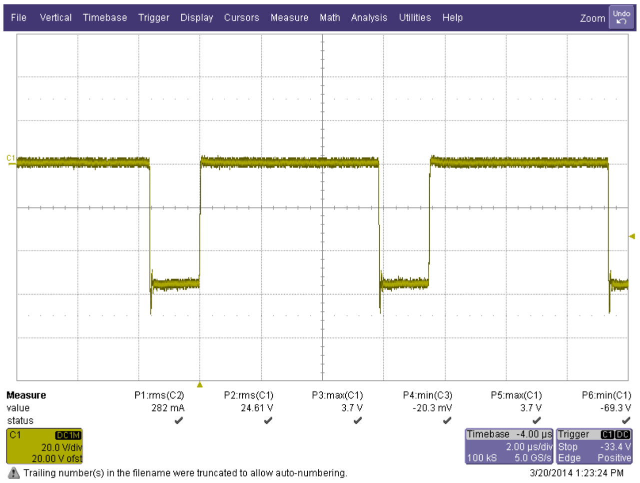

Figure 31 – 12 V Output Rectifier Diode Voltage
100% Load.
Upper: 12 V Diode Voltage, 20 V / div.
2 µs / div.

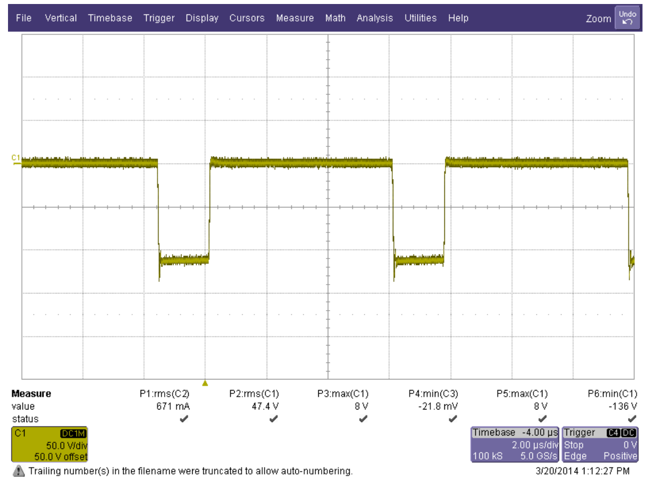

Figure 32 – 24 V Output Rectifier Diode Voltage
100% Load.
Upper: 24 V Diode Voltage, 50 V / div.
2 µs / div.

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14 Output Ripple Measurements

14.1 *Ripple Measurement Technique*

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

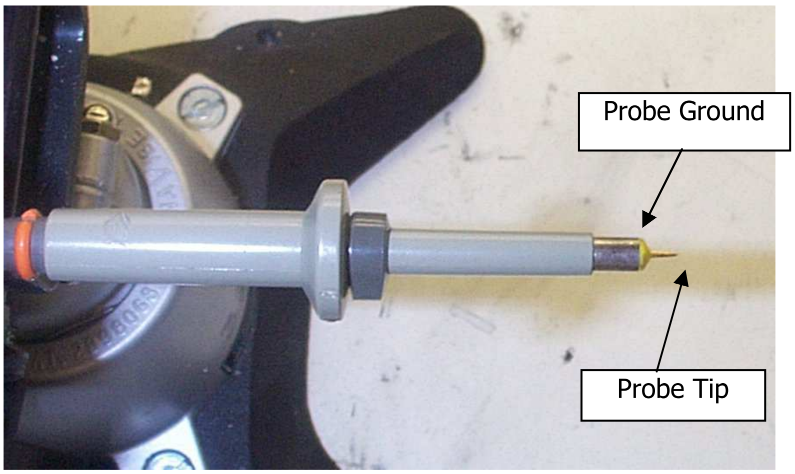

Figure 33 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

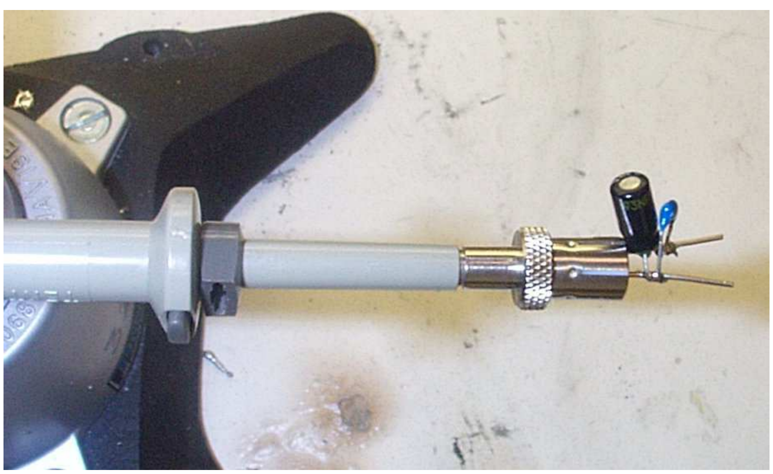

Figure 34 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

14.1.1 Full Load Output Ripple Results

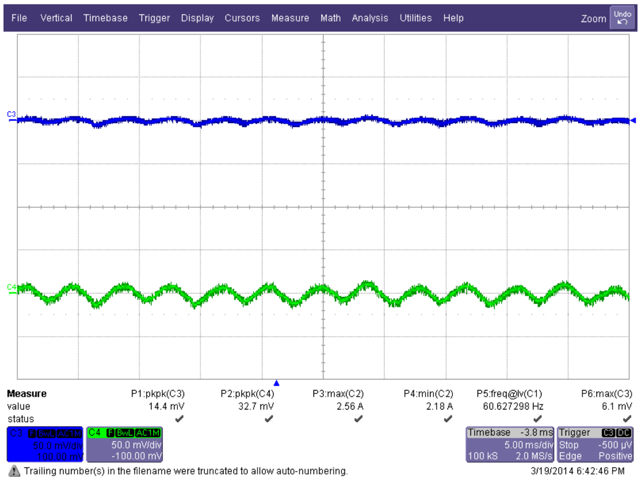

Figure 35 – Output Ripple, 100% Load.
Upper: 12 V_{RIPPLE}, 50 mV / div.
Lower: 24 V_{RIPPLE}, 50 mV / div., 5 ms / div.

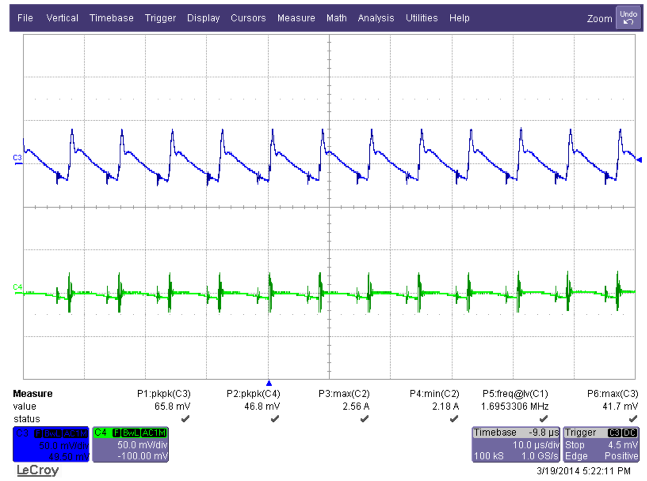

Figure 36 – Output Ripple, 100% Load.
Upper: 12 V_{RIPPLE}, 50 mV / div.
Lower: 24 V_{RIPPLE}, 50 mV / div., 10 μs / div.

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14.2 Output Load Step Response

The figures below show transient response with a 10%-100%-10%, 50%-100%-50%, load steps for the 12/24 V outputs by keeping constant load on one output. The oscilloscope was triggered using the rising edge of the load step, and averaging was used to cancel out ripple components asynchronous to the load step in order to better ascertain the load step response.

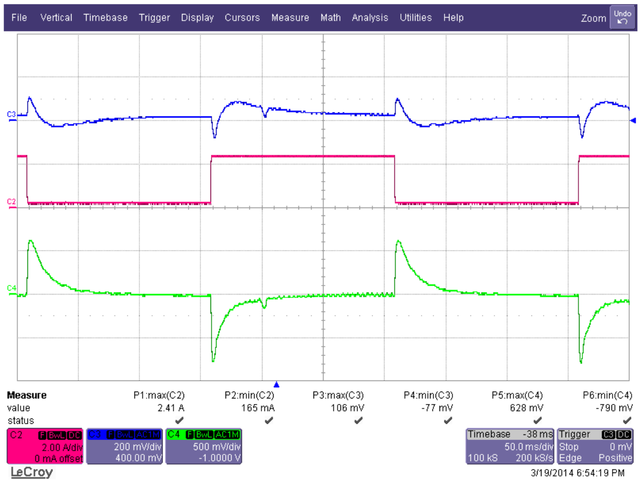

Figure 37 – Output Transient Response.
10%-100%-10% Load Step on 24 V and 10% Load on 12 V, 50 ms / div.
Upper: 12 V_{OUT}, 200 mV / div.
Middle: I_{LOAD}, 24 V, 2 A / div.
Lower: 24 V_{OUT}, 500 mV / div.

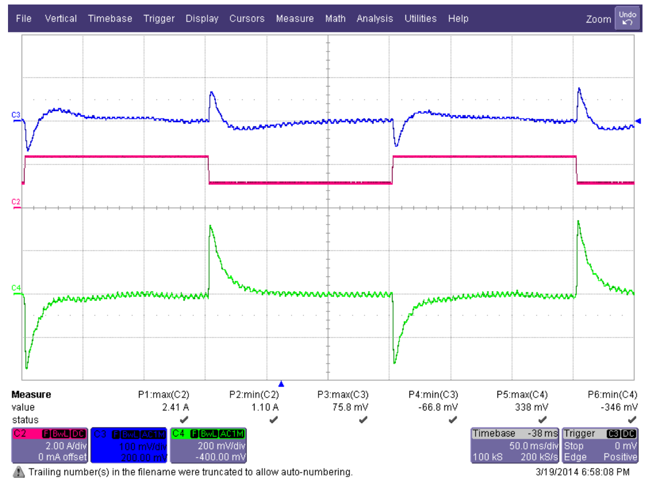

Figure 38 – Output Transient Response.
50%-100%-50% Load Step on 24 V and 10% Load on 12 V, 50 ms / div.
Upper: 12 V_{OUT}, 100 mV / div.
Middle: I_{LOAD}, 24 V, 2 A / div.
Lower: 24 V_{OUT}, 200 mV / div.

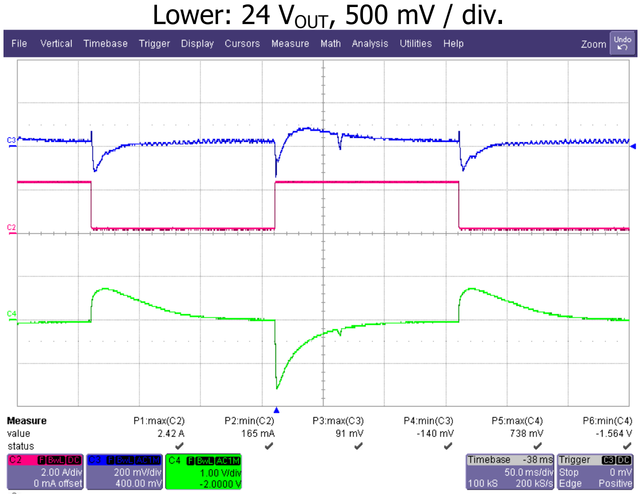

Figure 39 – Output Transient Response.
10%-100%-10% Load Step on 24 V and 100% Load on 12 V, 50 ms / div.
Upper: 12 V_{OUT}, 200 mV / div.
Middle: I_{LOAD}, 24 V, 2 A / div.
Lower: 24 V_{OUT}, 1 V / div.

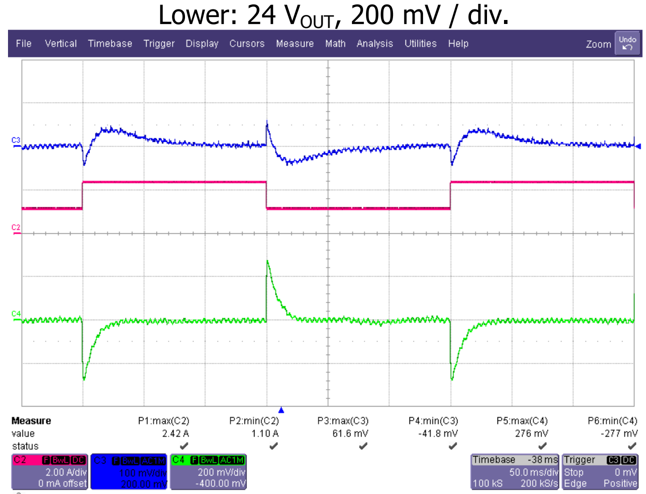

Figure 40 – Output Transient Response.
50%-100%-50% Load Step on 24 V and 100% Load on 12 V, 50 ms / div.
Upper: 12 V_{OUT}, 100 mV / div.
Middle: I_{LOAD}, 24 V, 2 A / div.
Lower: 24 V_{OUT}, 200 mV / div.

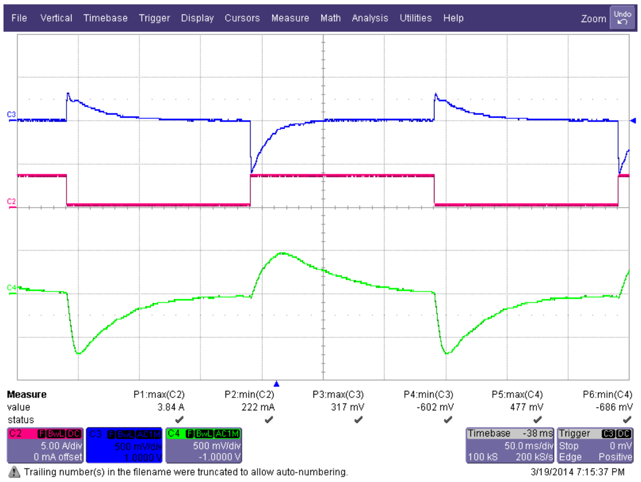

Figure 41 – Output Transient Response.
10%-100%-10% Load Step on 12 V and 10% Load on 24 V, 50 ms / div.
Upper: 12 V_{OUT}, 500 mV / div.
Middle: I_{LOAD}, 12 V, 5 A / div.
Lower: 24 V_{OUT}, 500 mV / div.

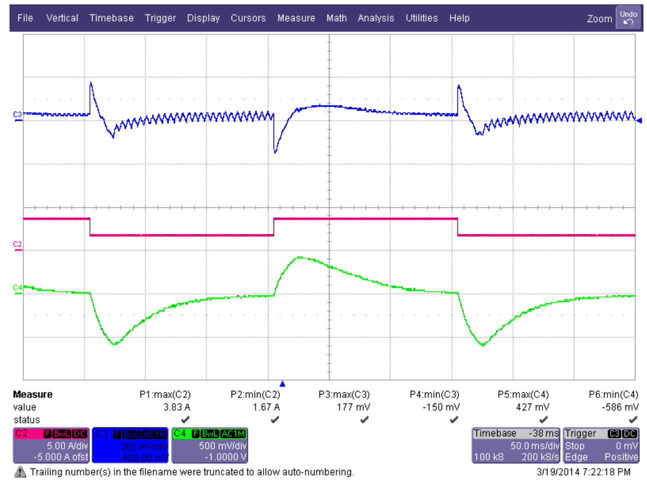

Figure 42 – Output Transient Response.
50%-100%-50% Load Step on 12 V and 10% Load on 24 V, 50 ms / div.
Upper: 12 V_{OUT}, 200 mV / div.
Middle: I_{LOAD}, 12 V, 5 A / div.
Lower: 24 V_{OUT}, 500 mV / div.

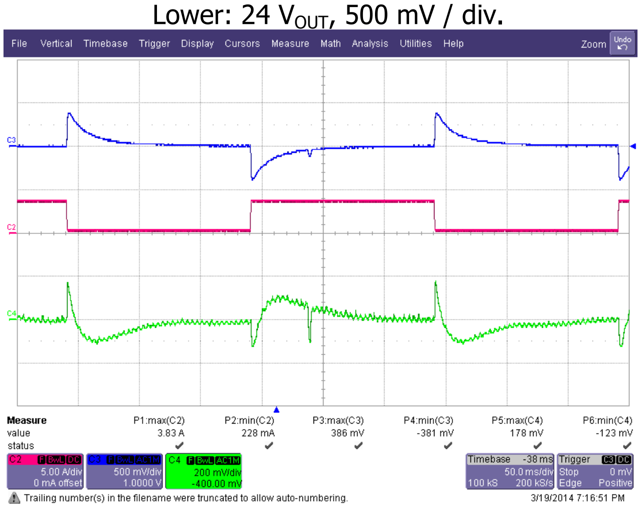

Figure 43 – Output Transient Response.
10%-100%-10% Load Step on 12 V and 100% Load on 24 V, 50 ms / div.
Upper: 12 V_{OUT}, 500 mV / div.
Middle: I_{LOAD}, 12 V, 5 A / div.
Lower: 24 V_{OUT}, 200 mV / div.

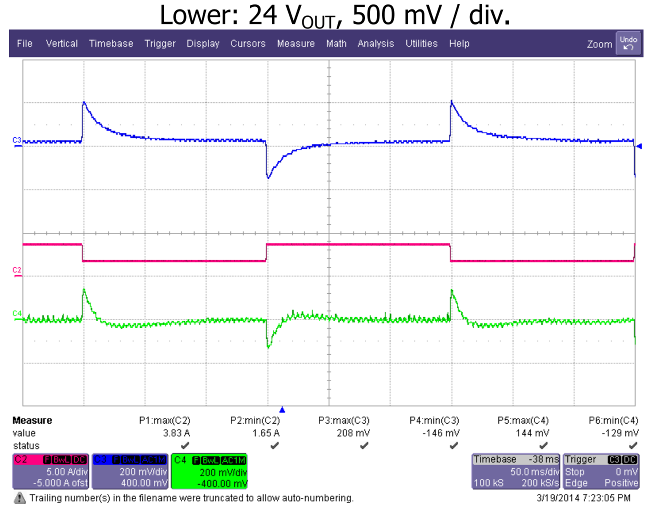

Figure 44 – Output Transient Response.
50%-100%-50% Load Step on 12 V and 100% Load on 24 V, 50 ms / div.
Upper: 12 V_{OUT}, 200 mV / div.
Middle: I_{LOAD}, 12 V, 2 A / div.
Lower: 24 V_{OUT}, 200 mV / div.

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15 Conducted EMI

15.1 EMI Set-up

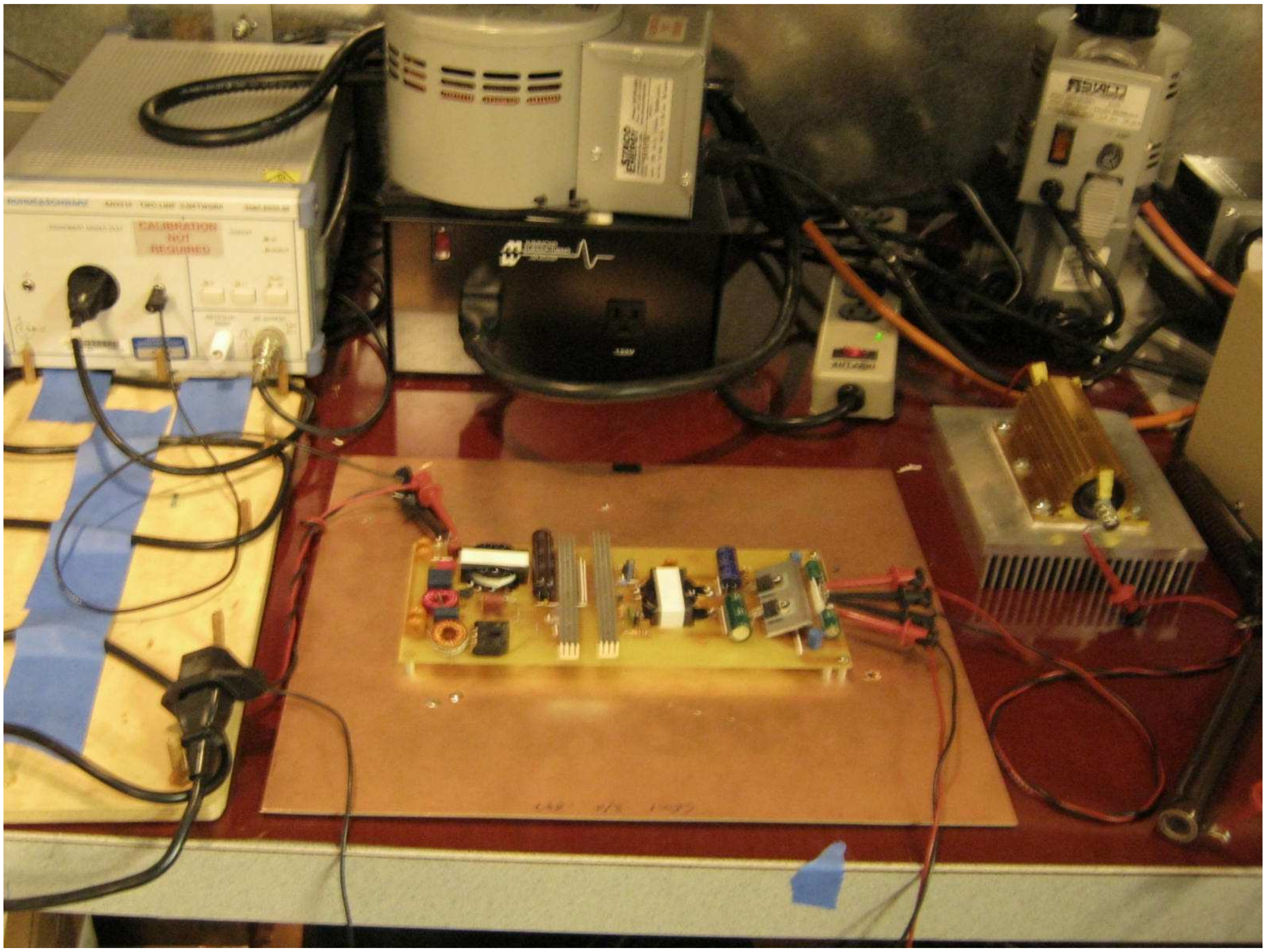

Figure 45 – EMI Test Set-up.

15.2 *EMI Scans*

Conducted EMI tests were performed with a resistive load on the 12/24 V outputs. The secondary ground of the unit was connected to the metallic copper plane via a mounting screw in the top right corner of the PCB as was the Y-capacitors via a mounting screw in the top left corner of the PCB. The AC cord's earth was also bonded directly to the copper plane. The resistive load was left floating.

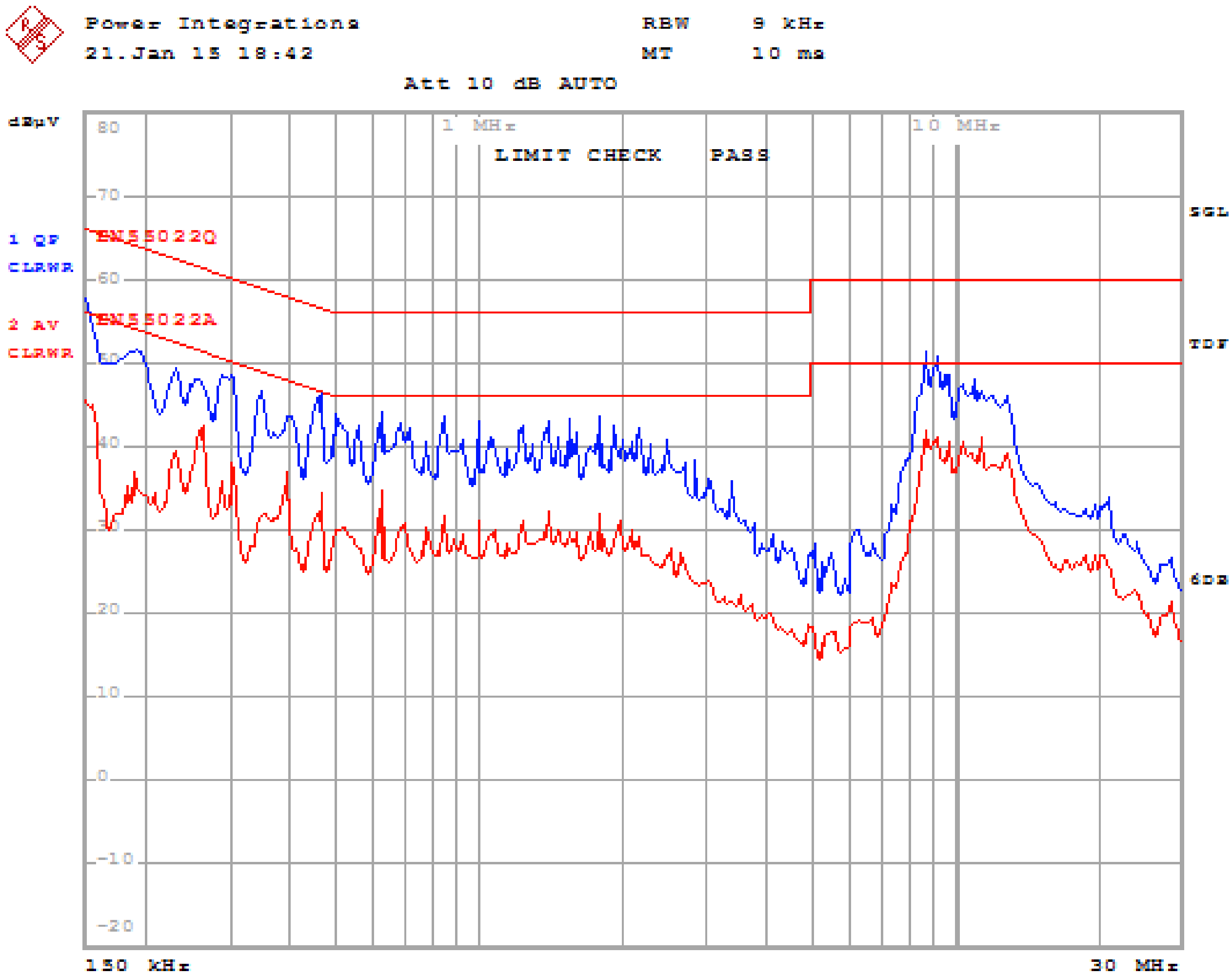

Figure 46 – Conducted EMI, 115 VAC.

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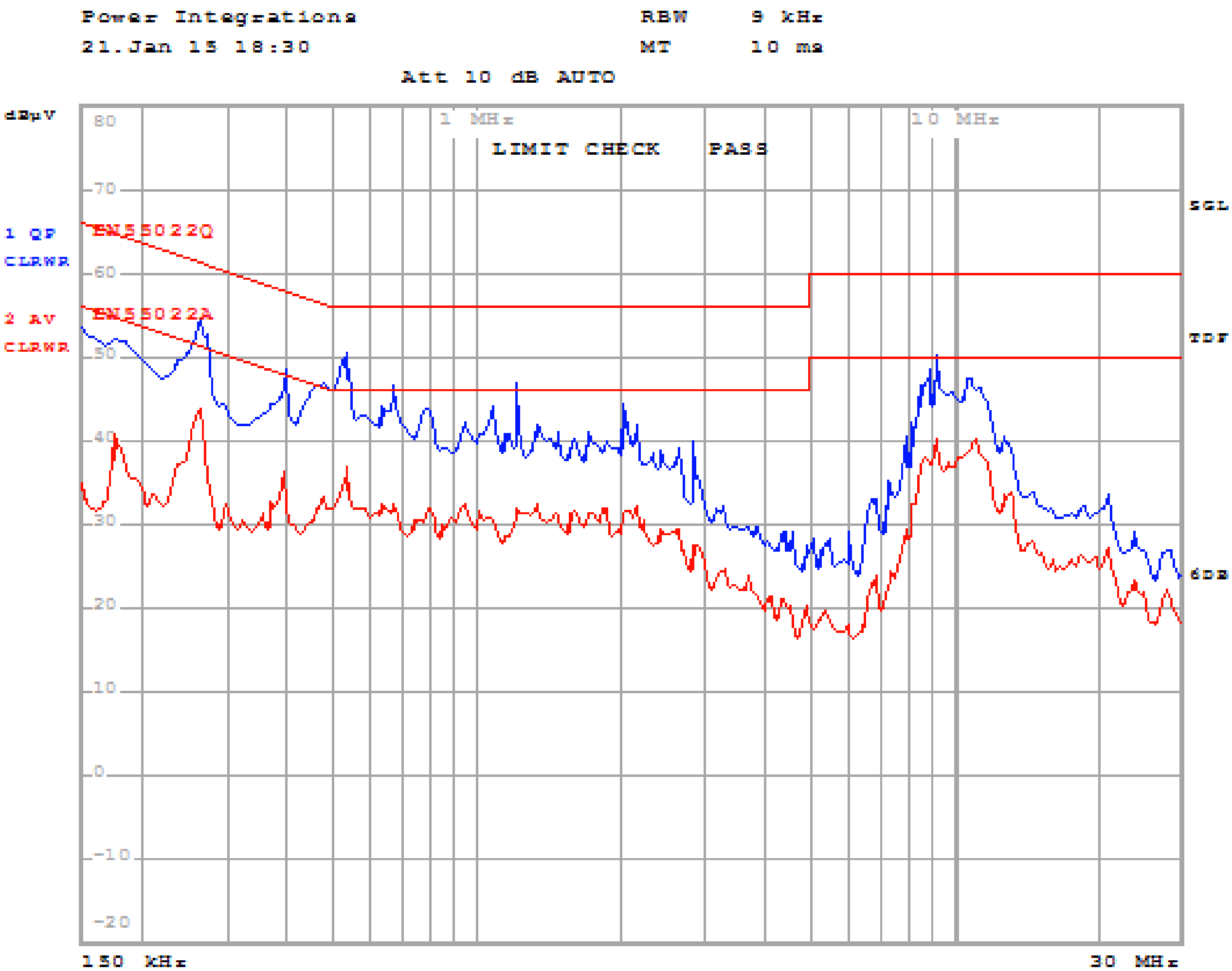

Figure 47 – Conducted EMI, 230 VAC.

16 Gain-Phase Measurement

Gain-phase measurements were carried out on DER-393 at 20%, 50% and 100% loads.

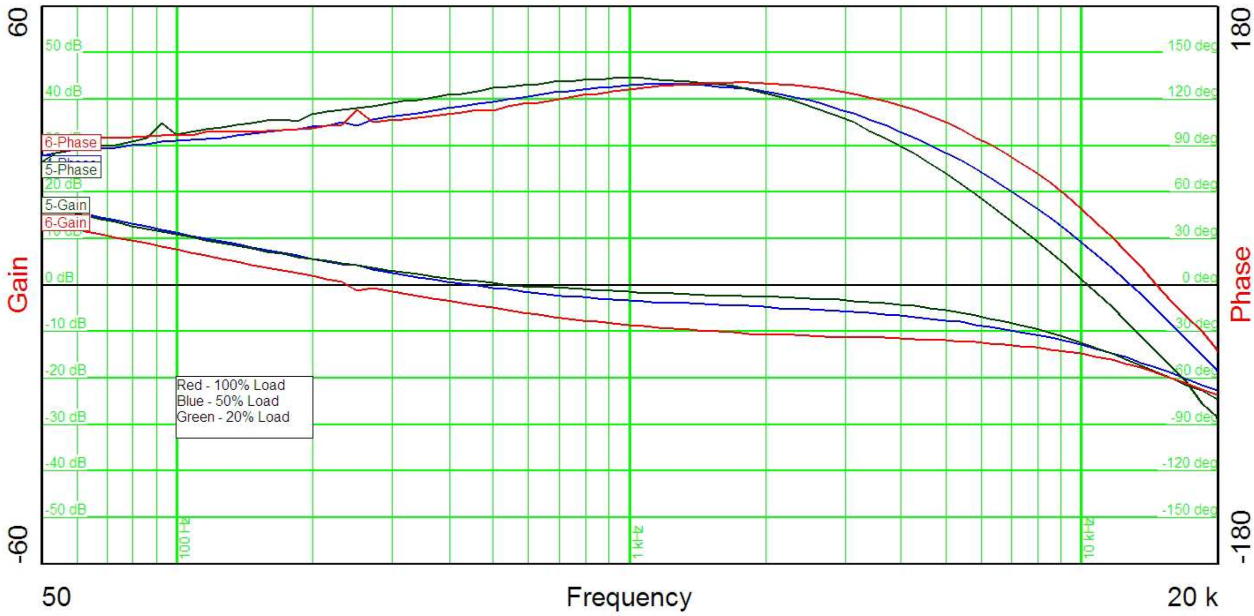

Figure 83 – DER-393 LinkSwitch-HP Gain-Phase Measurement.

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17 Surge Tests

17.1 *Combination Wave (Differential Mode Surge)*

Combination Wave Surge Test (IEC 61000-4-5)							
S.No	**Polarity**	**Voltage (kV)**	**Time Interval (Sec)**	**Impedance (Ω)**	**Angle (°)**	**Differential Mode**	**Test Result**
1	Positive	2	10	2	0, 90, 180, 270	L-N	Pass
2	Negative	2	10	2	0, 90, 180, 270	L-N	Pass

Note: DC-DC Stage is turning off during surge because of input over voltage protection and recovering back when the DC bus voltages goes below OV turn on threshold.

17.2 *Combination Wave (Common Mode Surge)*

Combination Wave Surge Test (IEC 61000-4-5)						
Polarity	**Voltage (kV)**	**Time Interval (Sec)**	**Impedance (Ω)**	**Angle (°)**	**Common Mode**	**Test Result**
Positive	3	10	12	0, 90, 180, 270	L,N-PE	Pass
Negative	3	10	12	0, 90, 180, 270	L,N-PE	Pass
Positive	3	10	12	0, 90, 180, 270	L-PE	Pass
Negative	3	10	12	0, 90, 180, 270	L-PE	Pass
Positive	3	10	12	0, 90, 180, 270	N-PE	Pass
Negative	3	10	12	0, 90, 180, 270	N-PE	Pass

18 ESD

TEST	
10 strikes, +8.8 kV contact on output ground	pass
10 strikes, +8.8 kV contact on 12 V output	pass
10 strikes, +8.8 kV contact on 24 V output	pass
10 strikes, -8.8 kV contact on output ground	pass
10 strikes, -8.8 kV contact on 12 V output	pass
10 strikes, -8.8 kV contact on 24 V output	pass
10 strikes, +16.5 kV air discharge on output ground	pass
10 strikes, +16.5 kV air discharge on 12 V output	pass
10 strikes, +16.5 kV air discharge on 24 V output	pass
10 strikes, -16.5 kV air discharge on output ground	pass
10 strikes, -16.5 kV air discharge on 12 V output	pass
10 strikes, -16.5 kV air discharge on 24 V output	pass

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19 Revision History

Date	Author	Revision	Description and Changes	Reviewed
24-Jun-15	SS	3.1	Initial Release	Apps & Mktg
13-Jul-15	KM	3.2	Updated Figure 4 Schematic and PFC Choke Information	

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