Design Example Report

Title	***Two-Wire (No Neutral), Wide-Range, Isolated Flyback, Bluetooth Wall Switch Using Power Integrations LinkSwitch™-TN2 LNK3202D and Nordic BLE/MCU nRF52382***
Specification	90 VAC – 277 VAC Input
Application	Lighting Control, Home Automation
Author	Applications Engineering Department
Document Number	DER-832
Date	September 18, 2019
Revision	1.0

Summary and Features

- Compatible with 2-wire (no neutral), home / building wiring
- Isolated LNK3202D power supply with full-wave rectifier
- Low-component count with integrated 725 V MOSFET, current-sensing, and protection
- Wide-range AC input
- 3 W to 600 W load
- <100 µA standby current (including BLE) at 230 VAC
- 60 µA LNK3202D no-load input current at 230 VAC

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

A typical smart wall switch requires LINE and NEUTRAL to work properly. This is true especially on many WIFI-based switch that consumes higher power. However, a majority of houses around the world do not have neutral wire on the wall switch. A two-wire (no Neutral) smart wall switch addresses this market.

One of the challenges in making a two-wire switch is the need to minimize leakage current that might cause 'ghosting' or light flutter even when the switch is OFF. Many bulbs, especially the non-dimmable types, do not have a bleeder circuit that prevents 'ghosting' due to high leakage current. Minimizing the leakage current ensures wider compatibility across many types of load.

LinkSwitch-TN2, paired with a proprietary current-shaping circuit for ultra-low current consumption, is the ideal solution in this type of applications.

This document is an engineering report describing a two-wire (no Neutral) Bluetooth low-energy (BLE) smart wall switch using LinkSwitch-TN2 LNK3202D. This demo board is intended as a general purpose evaluation platform for LinkSwitch-TN2.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit board layout, and performance data.

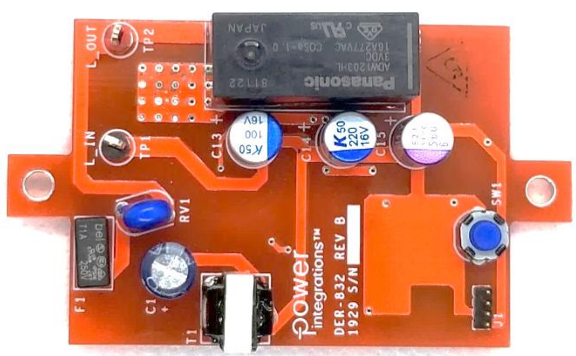

Figure 1 – Populated Circuit Board Photograph, Top

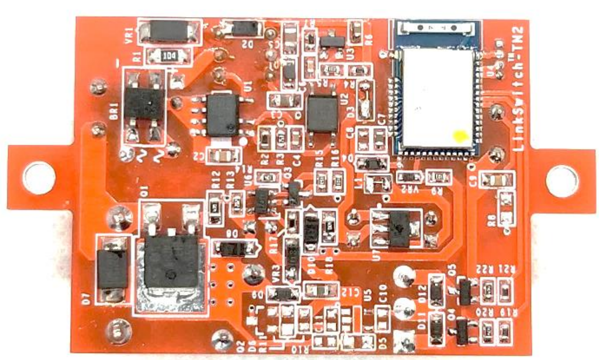

Figure 2 – Populated Circuit Board Photograph, Bottom

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		277	VAC	
Frequency	f_{LINE}	47	50/60	63	Hz	
Rated Load						
Resistive Load or High PF Load		3		600	W	
Low PF Load		5		150	W	
System Standby Input Current			120	150	μA	At 120 VAC, After 5 Minutes.
			80	100		At 230 VAC, After 5 Minutes.
LinkSwitch-TN2 + LDO Block						
LinkSwitch-TN2 Output Voltage	V_{TN2}		3.5		V	
3V Regulator Output Voltage	V_{OUT}		3			
3V Regulator Output Current	I_{OUT}		60		mA	
No-Load Input Current			70		μA	At 120 VAC, After 5 Minutes.
			60		μA	At 230 VAC, After 5 Minutes.
BLE Module						
Power Consumption			5		mW	
Ambient Temperature	T_{AMB}		40		ºC	Free Convection, Sea Level.

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3 Schematic

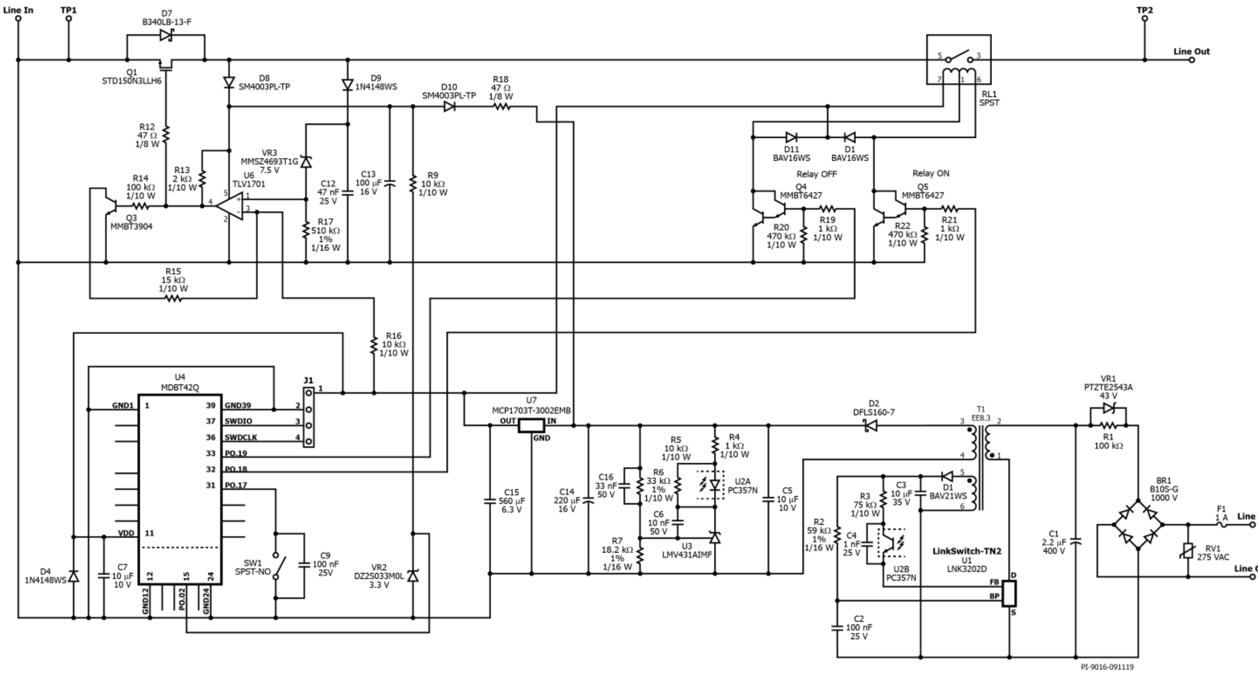

Figure 3 –Schematic.

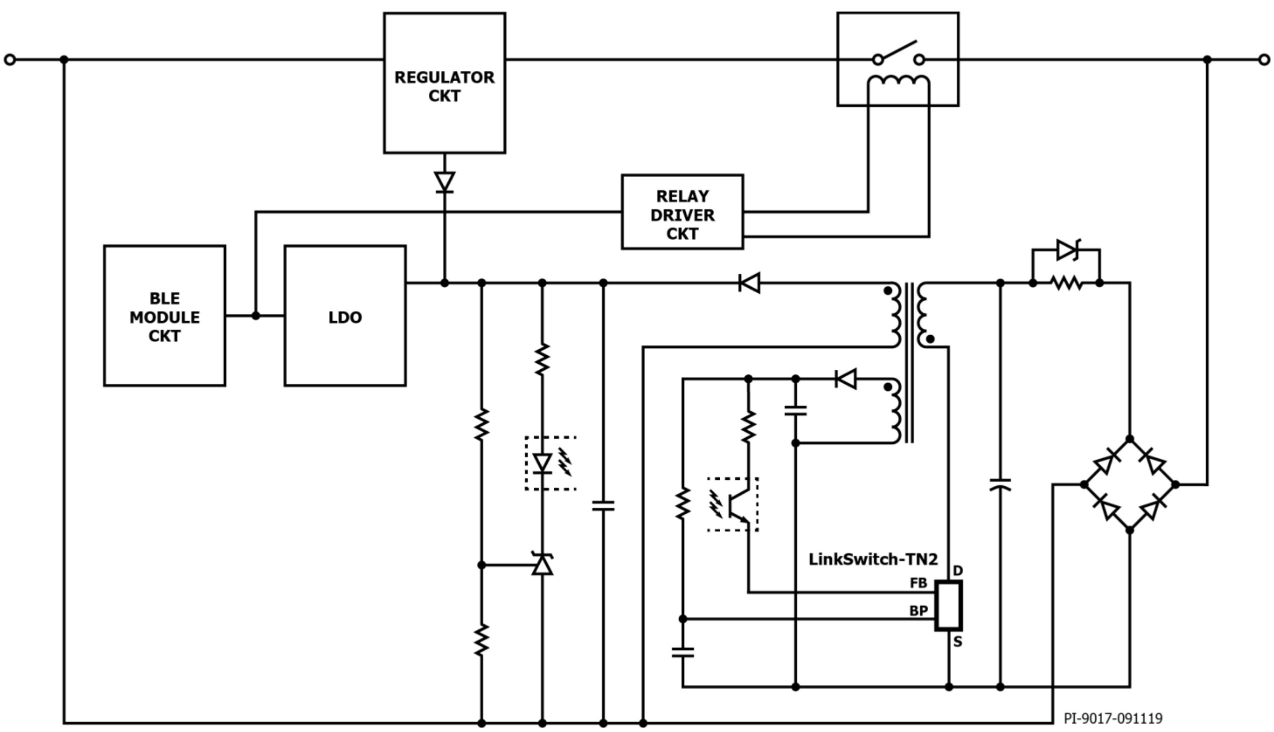

Figure 4 – Block Diagram Schematic.

4 Circuit Description

4.1 *LinkSwitch-TN2 Block*

4.1.1 Input Stage

The input stage is comprised of fuse F1 for safety protection, varistor RV1 for up to 500 V differential line surge protection, bridge rectifier BR1, and bulk capacitor C1.

4.1.2 Current-shaping Circuit

The proprietary R-Z circuit R1 and VR1 form a simple, yet effective means to improve the power factor of the circuit. A higher PF will result to the lowest standby input current. Resistor R1 reduces the peak input current which effectively reduces the input RMS current and increases the power factor. Zener diode VR1 connected in parallel with R1 provides the charging path for the bulk capacitor C1 during start-up to be able to operate the circuit properly. Please see appendix A for tips on how to choose the optimum values for R1 and VR1.

4.1.3 LinkSwitch-TN2 Circuit Operation

Linkswitch-TN2 LNK3202D was configured in an isolated flyback topology to be able to utilize full-wave bridge rectification and deliver power on either side of the AC line. The flyback circuit is formed by the main controller LNK3202D U1, transformer T1, bulk capacitor C1, secondary diode D2 and capacitors C5 and C14. The BP pin capacitor C2, with a value of 100 nF, sets the current limit to standard mode.

4.1.4 Primary Bias Supply

A 12 V auxiliary supply was taken from the bias winding of T1, rectified by D1 and C3. It provides bias current for the optocoupler feedback U2 as well as for the external biasing of the BP pin through R2. The value of R2 was tuned to provide the lowest no-load input current by setting the BP current to approximately 70 μA. Since the auxiliary winding is just a "slave" winding, there could be some part-to-part variation on the auxiliary voltage that may cause the BP current to deviate from its ideal supply current. If tighter control of BP current is desired, then a simple constant current circuit using a transistor and a Zener may be added.

4.1.5 Feedback

Output regulation is achieved using a high CTR optocoupler U2 and a 1.24 V reference U3. Resistors R6 and R7 set the output voltage. Capacitor C4, C6 and C16 provides stability compensation to prevent overshoot during startup or load step. Resistor R5 ensures that U3 gets sufficient bias. Resistor R4 provides the DC gain. The opto-transistor side of U2 is connected in series with the FB pin of LNK3202D. Resistor R3 provides the bias current for the FB pin.

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4.2 *Low Drop-Out Regulator Block*

The LDO regulator U7 provides a stable 3 V supply for the BLE module and relay RL1. Capacitor C15 is the output capacitor of U7. A 560 µF was used in order to sustain the power drawn by the relay during its transition period of 10 ms. When the relay is OFF, the input to the LDO comes from LinkSwitch-TN2. When the relay is ON, the supply comes from Q1 regulator via D10 and R18.

4.3 *Relay Circuit Block*

A 3 V, 2-coil, latching relay RL1 from Panasonic (ADW1203HL) was used. Unlike conventional relay, latching type retains its last state even when the power is gone, similar to that of a regular wall switch. Moreover, it only requires a 3 V pulse of about 10 ms to set and reset the relay unlike conventional relay that needs steady supply.

Transistor Q4, R19, R20 drive the relay OFF while Q5, R21, R22 drive the relay ON. Diodes D11 and D12 protect the transistors Q4 and Q5 from 'inductive kick' by clamping the voltage to 3 V plus 1 diode drop.

4.4 *Q1 Regulator Circuit Block (Power Supply when the Relay is ON)*

This DER uses low voltage MOSFET Q1 and gate driver circuit using a comparator U6.

When the relay is ON, the FET Q1 gate is initially OFF. Depending on the phase of the input line, current may flow from the Source to Drain through Q1 body diode or D7 if the AC line phase is more positive than neutral. In the negative-going phase, since Q1 is OFF, then current will flow through D8 and D9 and will charge the capacitors C12, C13 and C14. The output of comparator U6 is kept low until the voltage on its (+) input equals the reference (-) input which was set to 3 V. The 7.5 V Zener VR3 provides the voltage threshold that determines when the comparator will change state. The threshold is given by Vz (7.5 V) + Vref (3 V) = 10.5V. Resistor R17 provides the bias for the zener and is also responsible for the R-C timer formed by R17 and C12. A 1% tolerance resistor is recommended for R17 and C12 should be of NPO/COG type.

Once the threshold has been reached, the comparator will change from LOW to HIGH state, driving Q1 ON. The circuit comprised of R14, R15, R16 and Q3 provide hysteresis (from 3 V to 1.8 V reference) to prevent Q1 from rapidly turning ON and OFF, and is also part of the R-C timer circuit.

The time constant formed by R17 and C12 was selected such that once Q1 turns ON, it will remain ON for about 12 ms. The choice of 12 ms is chosen in order to ensure that the regulator will work properly for both 50 Hz and 60 Hz system. The ON time may be adjusted on a single input system (voltage, frequency). In selecting the ON-time, the goal is to maximize the time that Q1 is ON, and make sure that it turns OFF when the current is flowing in the direction from the Source to Drain (LINE IN more positive than LINE OUT). Diode D7 is connected in parallel with Q1 so that the current will not flow through Q1 body diode after the FET turns OFF. In order to minimize the dissipation on D7, the ON-time can be set as close as possible to the input voltage zero-crossing. However, enough margin must be maintained due to component tolerances that affects the timing.

Resistor R13 is the pull-up resistor for the output of the comparator U6.

The regulator circuit used in this DER has some restrictions:

a. There is a minimum load required to operate the switch properly. Unlike conventional wall switch with line and neutral, the bulb load is required to close the power loop. If the load is too small, it presents a high impedance or open-circuit; hence, the BLE switch will not work.

b. It is not advisable to use smart bulbs with the wall switch. When the smart bulb is remotely turned OFF, for example, it usually goes into low-power mode and the BLE switch might stop working because the load drops below the minimum load requirement.

4.5 *Bluetooth Low Energy (BLE) Module Circuit Block*

This DER uses a Bluetooth 5-certified Bluetooth Low Energy (BLE) module U4, MDBT42Q, based on Nordic NRF52832 SoC. Its ultra-low current consumption, together with LinkSwitch-TN2 power supply, enables a < 100 uA standby input current at 230 VAC.

4.5.1 Pin Functions

Pin Number	Description
15 (P0.02)	Configured as ADC Input. The pin detects the relay state by sensing the voltage across VR2. Resistor R9 provides the bias current for the zener.
31 (P0.17)	Configured as Digital Input. Senses the push-button switch SW1 to trigger relay ON/OFF. C9 provides passive de-bouncing to ensure clean input signal when the switch SW1 is pressed.
32 (P0.18)	Configured as Digital Output. Provides a 10ms pulse to turn OFF the latching relay.
33 (P0.19)	Configured as Digital Output. Provides a 10ms pulse to turn ON the latching relay.
36 (SWDCLK)	Programming pin.
37 (SWDIO)	Programming pin.
11 (VDD)	The VDD comes from the 3V LDO regulator. C7 is the VDD filter capacitor while D4 protects the BLE module from negative voltage.

Table 1 – Bluetooth Module Pin Description.

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4.5.2 Using the App

This DER uses a Nordic based application, nRF Blinky, for its BLE functionality.

Step 1: Power-up the BLE wall switch.

Step 2: Install nRF Blinky App on Android or IOS devices that support Bluetooth 4.0 or higher.

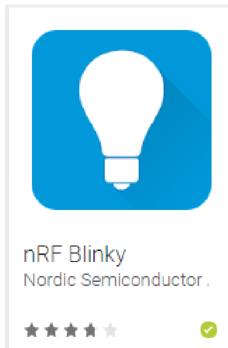

Figure 5 – nRF Blinky Application

Step 3: Switch-ON Bluetooth on the mobile device.

Step 4: Open the nRF Blinky App, the app should detect "DER 832"

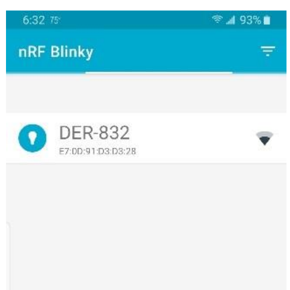

Figure 6 – DER-832 on nRF Blinky App

Step 5: Select DER-832 to connect to unit. Once connected, LED and Button interface can be seen.

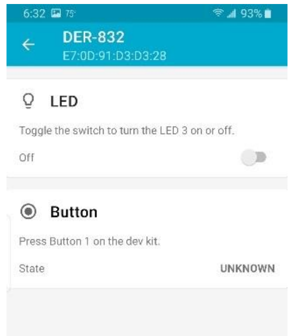

Figure 7 – "Connected" Status Interface

Step 6: Press the LED button to toggle the wall switch.

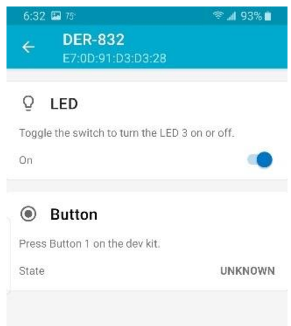

Figure 8 – Switched-ON Status

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5 PCB Layout

PCB copper thickness is 2oz (2.8 mils).

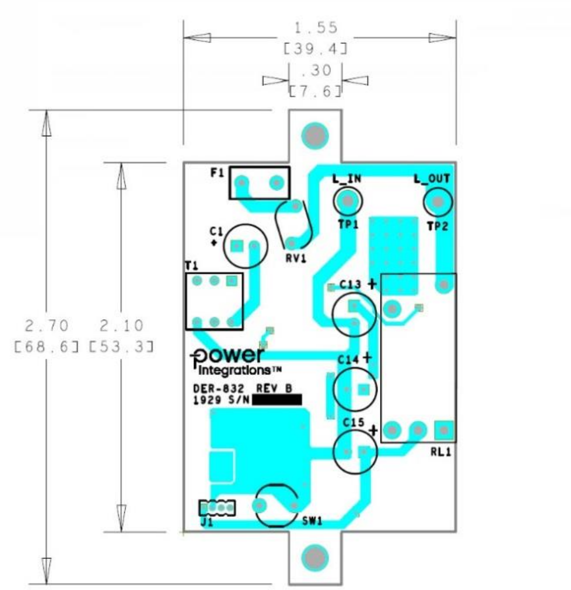

Figure 9 – Printed Circuit Board Layout, Top.

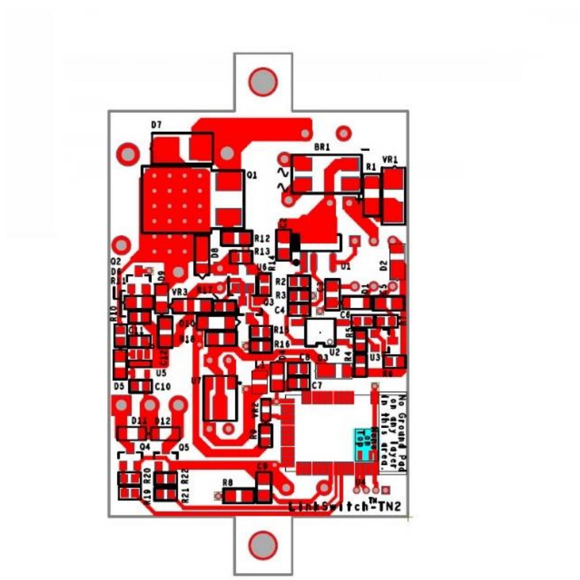

Figure 10 – Printed Circuit Board Layout, Bottom.

6 Bill of Materials

Item	Ref Des	Qty	Description	Mfg Part Number	Mfg
1	BR1	1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	C1	1	2.2 μF, 400 V, Electrolytic, (6.3 x 11)	TAB2GM2R2E110	Ltec
3	C2	1	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
4	C3	1	10 μF, 35 V, Ceramic, X5R, 0805	C2012X5R1V106K085AC	TDK
5	C4	1	1 nF, ±10%,25 V, Ceramic, X7R, 0603	GCM188R71E102KA37D	Murata
6	C5	1	10 μF, 10 V, Ceramic, X7R, 0805	C2012X7R1A106M	TDK
7	C6	1	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
8	C7	1	10 μF, 10 V, Ceramic, X5R, 0603	C1608X5R1A106M	TDK
9	C9	1	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
10	C12	1	47 nF, 25 V, Ceramic, C0G, NP0, 0805	C0805X473J3GECAUTO7210	Kemet
11	C13	1	100 μF, ±20%, 16V, Electrolytic, Gen. Purpose	A750EK107M1CAAE018	Nichicon
12	C14	1	220 μF, ±20%, 16V, Electrolytic, Gen. Purpose	A750EK227M1CAAE016	Nichicon
13	C15	1	560 μF, 6.3 V, Electrolytic, Low ESR, 7 mΩ, (6.3 x 9)	6SEPC560MW	Sanyo
14	C16	1	33 nF 50 V, Ceramic, X7R, 0603	06035C333JAT2A	AVX
15	D1	1	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
16	D2	1	60 V, 1 A, DIODE SCHOTTKY, PWRDI 123	DFLS160-7	Diodes, Inc.
17	D4	1	DIODE, GEN PURP, 75 V 150 mA, SOD323	1N4148WS-7-F	Diodes, Inc.
18	D7	1	40 V, 3 A, Schottky, SMD, DO-214AA	B340LB-13-F	Diodes, Inc.
19	D8	1	200 V, 1 A, Standard Recovery, SOD-123FL	SM4003PL-TP	Micro Commercial
20	D9	1	DIODE, GEN PURP, 75 V 150 mA, SOD323	1N4148WS-7-F	Diodes, Inc.
21	D10	1	200 V, 1 A, Standard Recovery, SOD-123FL	SM4003PL-TP	Micro Commercial
22	D11	1	75 V, 0.15 A, Switching,SOD-323	BAV16WS-7-F	Diodes, Inc.
23	D12	1	75 V, 0.15 A, Switching,SOD-323	BAV16WS-7-F	Diodes, Inc.
24	F1	1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
25	J1	1	4 Position (1 x 4) header, 0.050" (1.27 mm) pitch, Gold, Vertical	M50-3530442	Harwin Inc.
26	Q1	1	30 V, 80A (Tc,) 110W (Tc), 2.8 mΩ @ 40 A, N-Channel, D-PAK	STD150N3LLH6	ST Micro
27	Q3	1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semi
28	Q4	1	NPN, DARL NPN 40 V SMD SOT23-3	MMBT6427-7-F	Diodes, Inc.
29	Q5	1	NPN, DARL NPN 40 V SMD SOT23-3	MMBT6427-7-F	Diodes, Inc.
30	R1	1	RES, 100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
31	R2	1	RES, 59 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5902V	Panasonic
32	R3	1	RES, 75 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ753V	Panasonic
33	R4	1	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
34	R5	1	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
35	R6	1	RES, SMD, 33 kΩ, 1%, 1/10W, ±100ppm/°C, 0603	RC0603FR-0733KL	Yageo
36	R7	1	RES, 18.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1822V	Panasonic
37	R9	1	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
38	R12	1	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
39	R13	1	RES, 2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ202V	Panasonic
40	R14	1	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
41	R15	1	RES, 15 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ153V	Panasonic
42	R16	1	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
43	R17	1	RES, 510 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5103V	Panasonic
44	R18	1	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
45	R19	1	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
46	R20	1	RES, 470 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ474V	Panasonic
47	R21	1	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
48	R22	1	RES, 470 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ474V	Panasonic
49	RL1	1	RELAY, GP, Dual coil, SPST, 16 A, 3 VDC coils, 277 VAC, PCPin	ADW1203HLW	Panasonic
50	RV1	1	275 VAC, 8.6 J, 5 mm, RADIAL	S05K275	Epcos
51	SW1	1	SWITCH, TACTILE, SPST-NO, 0.02A, 15V	EVQ-11K05B	Panasonic
52	T1	1	Bobbin, Generic		
53	TP1	1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

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54	TP2	1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
55	U1	1	LinkSwitch-TN2, SO-8C	LNK3202D	Power Integrations
56	U2	1	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N4J00F	Sharp
57	U3	1	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF/NOPB	Texas Instruments
58	U4	1	MDBT42Q, (Nordic nRF52832 BASED BLE MODULE)	317030213	Seeed
59	U6	1	IC, Comparator, General Purpose, Open Collector, SOT-23-5	TLV1701AIDBVR	Linear
60	U7	1	IC, Linear Voltage Regulator, 3 V, 0.25 A, SOT-89-3,	MCP1703T-3002E/MB	Microchip
61	VR1	1	DIODE, ZENER, 43 V, ±7%, 1W, PMDS,DO-214AC, SMA	PTZTE2543A	Rohm Semi
62	VR2	1	3.3 V, 5%, 150 mW, SSMINI-2	DZ2S033M0L	Panasonic
63	VR3	1	DIODE, ZENER, 7.5 V, ±5%, 500 mW, SOD123, 150°C	MMSZ4693T1G	ON Semi

7 Transformer Specification

7.1 *Electrical Diagram*

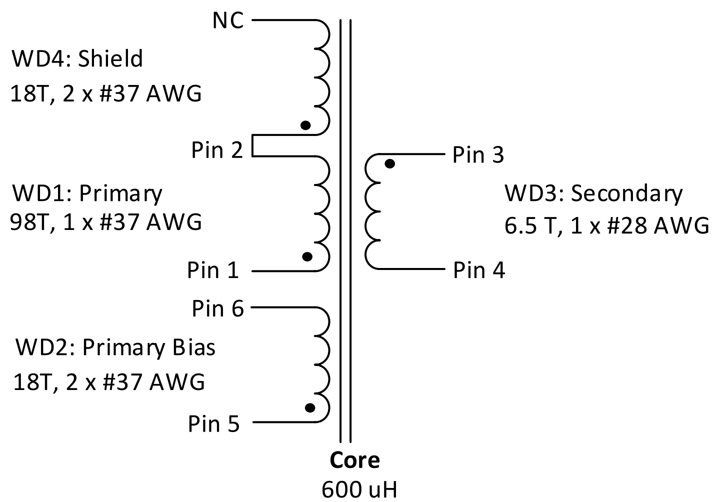

Figure 11 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz.	600 μH ±7%
Resonant Frequency	Pins 1-2, all other windings open.	1000 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with pins 3-6 shorted, measured at 100 kHz.	40 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE8.3.
[2]	Bobbin: EE8.3, Vertical, 6 pins (8.2mm W x 8.2mm L x 6.9mm H).
[3]	Magnet Wire: #37 AWG.
[4]	Magnet Wire: #28 AWG.
[5]	Polyester Tape: 4.5 mm.
[6]	Varnish.

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7.4 *Build Diagram*

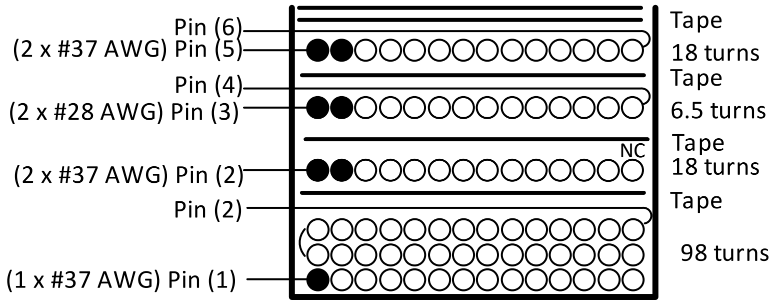

Figure 12 – Transformer Build Diagram.

7.5 *Construction*

Primary	Start at pin 1. Wind 98 turns of Item [3] in approximately 3 layers. Finish on pin 2.
Basic Insulation	Use 1 layer of Item [5] for basic insulation.
Shield	Start at pin 2. Wind 18T bifilar turns of Item [3] (1 layer). Leave the other end unterminated.
Basic Insulation	Use 1 layer of Item [5] for basic insulation.
Secondary Winding	Start at pin 3. Wind 6.5T bifilar turns of Item [4] (1 layer). Finish on pin 4.
Basic Insulation	Use 1 layer of Item [5] for basic insulation.
Bias Winding	Start at pin 5. Wind 18T bifilar turns of Item [3] (1 layer). Finish on pin 6.
Outer Wrap	Wrap windings with 2 layers of tape Item [5].
Final Assembly	Assemble and secure core halves so that the tape wrapped E core is at the bottom of the transformer.
Varnish	Dip varnish uniformly in Item [6]. Do not vacuum impregnate.

8 Transformer Design Spreadsheet

1	ACDC_LinkSwitchTN2_Flyback_021417; Rev.1.1; Copyright Power Integrations 2017	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchTN2 Flyback Design Spreadsheet
2	**ENTER APPLICATION VARIABLES**					
3	LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
4	VACMIN	90.00		90.00	Volts	Minimum AC line voltage
5	VACTYP			115.00	Volts	Typical AC line voltage
6	VACMAX			265.00	Volts	Maximum AC line voltage
7	fL			50	Hertz	AC mains frequency
8	TIME_BRIDGE_CONDUCTION			2.26	mseconds	Input bridge rectifier diode conduction time
9	LINE RECTIFICATION	F		F		Select 'F'ull wave rectification or 'H'alf wave rectification
10	VOUT	3.50		3.50	Volts	Output voltage
11	IOUT	0.060		0.060	Amperes	Average output current specification
12	CC THRESHOLD VOLTAGE	0.10		0.10	Volts	Voltage drop across the sense resistor
13	OUTPUT CABLE RESISTANCE			0.00	Ohms	Enter the resistance of the output cable (if used)
14	EFFICIENCY			0.80		Efficiency Estimate at output terminals. Under 0.8 if no better data available
15	LOSS ALLOCATION FACTOR			0.75		The ratio of power losses during the MOSFET off-state to the total system losses
16	POUT			0.22	Watts	Continuous Output Power
17	CIN			2.20	uFarads	Input capacitor
18	VMIN			119.31	Volts	Valley of the rectified VACMIN
19	VMAX			374.77	Volts	Peak of the VACMAX
20	FEEDBACK	OPTO		OPTO		Select the type of feedback required
21	BIAS WINDING	YES		YES		Select whether a bias winding is required
25	**LinkSwitch-TN2 VARIABLES**					
26	CURRENT LIMIT MODE	STD		STD		Pick between RED(Reduced) or STD(Standard) current limit mode of operation
27	PACKAGE	SO-8C		SO-8C		Device package
28	GENERIC DEVICE	Auto		LNK3202		Device series
29	DEVICE CODE			LNK3202D		Device code
30	VOR	70		70	Volts	Voltage reflected to the primary winding when the MOSFET is off
31	VDSON			10.0	Volts	MOSFET on-time drain to source voltage
32	VDSOFF			541.8	Volts	MOSFET off-time drain to source voltage
33	ILIMITMIN			0.126	Amperes	Minimum current limit
34	ILIMITTYP			0.136	Amperes	Typical current limit
35	ILIMITMAX			0.146	Amperes	Maximum current limit
36	FSMIN			62000	Hertz	Minimum switching frequency
37	FSTYP			66000	Hertz	Typical switching frequency
38	FSMAX			72000	Hertz	Maximum switching frequency
39	RDSON			88.40	Ohms	MOSFET drain to source resistance
43	**PRIMARY WAVEFORM PARAMETERS**					
44	MODE OF OPERATION			DCM		Mode of operation
45	KRP/KDP			15.631		Measure of continuous/discontinuous mode of operation
46	KP_TRANSIENT			5.111		KP under conditions of a transient
47	DMAX			0.043		Maximum duty cycle
48	TIME_ON			0.694	useconds	MOSFET conduction time at the minimum line voltage

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49	TIME_ON_MIN			0.284	useconds	MOSFET conduction time at the maximum line voltage
50	IAVG_PRIMARY			0.003	Amperes	Average input current
51	IRMS_PRIMARY			0.015	Amperes	Root mean squared value of the primary current
52	LPRIMARY_MIN			521	uH	Minimum primary inductance
53	LPRIMARY_TYP			579	uH	Typical primary inductance
54	LPRIMARY_MAX			637	uH	Maximum primary inductance
55	LPRIMARY_TOL			10		Primary inductance tolerance
59	**SECONDARY WAVEFORM PARAMETERS**					
60	IPEAK_SECONDARY			2.385	Amperes	Peak secondary current
61	IRMS_SECONDARY			0.341	Amperes	Root mean squared value of the secondary current
62	PIV_SECONDARY			26.44	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
63	VF_SECONDARY			0.70	Volts	Secondary diode forward voltage drop
67	**TRANSFORMER CONSTRUCTION PARAMETERS**					
68	Core selection					
69	CORE	EE8		EE8		Select the transformer core
70	BOBBIN			B-EE8-H		Select the bobbin
71	AE			7.00	mm^2	Cross sectional area of the core
72	LE			19.20	mm	Effective magnetic path length of the core
73	AL			610.0	nH/(turns^2)	Ungapped effective inductance of the core
74	VE			0.0	mm^3	Volume of the core
75	AW			0.00	mm^2	Window area of the bobbin
76	BW			4.78	mm	Width of the bobbin
77	MLT			0.00	mm	Mean length per turn of the bobbin
78	MARGIN			0.00	mm	Safety margin
80	**Primary winding**					
81	NPRIMARY			98		Prmary number of turns
82	BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
83	BMAX_ACTUAL			1232	Gauss	Actual value of the magnetic flux density
84	BAC			616	Gauss	AC flux density
85	ALG			60	nH/T^2	Gapped core effective inductance
86	LG			0.131	mm	Core gap length
87	LAYERS_PRIMARY	3		3		Number of primary layers
88	AWG_PRIMARY			37		Primary winding wire AWG
89	OD_PRIMARY_INSULATED			0.140	mm	Primary winding wire outer diameter with insulation
90	OD_PRIMARY_BARE			0.113	mm	Primary winding wire outer diameter without insulation
91	CMA_PRIMARY		Info	1314	mil^2/Amperes	The primary winding wire CMA is higher than 500 mil^2/Amperes: Decrease the primary layers or wire thickness
93	**Secondary winding**					
94	NSECONDARY	6		6		Secondary turns
95	AWG_SECONDARY			31		Secondary winding wire AWG
96	OD_SECONDARY_INSULATED			0.532	mm	Secondary winding wire outer diameter with insulation
97	OD_SECONDARY_BARE			0.227	mm	Secondary winding wire outer diameter without insulation
98	CMA_SECONDARY			234	mil^2/Amperes	Secondary winding CMA
100	**Bias winding**					
101	NBIAS	18		18		Bias turns
102	VF_BIAS			0.70	Volts	Bias diode forward voltage drop
103	VBIAS			12.90	Volts	Bias winding voltage
104	PIVB			81.73	Volts	Peak inverse voltage on the bias diode
105	CBP			0.1	uF	BP pin capacitor
109	**FEEDBACK PARAMETERS**					
110	DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
111	RUPPER			500 - 1000	ohms	Resistor divider component between bias winding and FB pin of LinkSwitch-TN2. See LinkSwitch-TN2

						Design Guide
112	RLOWER			200 - 820	ohms	Resistor divider component between FB pin of LinkSwitch-TN2 and primary RTN. See LinkSwitch-TN2 Design Guide

Note: Actual Rupper and Rlower values are higher than in the spreadsheet in order to further minimize the input current. The divider ratio was maintained.

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9 Performance Data

All measurements performed at room temperature. Unless otherwise stated, the test data refers to system-level performance.

9.1 *Standby Input Leakage Current*

Standby current was measured when the relay is OFF. A 40 W incandescent bulb was connected between Line Out and Neutral in order to complete the circuit loop. The leakage current, even with BLE connected, was kept below 200 μA at worst-case input voltage. At 230 VAC, the leakage current was below 100 μA.

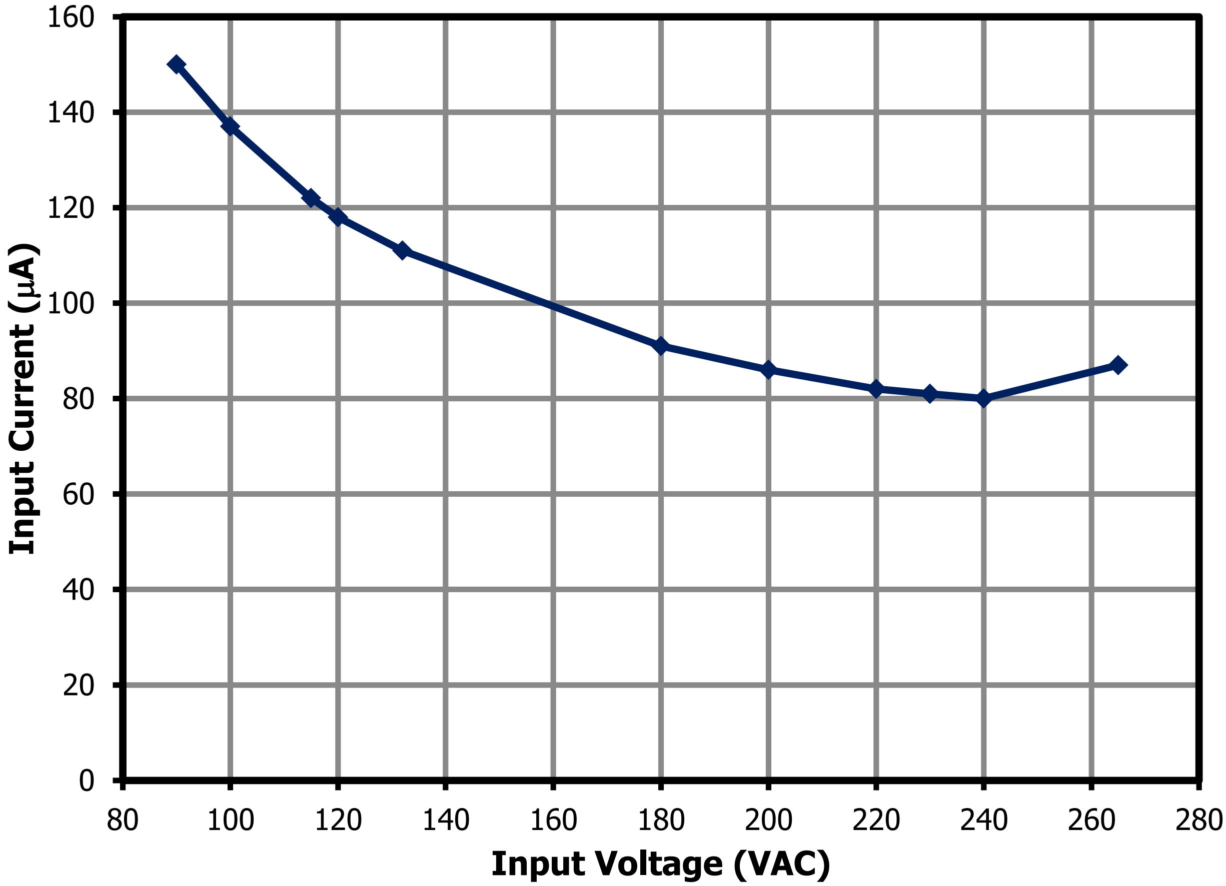

Figure 13 – Standby Input Current.

9.2 *LinkSwitch-TN2 Leakage Current vs. System-Level Leakage Current*

The leakage current contribution of the LinkSwitch-TN2 power supply was taken by disconnecting the LDO regulator from the circuit. System input current measurements were taken after adding the 3 V regulator and the BLE module.

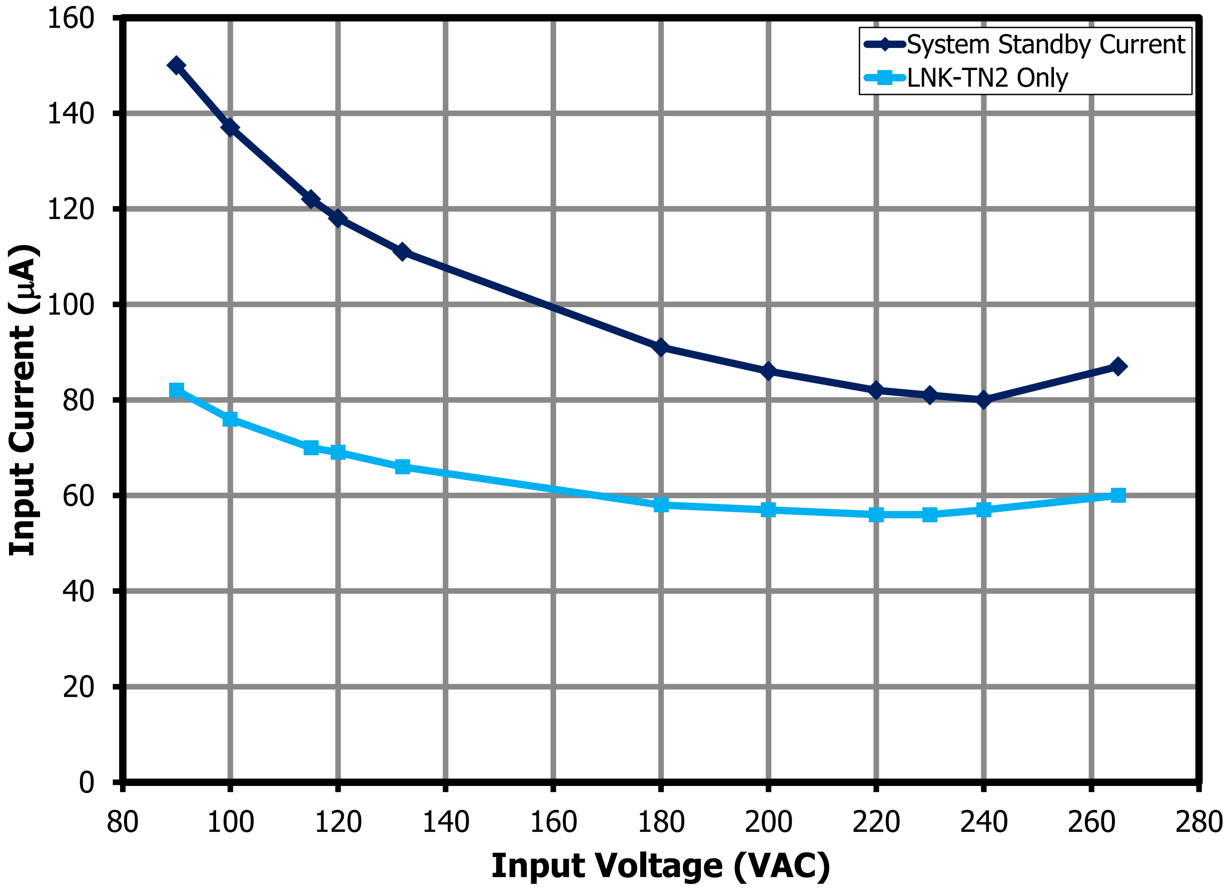

Figure 14 – LinkSwitch-TN2 Leakage Current vs. System Leakage.

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9.3 *LinkSwitch-TN2 Regulation vs. Load on 3 V Output, Relay OFF*

The isolated flyback design using LinkSwitch-TN2 LNK3202D is rated for 3.5 V, 60 mA output. Actual current capability increases as the input voltage increases as shown in the graph below.

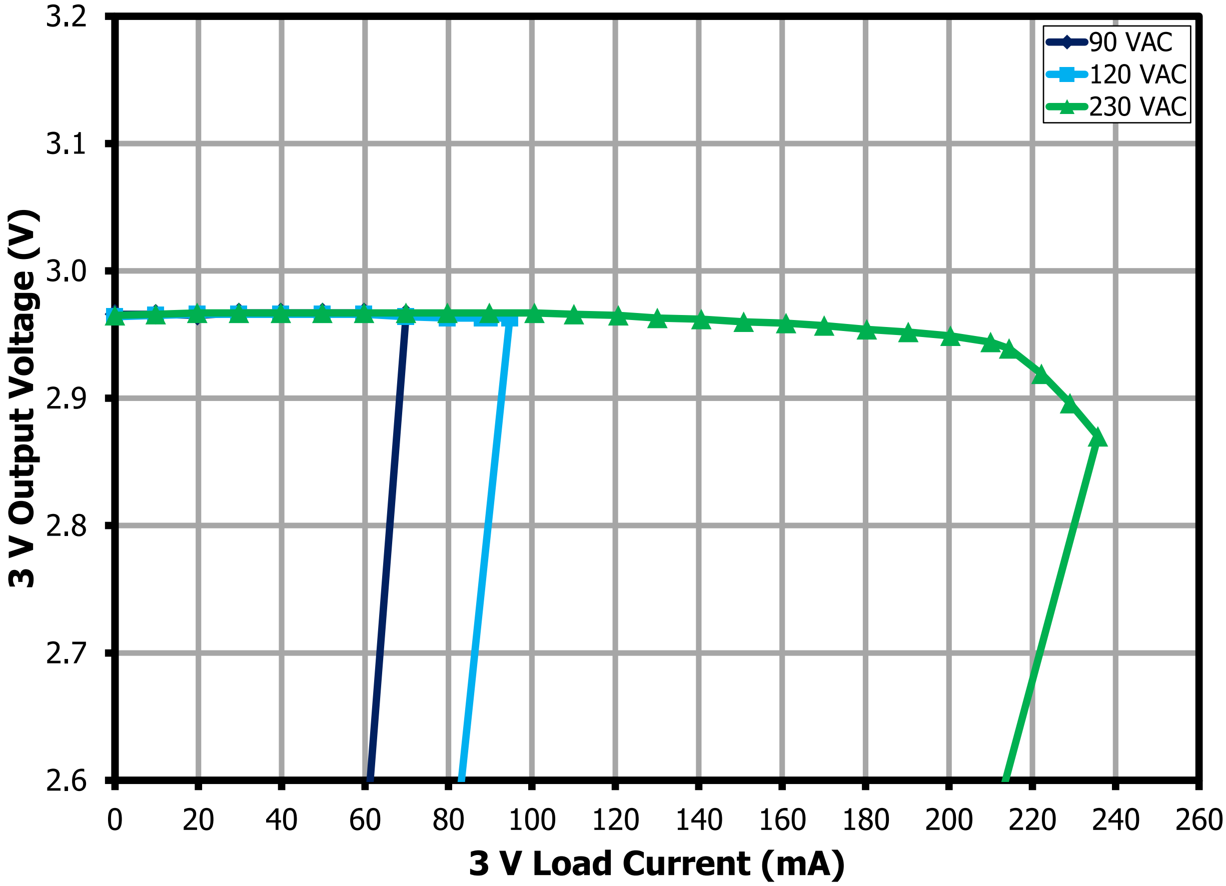

Figure 15 – LinkSwitch-TN2 Regulation vs. Load on 3 V Output.

9.4 *Maximum Continuous Load on 3 V Regulator Output, Relay ON*

Supply comes from the Q1 FET regulator.

The MOSFET Q1 regulator current capability is dependent on the characteristic of the load connected to the AC line. This is because the charging current needed to charge the capacitor that supplies power to the 3 V LDO regulator is limited by the current being drawn by the bulb load.

If this reference design is used on other wireless module, then the maximum load that the FET regulator can supply is shown on Figure 17. Also, as the 3 V load goes up, it is necessary to reduce or even short R18, increase C13, C14, and C15, as well as use a higher current-rated 3 V linear regulator.

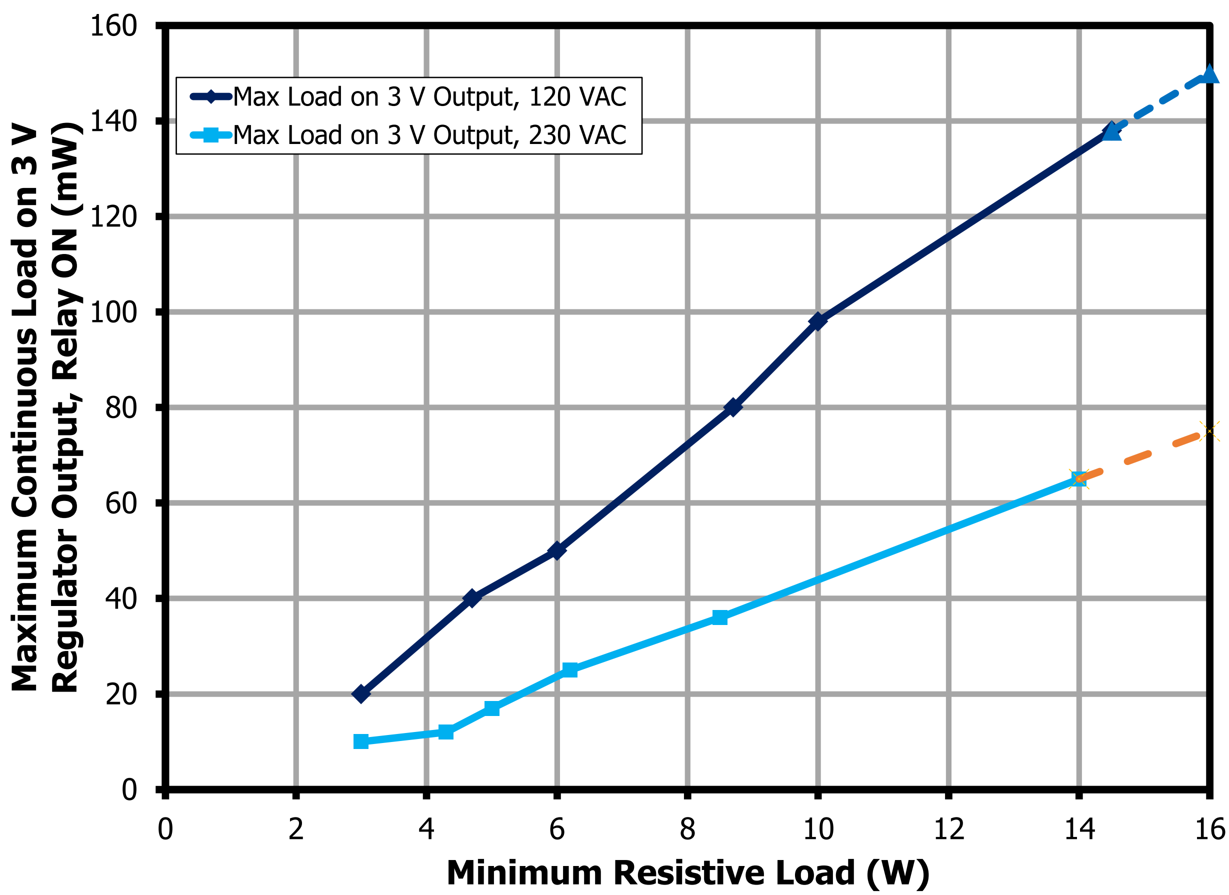

Figure 16 – Maximum Continuous Load on 3 V Regulator Output vs. Resistive Load (Connected to AC Line).

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10 Waveforms

10.1 *LinkSwitch-TN2 Drain Voltage, Normal Operation, Relay OFF*

The VDS stress on LinkSwitch-TN2 kept below 80% of rated BV_{DSS} at nominal input (230 VAC). No primary snubber was used. For designs that require higher power, an R-C-D snubber may be added.

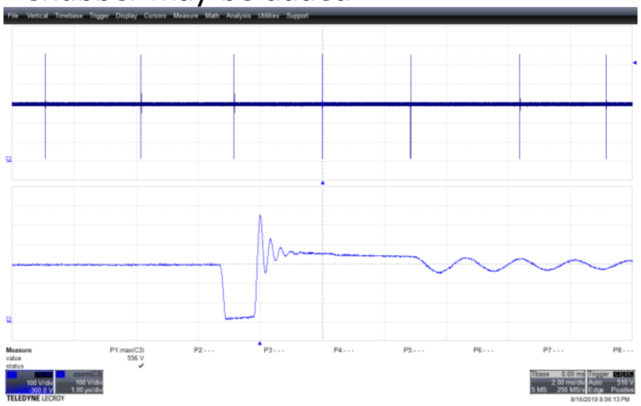

Figure 17 – Drain Voltage, 230 VAC, 50 Hz.
CH3: V_{DRAIN}, 100 V / div.
VDS Max: 556 V Peak.

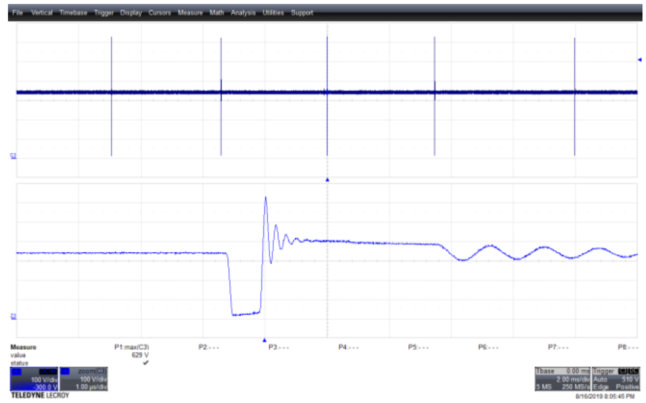

Figure 18 – Drain Voltage, 265 VAC, 50 Hz.
CH3: V_{DRAIN}, 100 V / div.
VDS Max: 629 V Peak.

10.2 *Output Waveforms, Start-up, Relay OFF*

No huge overshoot/undershoot on the 3 V LDO output.

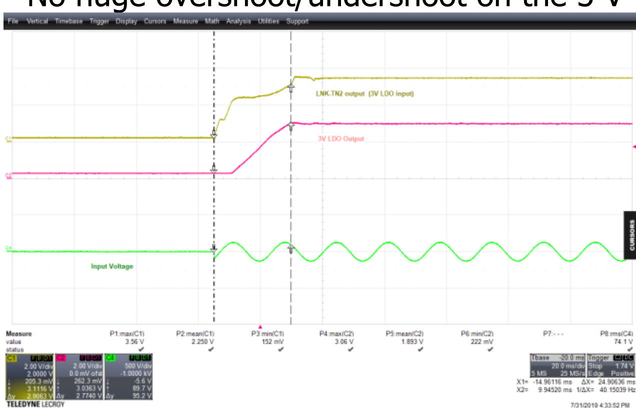

Figure 19 – Output Waveforms, Start-up at 90 VAC, 60 Hz, Relay OFF.
CH1: LinkSwitch-TN2 Output Voltage (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

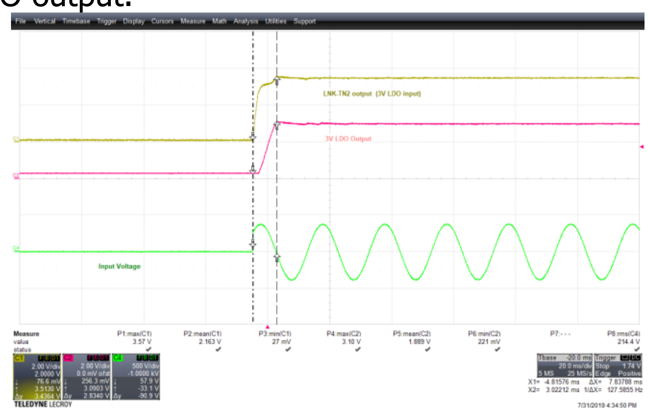

Figure 20 – Output Waveforms, Start-up at 265 VAC, 50 Hz, Relay OFF.
CH1: LinkSwitch-TN2 Output Voltage (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

10.3 *Output Waveforms, Start-up, Relay ON*

With the relay already ON, the supply comes from the output of the Q1 regulator circuit.

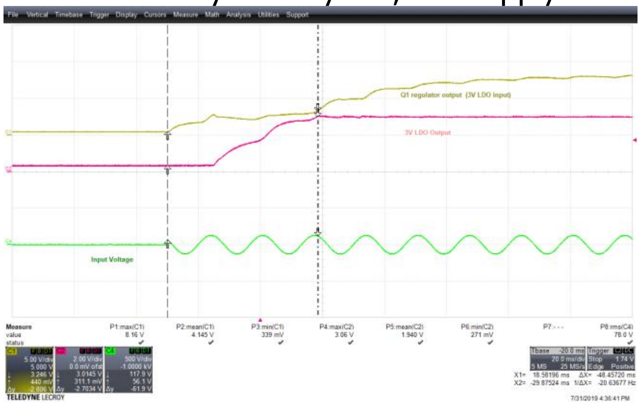

Figure 21 – Output Waveforms, Start-up at 90 VAC, 60 Hz, Relay ON.
CH1: Q1 Regulator Output (LDO input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

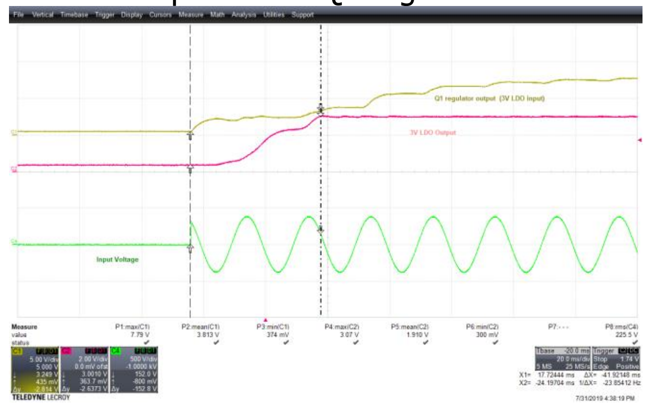

Figure 22 – Output Waveforms, Start-up at 265 VAC, 50 Hz, Relay ON.
CH1: Q1 Regulator Output (LDO input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

10.4 *Output Waveforms, Steady-State, Relay OFF*

When the relay is OFF, the supply comes from LinkSwitch-TN2 output voltage.

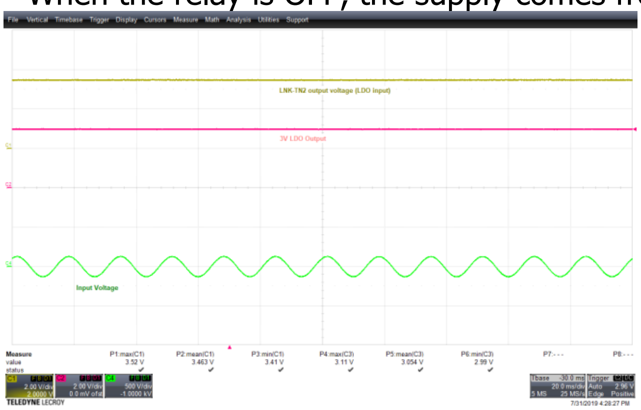

Figure 23 – Output Waveforms, Steady-State, 90 VAC, 60 Hz, Relay OFF.
CH1: LinkSwitch-TN2 Output Voltage (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

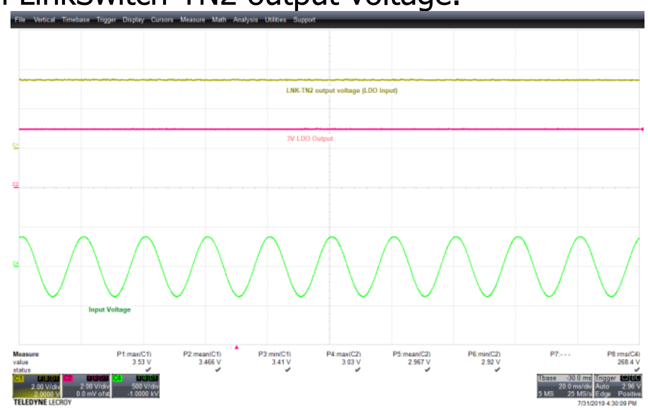

Figure 24 – Output Waveforms, Steady-State, 265 VAC, 50 Hz, Relay OFF.
CH1: LinkSwitch-TN2 Output Voltage (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage

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10.5 *Output Waveforms, Steady-State, Relay ON*

When the relay is ON, the supply comes from the output of the Q1 regulator circuit.

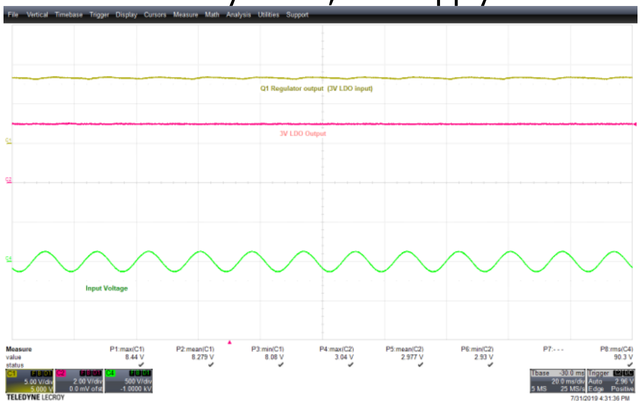

Figure 25 – Output Waveforms, Steady-state, 90 VAC, 60 Hz, Relay ON.
CH1: Q1 Regulator Output (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

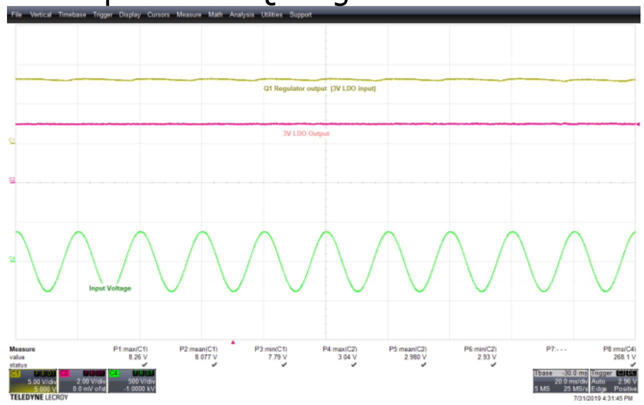

Figure 26 – Output Waveforms, Steady-state, 265 VAC, 50 Hz, Relay ON.
CH1: Q1 Regulator Output (LDO Input).
CH2: 3 V LDO Output.
CH4: Input AC Voltage.

10.6 *Output Waveforms, Relay OFF to ON Transition*

No huge overshoot/undershoot on the 3 V LDO output during the transition.

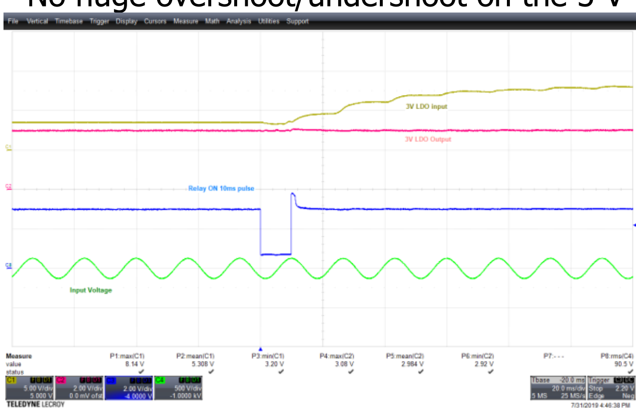

Figure 27 – Output Waveforms, 90 VAC, 60 Hz, Relay OFF to ON Transition.
CH1: 3 V LDO Input.
CH2: 3 V LDO Output.
CH3: Relay ON Drive Pulse.
CH4: Input AC Voltage.

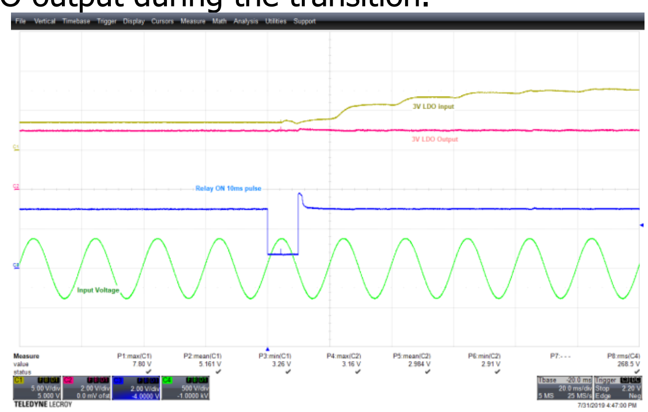

Figure 28 – Output Waveforms, 265 VAC, 50 Hz, Relay OFF to ON Transition.
CH1: 3 V LDO Input.
CH2: 3 V LDO Output.
CH3: Relay ON Drive Pulse.
CH4: Input AC Voltage.

10.7 *Output Waveforms, Relay ON to OFF Transition*

No huge overshoot/undershoot on the 3 V LDO output during the transition.

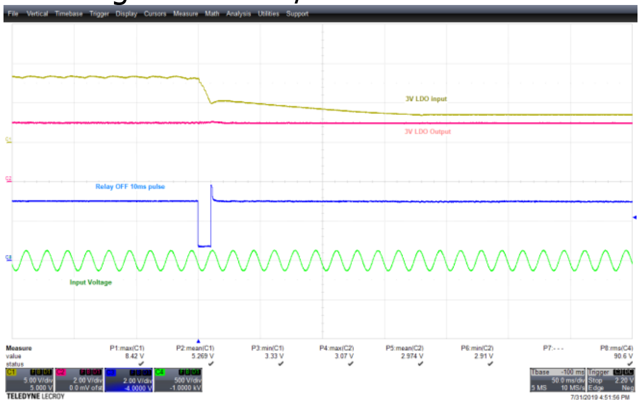

Figure 29 – Output Waveforms, 90 VAC, 60 Hz, Relay ON to OFF Transition.
CH1: 3 V LDO Input.
CH2: 3 V LDO Output.
CH3: Relay OFF Drive Pulse.
CH4: Input AC Voltage.

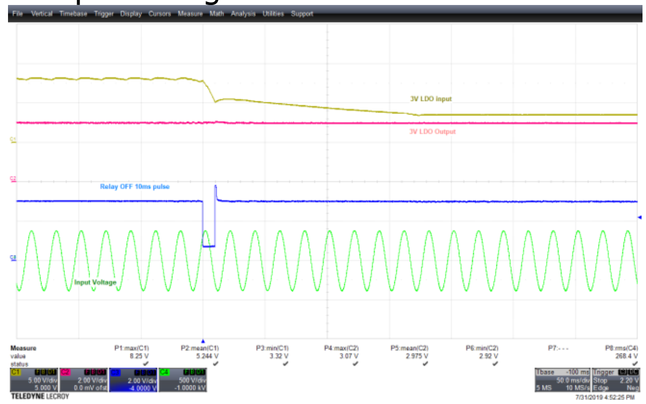

Figure 30 – Output Waveforms, 265 VAC, 50 Hz, Relay ON to OFF Transition.
CH1: 3 V LDO Input.
CH2: 3 V LDO Output.
CH3: Relay OFF Drive Pulse.
CH4: Input AC Voltage.

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10.8 *Q1 Regulator Waveforms*

The regulator circuit works on either 50 Hz or 60 Hz system.

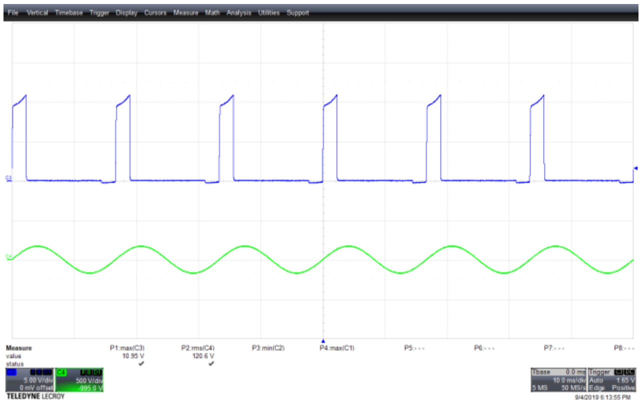

Figure 31 – Q1 VDS Waveform, 120 VAC, 60 Hz, Relay ON.
CH3: Q1 V_{DRAIN}.
CH4: Input AC Voltage.

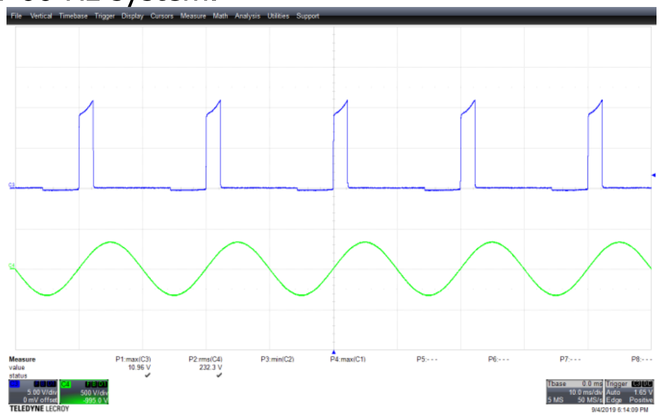

Figure 32 – Q1 VDS Waveform, 230 VAC, 50 Hz, Relay ON.
CH3: Q1 V_{DRAIN}.
CH4: Input AC Voltage.

11 Thermals

11.1 *Thermals, Relay ON*

The thermal data was taken using a total of 500 W incandescent bulb load.

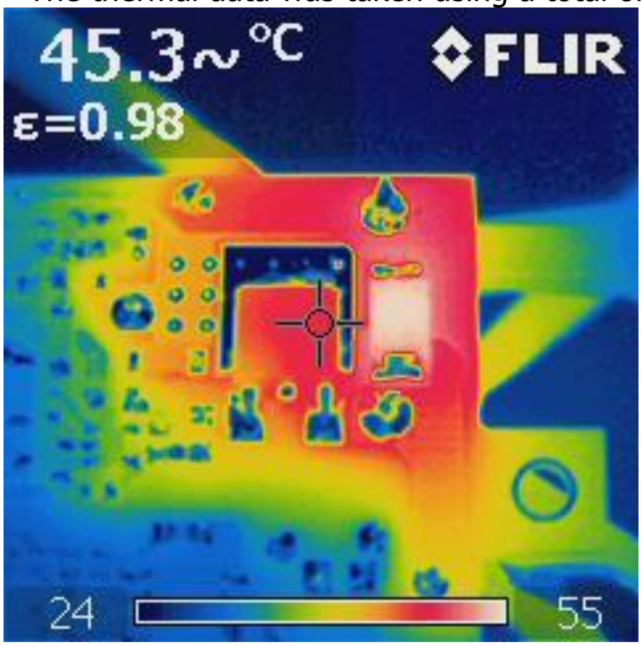

Figure 33 – Q1 Thermal, 120 VAC, 60 Hz.

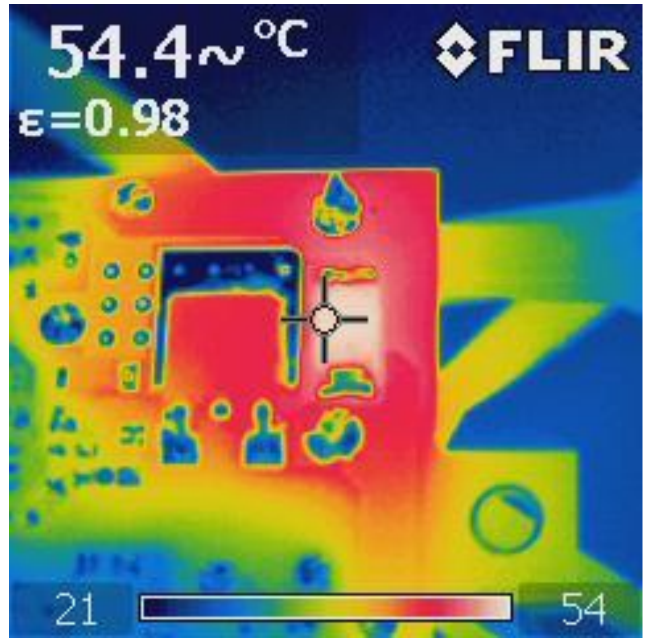

Figure 34 – D7 Thermal, 120 VAC, 60 Hz .

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11.2 *Thermals, Relay OFF*

When the relay is OFF, the power supply comes from the Linkswitch-TN2 circuit. The thermal data, however, was taken using simulated load on the 3 V output in order to verify the performance if the same design will be used on higher power design up to its rated limit.

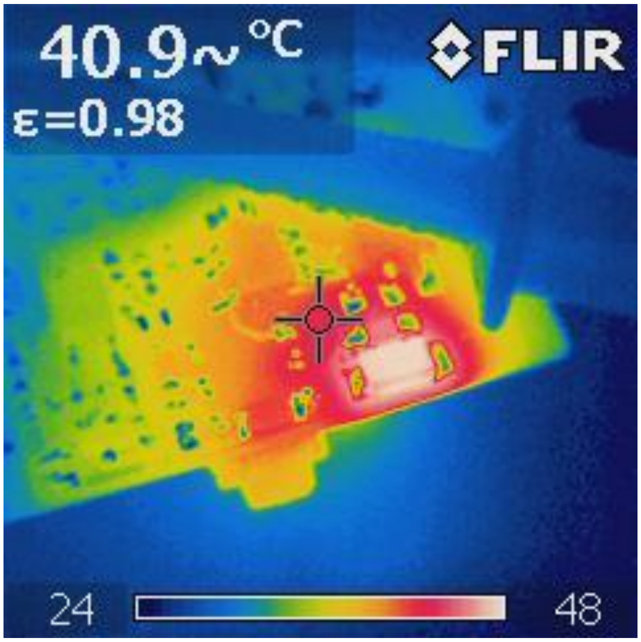

Figure 35 – LinkSwitch-TN2 U1 Thermal, 90 VAC, 60 Hz. 3 V Load: 60 mA.

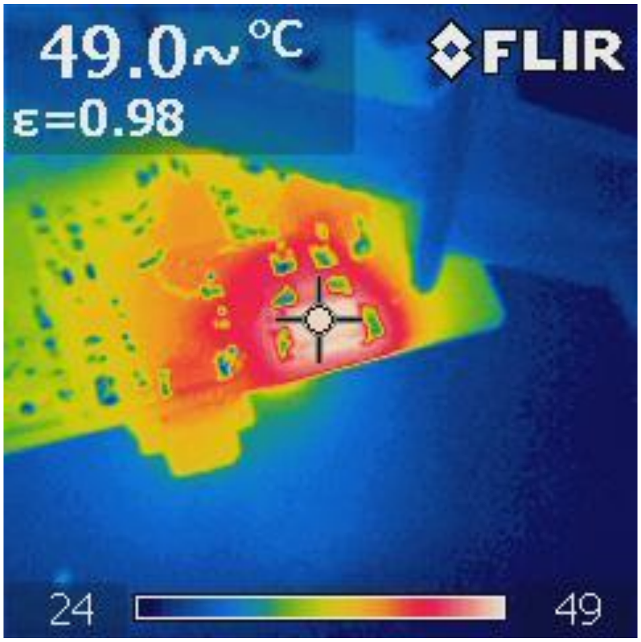

Figure 36 – VR1 Thermal, 90 VAC, 60 Hz. 3 V Load: 60 mA.

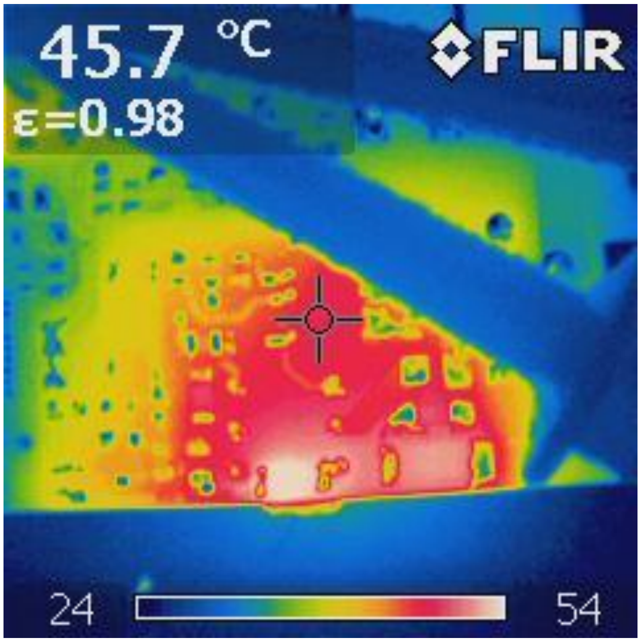

Figure 37 – U1 Thermal, 265 VAC, 50 Hz.
3 V Load: 200 mA.

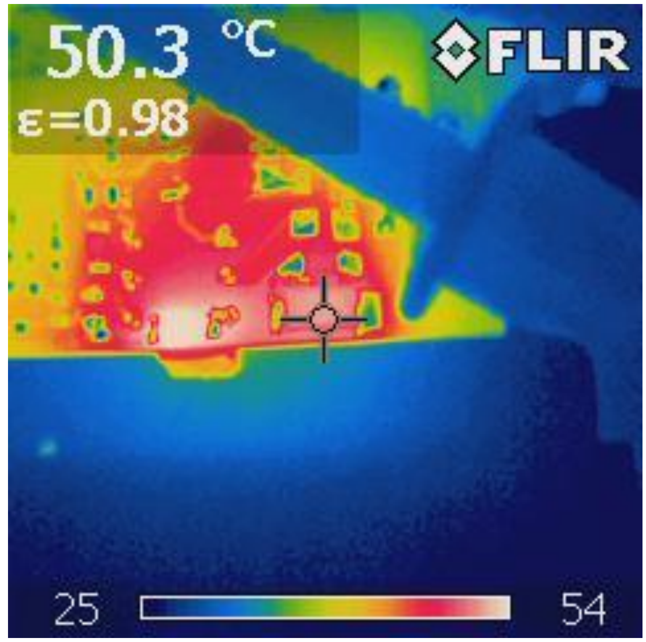

Figure 38 – VR1 Thermal, 265 VAC, 50 Hz.
3 V Load: 200 mA.

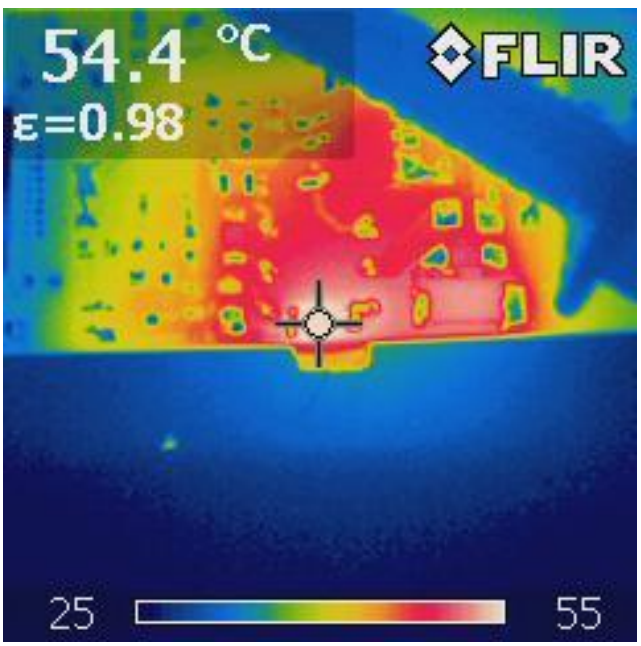

Figure 39 – D2 Thermal, 265 VAC, 50 Hz.
3 V Load: 200 mA.

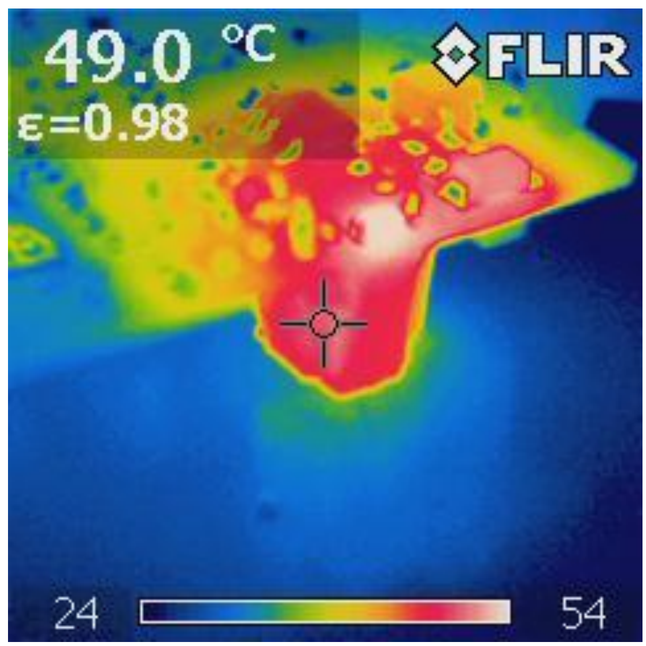

Figure 40 – VR1 Thermal, 265 VAC, 50 Hz,
3 V Load: 200 mA.

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12 Conducted EMI

Conducted EMI was tested when the relay is OFF. This was to check the emission of LinkSwitch-TN2 only. When the relay is ON, LinkSwitch-TN2 does not switch anymore and only the Q1 regulator is operational. Since the regulator switches every AC line cycle, it is possibly to get worse EMI than when a bulb is directly connected to the line. However, this response is analogous to a typical triac dimmer that 'chops' the line voltage and causes incident emission which is acceptable as per FCC part 15 standard. Hence, this DER does not address EMI issue that may arise due to the Q1 regulator.

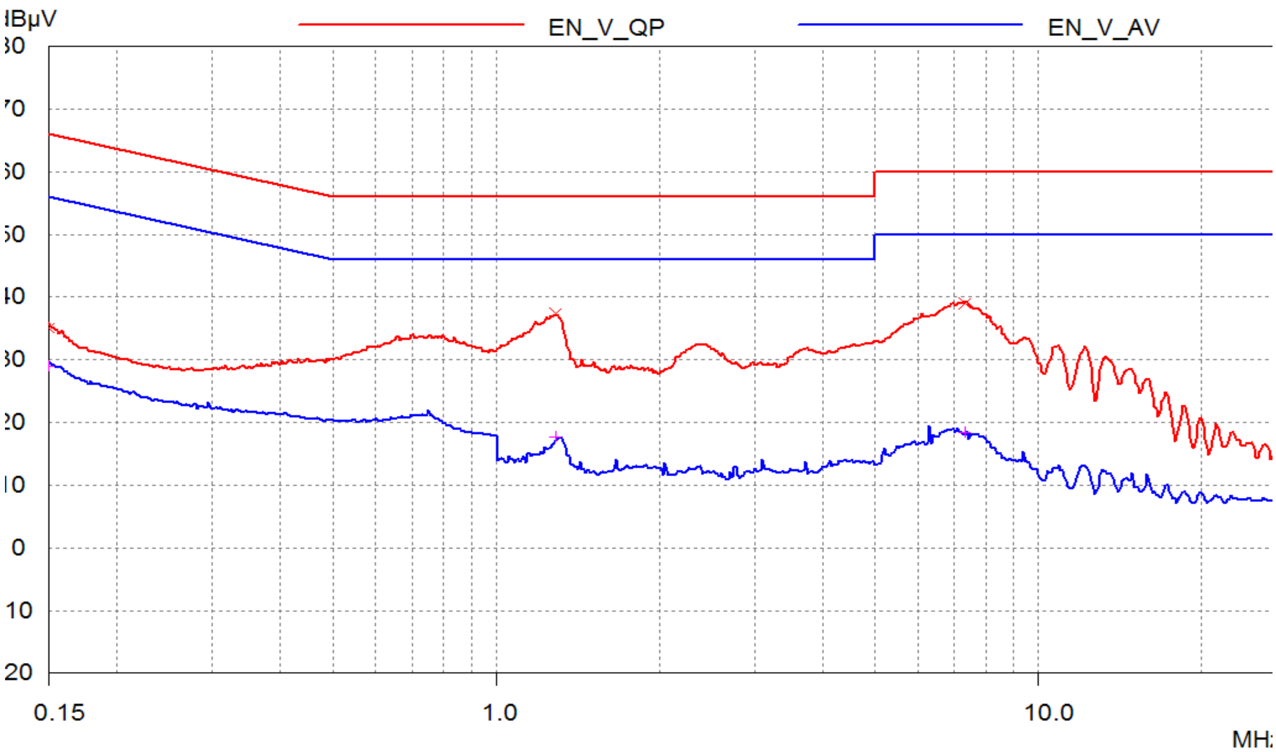

Figure 41 – Conducted Emission, 120 VAC, 60 Hz.

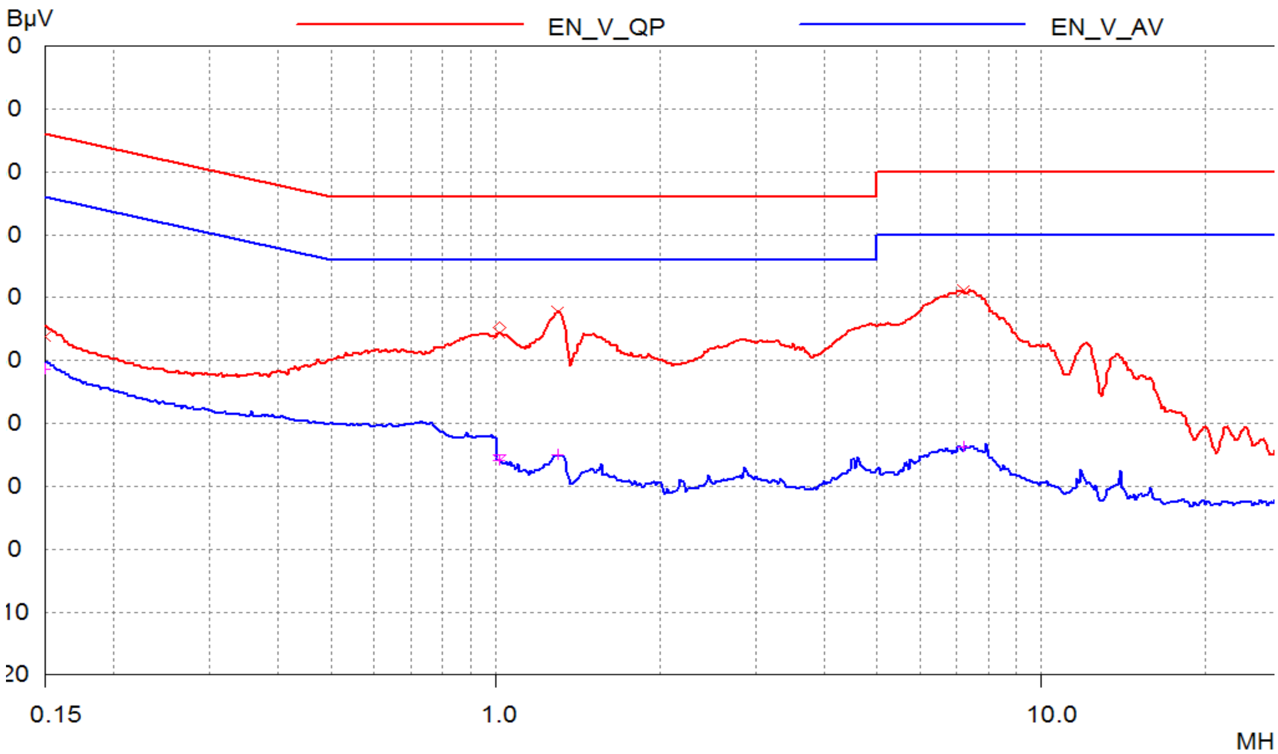

Figure 42 – Conducted Emission, 230 VAC, 60 Hz.

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13 Line Surge Testing

The unit was subjected to ±2500 V, 100 kHz ring wave and ±500 V differential surge with 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage. The test was done with the relay in OFF position, and with an incandescent bulb in order to close the circuit loop.

13.1 *Differential Line Surge Test Results*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Line Impedance	Test Result (Pass/Fail)
+500	230	L to N	0	2Ω	Pass
-500	230	L to N	0	2Ω	Pass
+500	230	L to N	90	2Ω	Pass
-500	230	L to N	90	2Ω	Pass
+500	230	L to N	270	2Ω	Pass
-500	230	L to N	270	2Ω	Pass

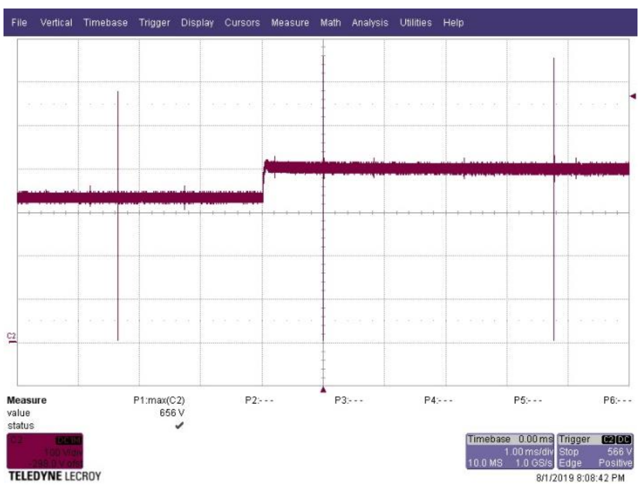

Figure 43 – (+500 V, 90°) Differential Line Surge, 230 VAC, 60 Hz. $V_{DS(MAX)}$: 656 V Peak.

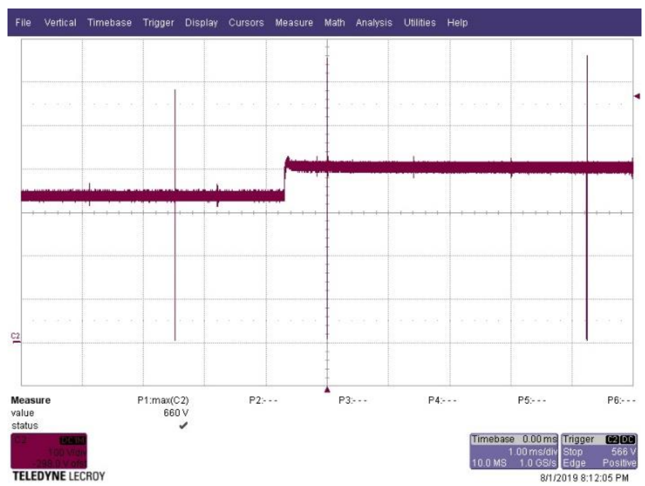

Figure 44 – (-500 V, 270°) Differential Line Surge, 230 VAC, 60 Hz. $V_{DS(MAX)}$: 660 V Peak.

13.2 *Ring Wave Test Results*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Line Impedance	Test Result (Pass/Fail)
+2500	230	L to N	0	12Ω	Pass
-2500	230	L to N	0	12Ω	Pass
+2500	230	L to N	90	12Ω	Pass
-2500	230	L to N	90	12Ω	Pass
+2500	230	L to N	270	12Ω	Pass
-2500	230	L to N	270	12Ω	Pass

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14 Appendix A – Current-Shaping Circuit Optimization

The proprietary current-shaping circuit using R1 and VR1 improves the power factor of the circuit, which results to lower standby input current. The optimized value to maximize PF depends on the amount of load that is being drawn by the circuit. In this DER, since the overall system consumption is very low, then a value of 100 kΩ can be used. The Zener voltage was set to 43 V so that Linkswitch-TN2 would still operate properly even if the available bulk voltage on C1 is reduced by 43 V.

If the system current consumption is higher, such as when using different wireless module with higher standby current, then the value of R1 needs to be re-tuned accordingly. Maximum PF can be achieved by setting the resistor value such that the voltage across the resistor is slightly below the Zener voltage. Figure 45 shows the graph of recommended R1 value for various 3 V load current.

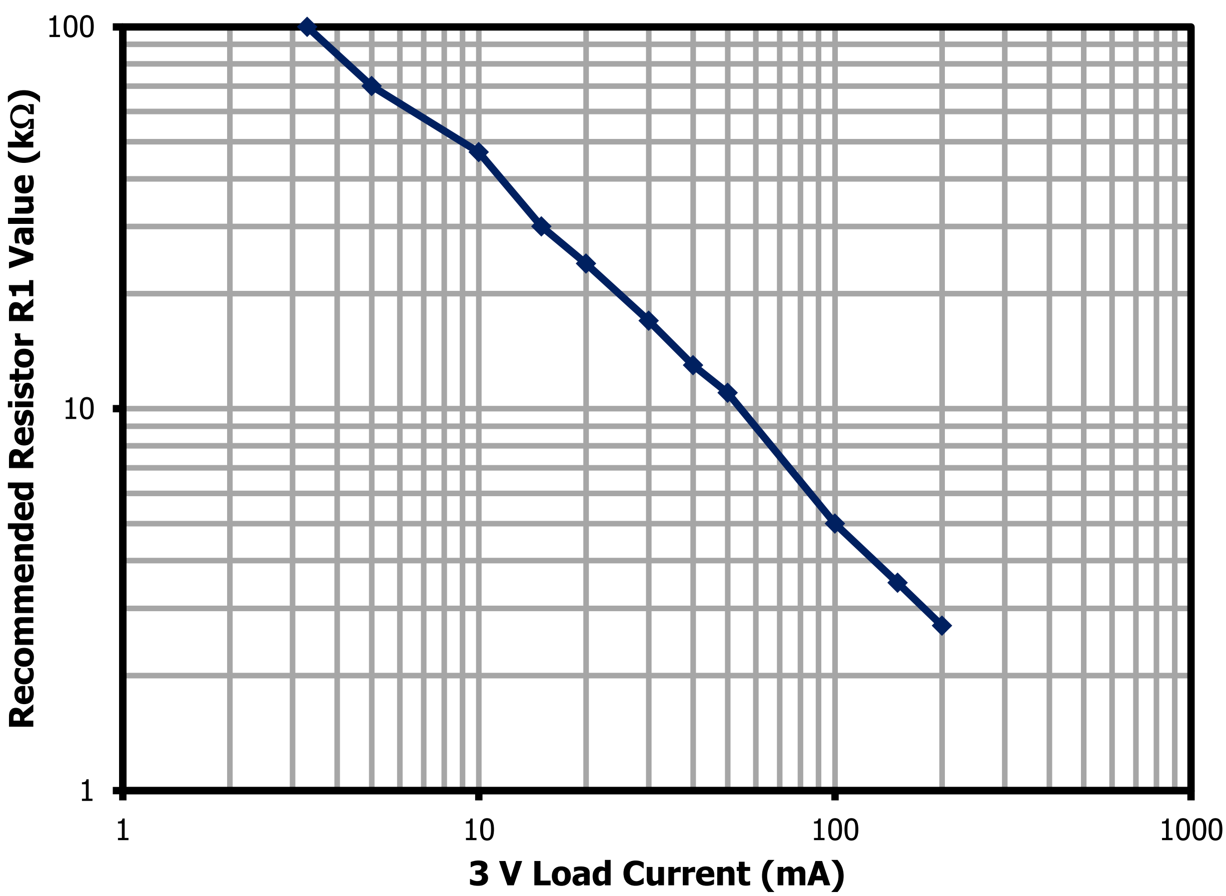

Figure 45 – Recommended R1 Value For Various Load on the 3 V Regulator.

15 Revision History

Date	Author	Revision	Description & changes	Reviewed
18-Sep-19	DL / DS	1.0	Initial Release.	Apps & Mktg

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