Design Example Report

Title	***60 W Power Supply Using InnoSwitch™4-CZ PowiGaN™ INN4075C-H180 and ClampZero™ CPZ1075M***
Specification	90 VAC – 265 VAC Input; 20 V / 3.0 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	DER-943
Date	March 24, 2023
Revision	1.1

Summary and Features

- InnoSwitch4-CZ – active clamp flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- Zero voltage switching in both CCM and DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- >95% full-load efficiency at 230 VAC
- >94.5% full-load efficiency at 115 VAC
- 93.9% full-load efficiency at 90 VAC, meets DOE6 and CoC v5 2016 efficiency requirement
- High power density: 28.45 W/in^3
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <60 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B conducted EMI

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency-approved. Therefore, all testing should be performed using an isolation transformer to provide AC input to the prototype board.

1 Introduction

This engineering report describes a 60 W 20 V 3 A output power supply using InnoSwitch4-CZ INN4075C-H180 and ClampZero CPZ1075M. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-CZ active clamp flyback controller providing exceptional performance.

This document contains the power supply specifications, schematic diagram, bill of materials (BOM), printed circuit board (PCB) layout, transformer documentation, and performance data.

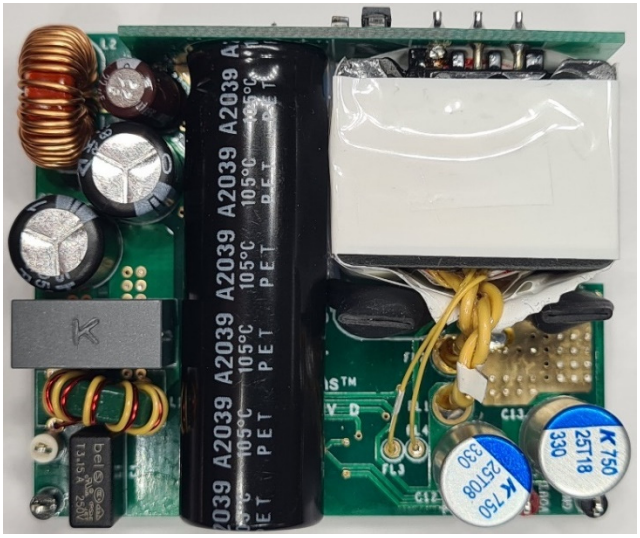


Figure 1 – Populated Circuit Board Photograph, Top.

Figure 2 – Populated Circuit Board Photograph, Bottom.

Note: Component VR3, although present in the board photo, should not be installed.

2 Power Supply Specification

The table below provides the electrical specification and minimum acceptable performance of the power supply design. Actual performance is provided in the performance data section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power	P_{IN}		53.23		mW	Measured at 230 VAC.
Output						
Voltage	V_{OUT}		20.0		V	< ± 2% Voltage Regulation.
Current	I_{OUT}		3.0		A	3.24 A Constant Current Mode Regulation.
Continuous Power	P_{OUT}			60	W	
Voltage Ripple				<250	mV	Measured at PSU output terminals. (20 MHz Bandwidth)
Efficiency						
Full Load Efficiency	$\eta_{100\% LOAD}$		95.3		%	Measured at 230 VAC.
Average Efficiency	$\eta_{AVERAGE}$		94.8		%	
10% Load Efficiency	$\eta_{10\% LOAD}$		91.1		%	
Conducted EMI						Meets CISPR22 / EN55022B.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection at Sea Level.

Table 1 – DER-943 Power Supply Specifications.

3 Schematic

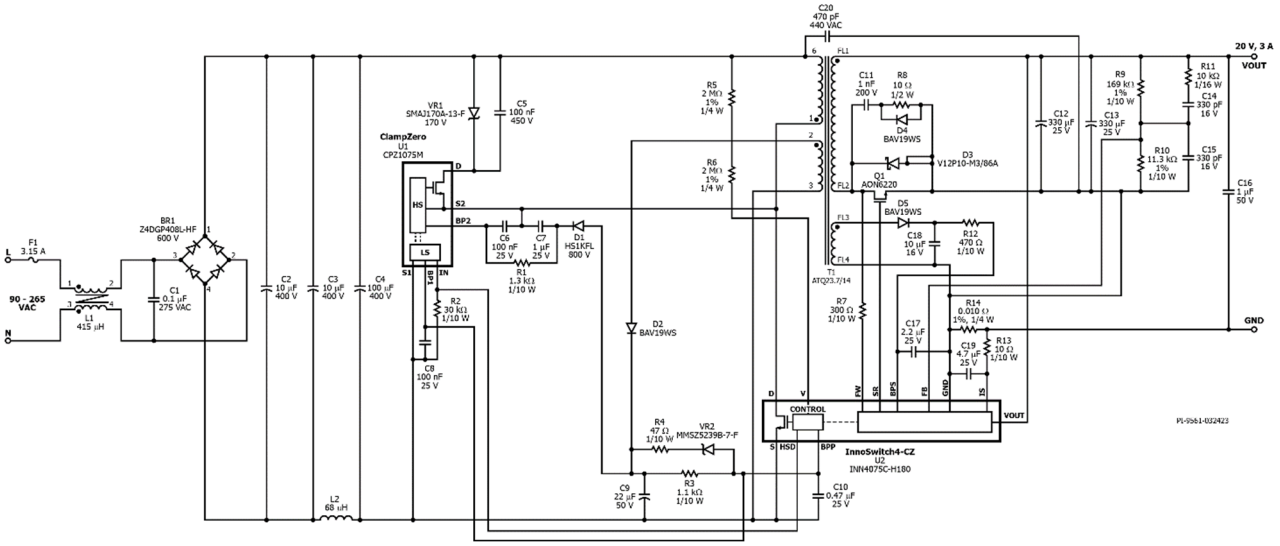


Figure 3 – Schematic.

4 Circuit Description

4.1 *Input Rectifier and EMI Filtering*

Input fuse F1 isolates the circuit and provides protection from component failure. Inductor L1, and L2, along with the capacitor C1 provides EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectifier DC across the input capacitors C2, C3, and C4. Y-capacitor C20 connected between the power supply output and input helps to reduce common-mode EMI.

4.2 *InnoSwitch4-CZ IC Primary*

One end of the transformer T1 primary winding is connected to the rectified DC bus, while the other is connected to the drain pin of the PowiGaN switch inside the InnoSwitch4-CZ IC (U2).

Resistors R5 and R6 connected to the V pin provide input voltage sensing for the InnoSwitch4-CZ IC. The value of the bypass capacitor C10 was chosen based on the desired current limit of the InnoSwitch4-CZ IC. The BPP pin of the InnoSwitch4-CZ IC also supplies the ClampZero IC (U1).

The primary clamp capacitor C5 limits the peak drain voltage of the PowiGaN switch inside the InnoSwitch4-CZ IC. The energy stored in the leakage inductance of the transformer T1 is transferred to capacitor C5. Part of the magnetizing energy is also transferred to capacitor C5 depending on the capacitance value used. Zener diode VR1 acts as fail-safe to protect the InnoSwitch4-CZ IC from excessive drain voltage if there is any malfunction in the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ IC generates an HSD signal to turn on the ClampZero IC device. When the ClampZero IC turns on, to achieve soft switching of the InnoSwitch4-CZ primary switch, clamp capacitor C5 starts to charge the leakage inductance of the transformer during CCM operation and both the leakage and magnetizing inductance of the transformer during DCM operation. A small delay from the high-side switch turn off is provided to achieve zero voltage switching on the primary switch. This delay is programmable by the value of resistor R2.

Capacitor C8 is used to provide local decoupling at the BP1 pin of ClampZero IC. Capacitor C6 provides the decoupling for the BP2 pin. Diode D1 and capacitor C7 forms a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R1 limits the current flowing into the BP2 pin.

The InnoSwitch4-CZ IC is self-starting, using an internal high-voltage current source to charge the primary bypass pin capacitor C10, when AC is first applied. During normal operation, the primary-side section is powered by a bias winding on the transformer T1. Output of this bias winding is rectified using diode D2 and filtered using capacitor C9 to

provide a constant voltage source to supply the BPP pin of InnoSwitch4-CZ IC. Resistor R3 limits the current being supplied to the primary bypass pin of the InnoSwitch4-CZ IC.

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of the switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range, and at light load or no-load, most cycles are disabled, while the cycles that are enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the primary switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is achieved using Zener diode VR2 and the current limiting resistor R4. In a flyback converter, the output of the bias winding tracks the output voltage of the converter by winding turns-ratio. In case of overvoltage at the output of the converter, the bias winding voltage increases and causes Zener diode VR2 to breakdown, which then causes a current to flow into the BPP pin of the InnoSwitch4-CZ IC. If the current flowing in the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-CZ IC auto-restarts to prevent any further increase in output voltage.

4.3 *InnoSwitch4-CZ IC Secondary*

The secondary-side of the InnoSwitch4-CZ IC provides the output voltage and output current sensing, and a signal to drive a SR FET providing synchronous rectification. The secondary winding of the transformer T1 is rectified by SR FET Q1 and diode D3 then filtered by capacitors C12 and C13. Capacitor C16 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber formed by resistor R8, capacitor C11, and diode D4. Diode D4 minimizes the dissipation in resistor R8.

The gate of SR FET Q1 is turned on by the secondary-side controller of InnoSwitch4-CZ IC, based on the winding voltage sensed via resistor R7 fed into the FWD pin of the InnoSwitch4-CZ IC. In continuous conduction of operation, the SR FET is turned off prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous conduction mode of operation, the SR FET is turned off when the voltage drop across it falls below $V_{SR(TH)}$.

The secondary-side of the InnoSwitch4-CZ IC is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve system efficiency, a bias winding circuit was used. Diode D5 rectifies the output of the secondary bias winding and capacitor C18 provides filtering. Resistor R12 limits the current being supplied to the BPS pin of the InnoSwitch4-CZ IC. Capacitor C17 provides local decoupling to the BPS pin of InnoSwitch4-CZ IC.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing resistors

R9 and R10. The voltage across resistor R10 is fed into the FB pin of InnoSwitch4-CZ IC with an internal reference voltage of 1.265 V. Capacitor C15 provides noise filtering of the signal at the FB pin.

Output current is sensed by monitoring the voltage drop across resistor R14 between the IS and secondary GND pins with a threshold of approximately 35 mV. Resistor R13 and capacitor C19 provides filtering for the IS pin. Once the internal current sense threshold is exceeded, the device regulates the number of switching cycles to maintain a fixed output current. Resistor R14 also acts as a backup protection in case of output short-circuit.

5 Printed Circuit Board Layout

PCB thickness is 0.040 inches with a copper thickness of 2 ounces.

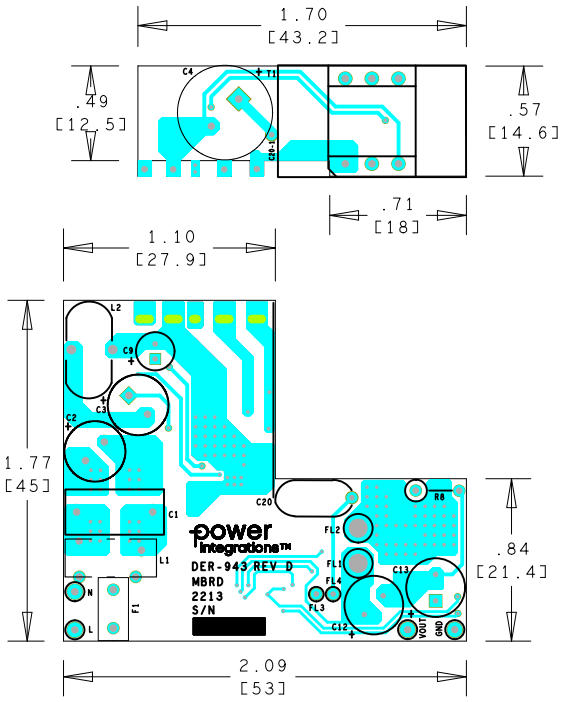


Figure 4 – Printed Circuit Layout, Top.

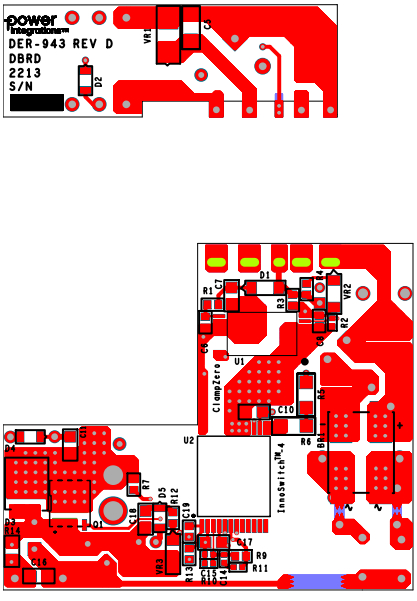


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	0.1 μF, X2, Film, 275 V 560 V, Polypropylene (PP), Metallized Radial, L 13.00 mm x W 6.00 mm x H 12.10 mm	R46KF310000M1K	KEMET
3	2	C2 C3	10 μF, 400 V, 20%, Electrolytic, (8 x 11), 3.5 mm lead spacing, Radial, Can, 2000 Hrs @ 105 °C	ERK2GM100F11OTO	AiSHi
4	1	C4	100 μF, 400 V, Aluminum Electrolytic, Radial, Can - 2000 Hrs @ 105 °C, (12.5 x 42)	400HXW100MEFR12.5X40	Rubycon
5	1	C5	100 nF, 450 V, Ceramic, X7T, 1206	C3216X7T2W104K160AA	TDK
6	2	C6 C8	100 nF, 0.1 μF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
7	1	C7	1 μF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
8	1	C9	22 μF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
9	1	C10	0.47 μF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
10	1	C11	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
11	2	C12 C13	330 μF, ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105 °C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
12	2	C14 C15	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
13	1	C16	1 μF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
14	1	C17	2.2 μF, ±10%, 25 V, Ceramic, X7R, 0805	CL21B225KAFNFNE	Samsung
15	1	C18	10 μF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
16	1	C19	4.7 μF ±20% 25 V Ceramic X5R 0603	GRT188R61E475ME13D	Murata
17	1	C20	470 pF, ±10%, 440 VAC, (X1, Y2) rated, Ceramic, Y5S, Radial, Disc, -40°C ~ 125°C	VY2471K29Y5SS63V7	Vishay
18	1	D1	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
19	3	D2 D4 D5	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
20	1	D3	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay
21	1	F1	3.15 A, 250 V, Slow, RST	RST 3.15-BULK	Belfuse
22	2	GND L	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
23	1	L1	415 μH, Toroidal Common Mode Choke, custom, wound on 32-00330-00 core	32-00412-00	Power Integrations
24	1	L2	68 μH, Unshielded Toroidal Inductor, 2 A, 55 mΩ Max, Radial, Vertical (Open)	7447033	Wurth
25	1	N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
26	1	Q1	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
27	1	R1	RES, 1.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ132V	Panasonic
28	1	R2	RES, 30 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ303X	Panasonic
29	1	R3	RES, 1.1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ112V	Panasonic
30	1	R4	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
31	2	R5 R6	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
32	1	R7	RES, 300 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ301V	Panasonic
33	1	R8	RES, 10 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-10R	Yageo
34	1	R9	RES, 169 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1693V	Panasonic
35	1	R10	RES, 11.3 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1132X	Panasonic
36	1	R11	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
37	1	R12	RES, 470 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ471V	Panasonic
38	1	R13	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
39	1	R14	RES, SMD, 0.010 R, ±1%, 1/4 W, 100 PPM / C, 0805, Current Sense, Thick Film	PE0805FRF7W0R01L	Yageo
40	1	U1	ClampZero, MinSOP-16	CPZ1075M	Power Integrations

41	1	U2	InnoSwitch4-CZ, InSOP-24D	INN4075C-H180	Power Integrations
42	1	VOUT	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
43	1	VR1	TVS Diode, 275 V Clamp, 1.4 A Ipp, Tvs Diode, SMT, SMA SMAJ (DO-214AC)	SMAJ170A-13-F	Diodes, Inc.
44	1	VR2	Diode ZENER 9.1 V 500 mW SOD123	MMSZ5239B-7-F	Diodes, Inc.

Note: Component VR3, although present in the layout, should not be installed.

7 Transformer Design Spreadsheet

Note: The device, INN4075C, used for this design example has an ILIMIT_TYP of 1.7 A. INN4073C was used in the spreadsheet as substitute to achieve equivalent ILIMIT_TYP.

1	ACDC_InnoSwitch4-CZ_Flyback_021522; Rev.2.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 CZ Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	90		90	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ	60		60	Hz	AC Input voltage frequency
8	CAP_INPUT	120.0		120.0	uF	Input capacitor
9	VOUT	20.00		20.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	3.000		3.000	A	Output current
12	POUT			60.00	W	Output power
13	EFFICIENCY	0.94		0.94		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	INN4073		INN4073		Generic device code
22	DEVICE_CODE			INN4073C		Actual device code
23	POUT_MAX			60	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			1.02	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			1.581	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			1.700	A	Typical current limit of the primary switch
27	ILIMIT_MAX			1.819	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.65	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			563.4	V	Peak drain voltage on the primary switch during turn-off
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	100500		100500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	140.0		140.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			96.82	V	Valley of the minimum input AC voltage at full load
38	KP			0.61		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.593		Primary switch duty cycle
41	TIME_ON			10.49	us	Primary switch on-time
42	TIME_OFF			3.55	us	Primary switch off-time
43	LPRIMARY_MIN			579.5	uH	Minimum primary inductance
44	LPRIMARY_TYP			610.0	uH	Typical primary inductance
45	LPRIMARY_TOL	5.0		5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			640.5	uH	Maximum primary inductance

48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			1.758	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.615	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.648	A	Primary switch average current
52	IRIPPLE_PRIMARY			1.331	A	Primary switch ripple current
53	IRMS_PRIMARY			0.892	A	Primary switch RMS current
55	**SECONDARY CURRENT**					
56	IPEAK_SECONDARY			12.308	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			4.307	A	Secondary winding current pedestal
58	IRMS_SECONDARY			5.174	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	ATQ23.7/14.6		ATQ23.7/14.6		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE			ATQ23.7/14.6		Core code
66	AE			103.00	mm^2	Core cross sectional area
67	LE			38.20	mm	Core magnetic path length
68	AL			7200	nH/turns^2	Ungapped core effective inductance
69	VE			3935.0	mm^3	Core volume
70	BOBBIN			TBI-238-10051.17XX		Bobbin
71	AW			22.11	mm^2	Window area of the bobbin
72	BW			6.60	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			35		Primary turns
77	BPEAK			3308	Gauss	Peak flux density
78	BMAX			3092	Gauss	Maximum flux density
79	BAC			1150	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			498	nH/turns^2	Typical gapped core effective inductance
81	LG			0.242	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			2		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY	5		5		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			2		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	**CLAMPZERO**					
96	LLEAK			6.10	uH	Primary winding leakage inductance
97	CCLAMP			100.0	nF	Primary clamp capacitor
98	RD_CLAMPZERO	30		30	kΩ	HSD resistor
99	TLLDL/THLDL			120.0	ns	HSD resistor programmed delay
100	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			65.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
101	TIME_VDS_VALLEY			50.9	ns	Time taken by the VDS ring to reach its first valley
102	IPEAK_CLAMPZERO			1.712	A	Active clamp peak current
104	**LINE UNDERVOLTAGE**					
105	BROWN-IN REQURED			72.0	V	Required AC RMS/DC line voltage brown-in threshold
106	RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold

107	BROWN-IN ACTUAL			73.0	V	Actual AC RMS/DC brown-in threshold
108	BROWN-OUT ACTUAL			66.0	V	Actual AC RMS/DC brown-out threshold
110	**LINE OVERVOLTAGE**					
111	OVERVOLTAGE_LINE			304.2	V	Actual AC RMS/DC line over-voltage threshold
113	**PRIMARY BIAS DIODE**					
114	VBIAS_PRIMARY	8.0	Info	8.0	V	The rectified primary bias voltage too low to supply the BPP pin: Increase the rectified primary bias voltage to a value greater than 10V
115	VF_BIAS_PRIMARY	0.00		0.00	V	Bias winding diode forward drop
116	VREVERSE_BIASDIODE_PRIMARY			29.42	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
117	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
118	CBPP			0.47	uF	BPP pin capacitor
122	**SECONDARY COMPONENTS**					
123	RFB_UPPER	169.00		169.00	kΩ	Upper feedback resistor (connected to the first output voltage)
124	RFB_LOWER			11.50	kΩ	Lower feedback resistor
125	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127	**SECONDARY BIAS DIODE**					
128	USE_SECONDARY_BIAS	YES		YES		Use secondary bias winding for the design
129	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
130	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
131	VREVERSE_BIASDIODE_SECONDARY			26.42	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
132	CBIAS_SECONDARY			10	uF	Bias winding rectification capacitor
133	CBPS			2.20	uF	BPP pin capacitor
136	**MULTIPLE OUTPUT PARAMETERS**					
137	**OUTPUT 1**					
138	VOUT1			20.00	V	Output 1 voltage
139	IOUT1			3.00	A	Output 1 current
140	POUT1			60.00	W	Output 1 power
141	IRMS_SECONDARY1			5.174	A	Root mean squared value of the secondary current for output 1
142	IRIPPLE_CAP_OUTPUT1			4.216	A	Current ripple on the secondary waveform for output 1
143	NSECONDARY1			5		Number of turns for output 1
144	VREVERSE_RECTIFIER1			73.54	V	SR FET reverse voltage (not accounting parasitic voltage ring) for output 1
145	SR FET1	AONS66920		AONS66920		Secondary rectifier (Logic MOSFET) for output 1
146	VF_SR FET1			0.032	V	SR FET on-time drain voltage for output 1
147	VBREAKDOWN_SR FET1			100	V	SR FET breakdown voltage for output 1
148	RDSON_SR FET1			10.7	mΩ	SR FET on-time drain resistance at 25degC and VGS=4.4V for output 1
176	PO_TOTAL			60	W	Total power of all outputs
177	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Note: The warnings on the spreadsheet have been verified to not be an issue for this design.

8 Transformer Specification

8.1 *Electrical Diagram*

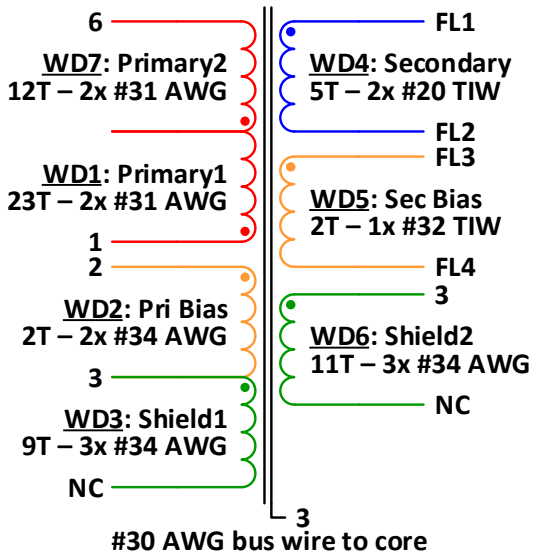


Figure 6 – Transformer Electrical Diagram.

8.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pins 1 and 6, with all other windings open.	610 µH ±5%
Resonant Frequency	Between pins 1 and 6, with all other windings open.	1,200 kHz (Min.)
Primary Leakage Inductance	Between pins 1 and 6, with pins FL1-FL2 shorted.	5 µH (Max.)

8.3 *Material List*

Item	Description
[1]	Core: ATQ23.7/14.
[2]	Bobbin: ATQ23.7/14 - Vertical - 6pins (3/3); PI#: 25-01171-00.
[3]	Magnet Wire: #31 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #20 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #32 AWG, Triple Insulated Wire.
[7]	Bus Wire: #30 AWG, Alpha Wire, Tinned Copper, 30 mm Length.
[8]	Tape: 3M 13450-F, Polyester Film, 1mil Thickness, 6.7 mm Width.
[9]	Tape: 3M 13450-F, Polyester Film, 1mil Thickness, 14 mm Width.
[10]	Tape: 3M 13450-F, Polyester Film, 1mil Thickness, 30 mm x 54 mm.
[11]	Varnish: Dolph BC-359.

8.4 *Transformer Build Diagram*

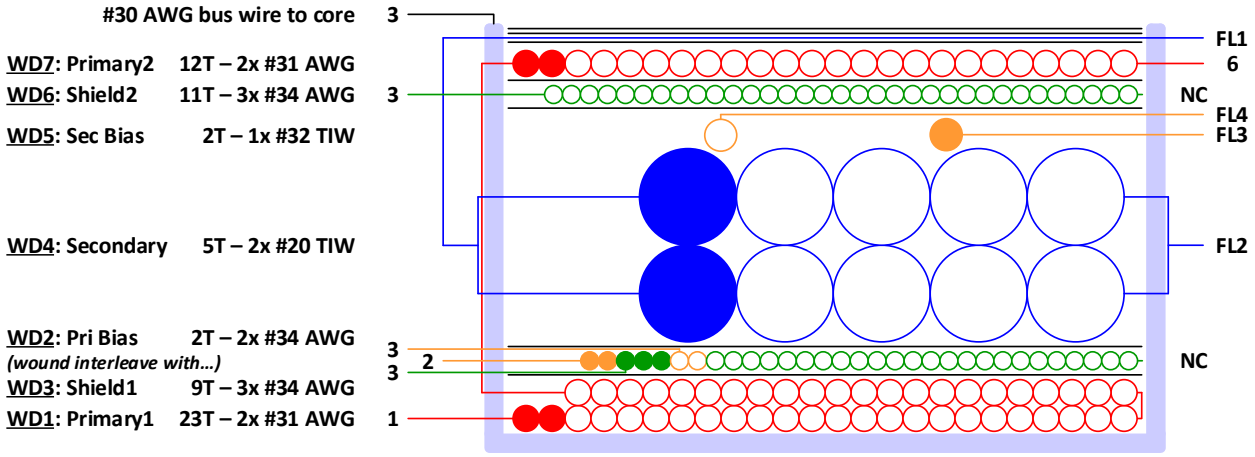


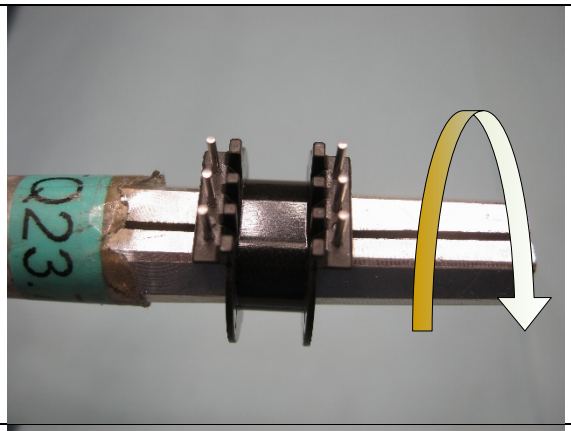
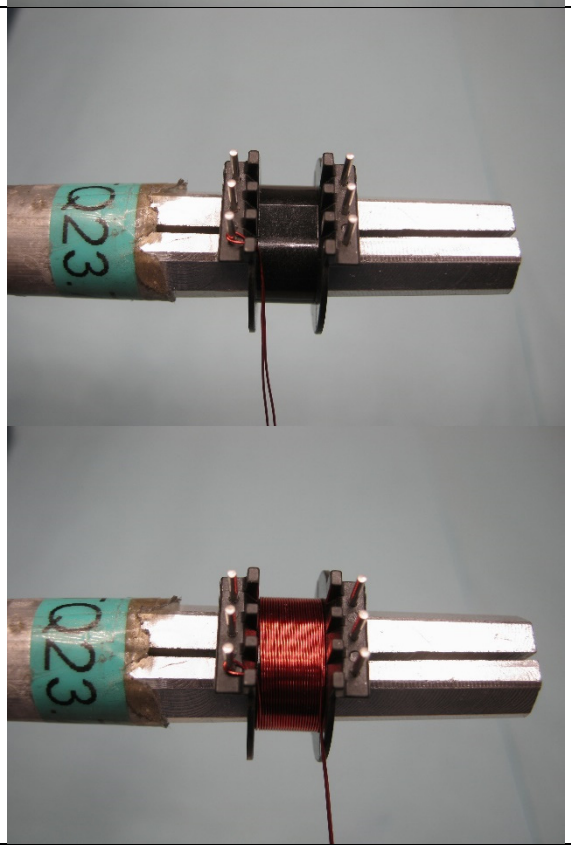
Figure 7 – Transformer Build Diagram.

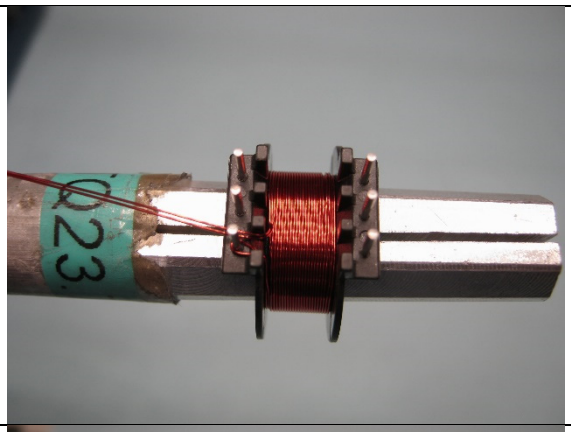
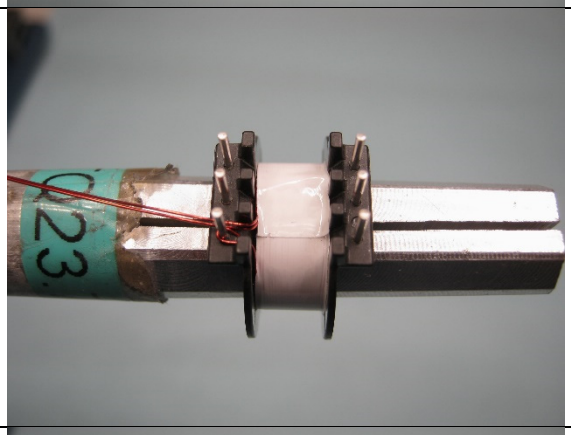
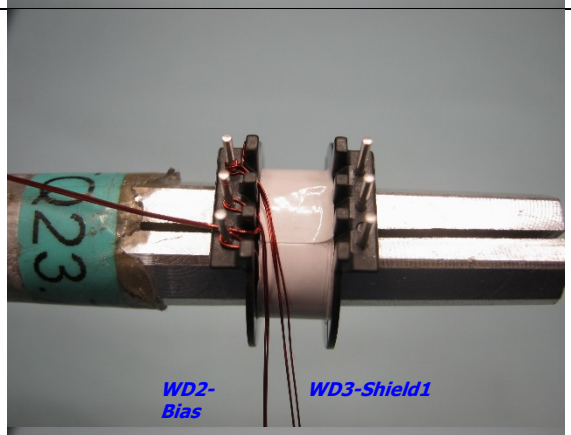
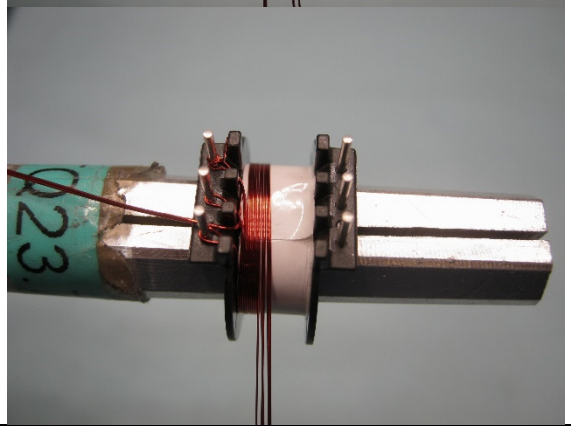
8.5 *Transformer Winding Instructions*

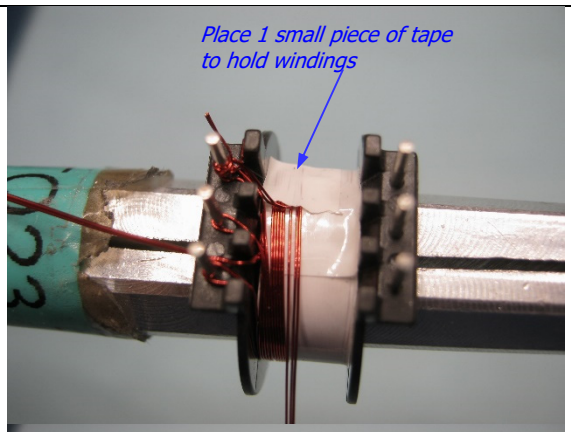
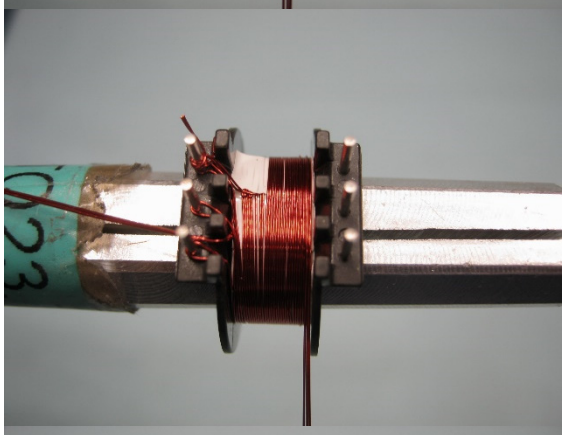
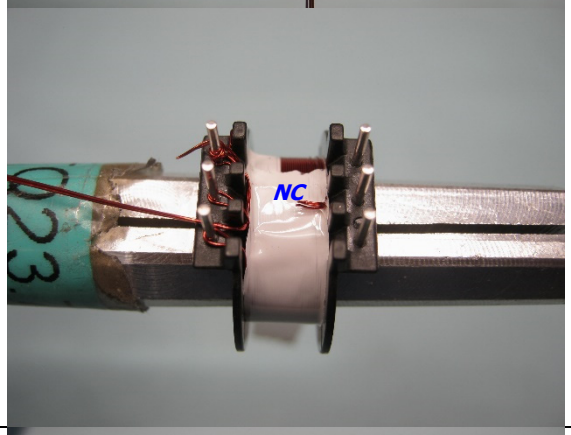
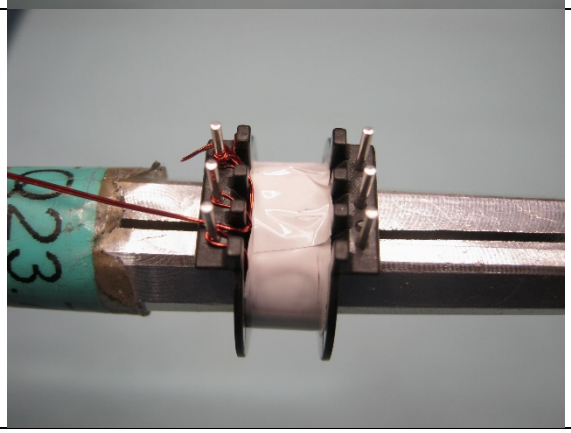
Winding Preparation	Place the bobbin Item [2] on the mandrel with pin side of the bobbin on the left side. Winding direction is clockwise direction.
WD1 Primary1	Start at pin 1, wind 12 turns using 2 wires of Item [3] in 1 layer, from left to right, then continue winding another 11 turns from right to left. At the last turn, bring the wires out of the bobbin and leaving enough wire length for WD7: Primary2.
Insulation	1 layer of tape Item [8].
WD2: PriBias & WD3: Shield1	Using 2 wires of Item [4], starting at pin 2 for WD2: PriBias and 3 wires of Item [4] starting at pin 3 for WD3: Shield1, wind all 5 wires in parallel. After 2 turns, bring 2 wires of WD2: PriBias to the pin side and terminate at pin 3. Using the remaining 3 wires, continue winding 9 turns, cut short the wires, and leave as NO CONNECT (NC) for WD3: Shield1.
Insulation	1 layer of tape Item [8].
WD4: Secondary	Start at the slot on the left side of the bobbin, use 1 wire of Item [5], leaving ~40mm floating, marked as FL1, and wind 5 turns in 1 layer. At the last turn, bring the wire at the slot on the right side while leaving ~30 mm floating, marked as FL2, for 1st half of WD4: Secondary. Repeat as instructed above for another winding for 2nd half of WD4: Secondary which is parallel with 1st half of WD4: Secondary.
WD5: SecBias	Using 1 wire of Item [6], start from the right side of the bobbin, leaving ~30 mm and mark as FL3. Wind 2 turns and bring the wire to the right side of the bobbin, leaving ~30 mm and mark as FL4 for WD5: SecBias.
Insulation	1 layer of tape Item [8].
WD6: Shield2	Start at pin 2, wind 11 tri-filar turns of wire Item [4]. At the last turn, cut short the wires, and leave as NO CONNECT (NC) for WD6: Shield2.
Insulation	1 layer of tape Item [8].
WD7: Primary2	Using the floating wires from WD1, wind 12 turns from left to right. At the last turn, terminate at pin 6 for WD7: Primary2.
Insulation	1 layer of tape Item [8] and bring the secondary wires FL1 to the right in between layers of tape.
Finish	Gap cores to get 610 µH, solder bus wire Item [7] to pin 3 and wrap around the core halves to the left side (*see illustration below*) and secure with tape Item [9].

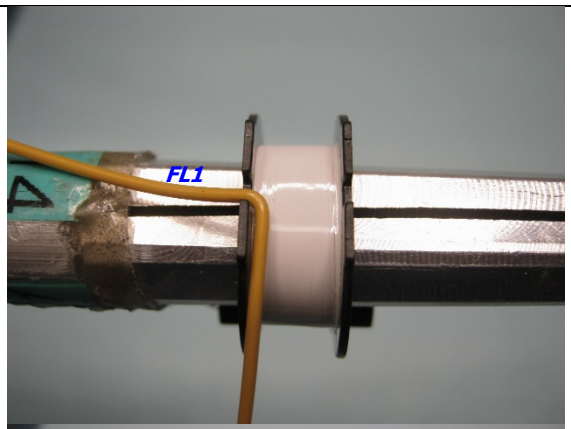
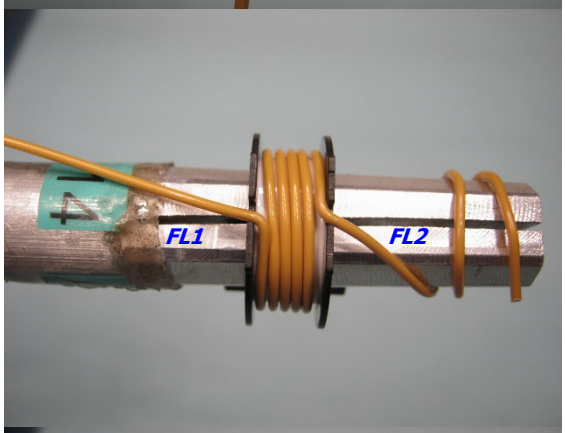
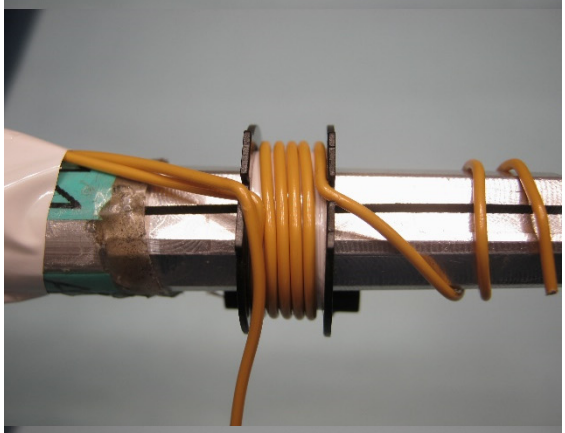
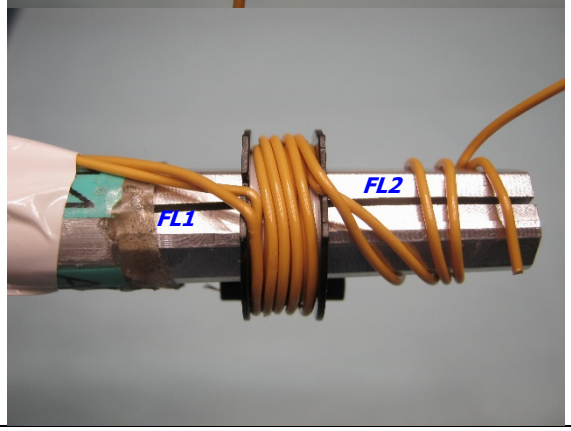
	Varnish with Item [11]. Place 2 layers of tape Item [10] at the bottom of transformer, completely covering the core (*see illustration below*), and wrap to cover the secondary side of transformer. Wrap 1 layer of tape Item [8] around the body of transformer *(see illustration below).*

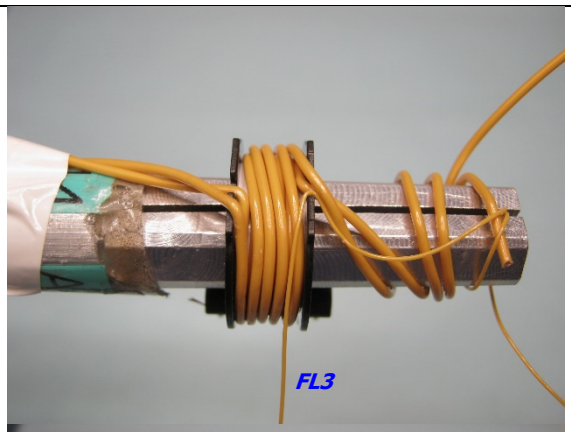
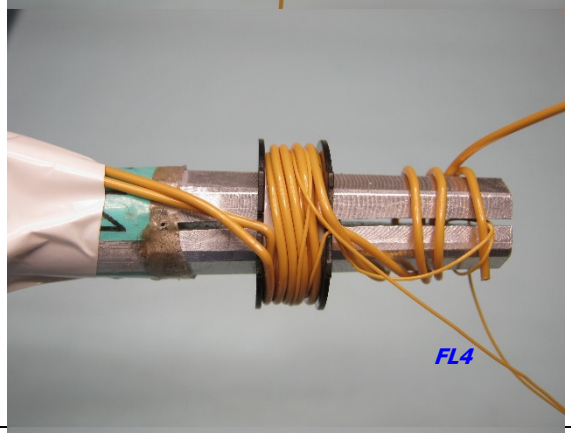
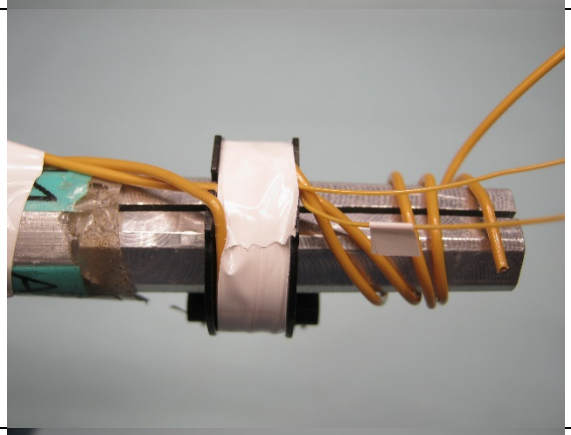
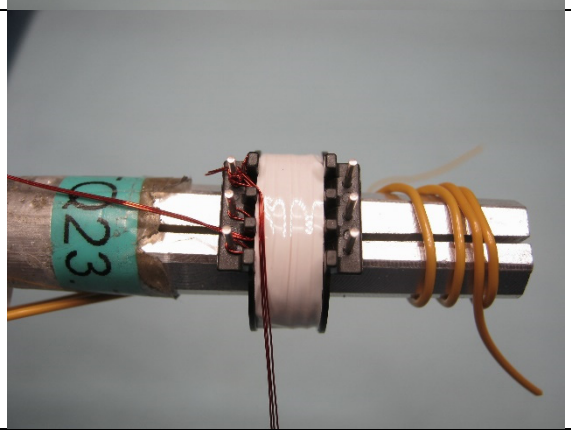
8.6 ***Transformer Winding Illustrations***

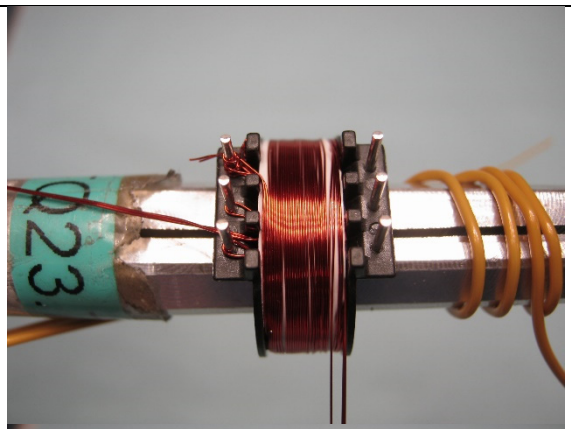
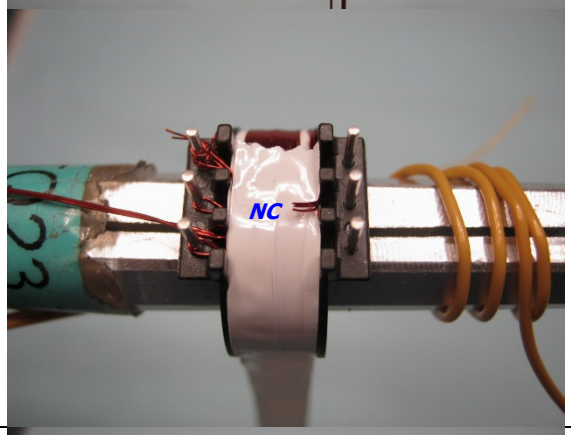
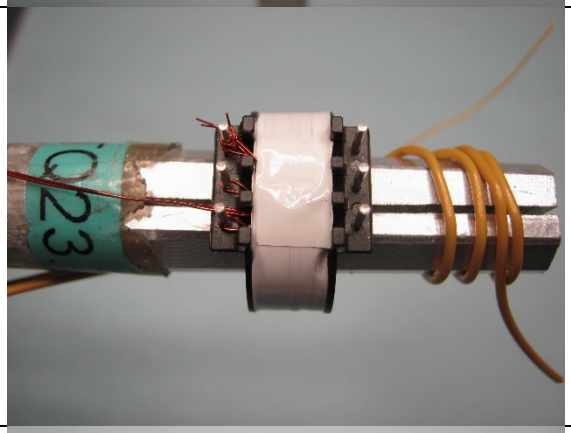
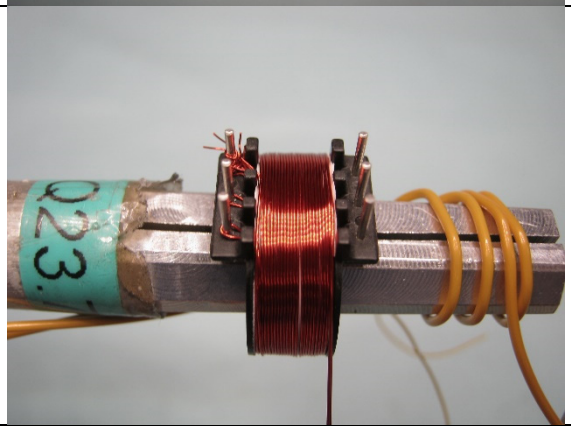
Winding Preparation		Place the bobbin Item [2] on the mandrel with pin side of the bobbin on the left side. Winding direction is clockwise direction.
WD1: Primary1		Start at pin 1, wind 12 turns using 2 wires of Item [3] in 1 layer, from left to right, then continue winding another 11 turns from right to left. At the last turn, bring the wires out of the bobbin and leaving enough wire length for WD7: Primary2.

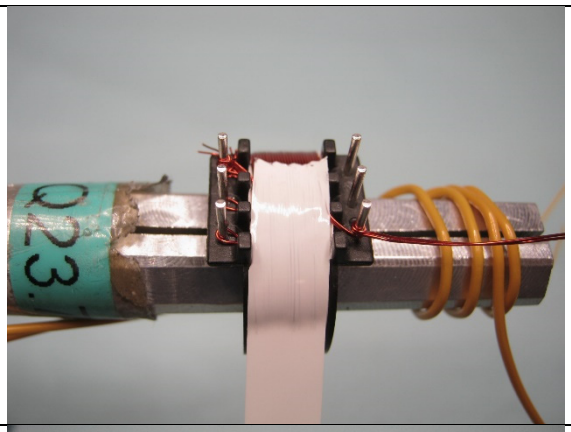
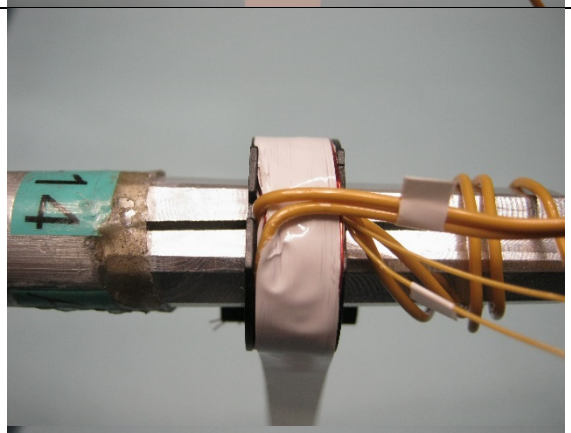
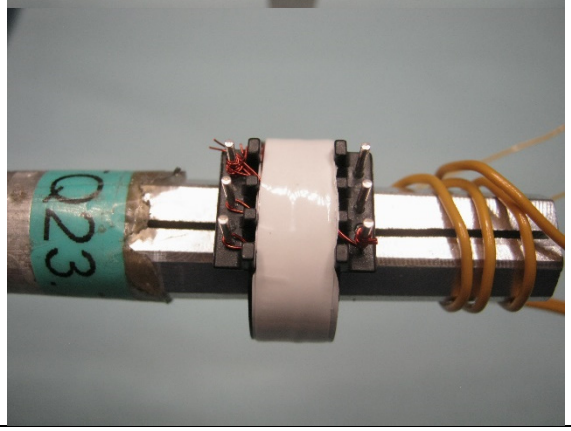
		
Insulation		1 layer of tape Item [8].
WD2: PriBias & WD3: Shield1	 	Using 2 wires of Item [4], starting at pin 2 for WD2: PriBias and 3 wires of Item [4] starting at pin 3 for WD3: Shield1, wind all 5 wires in parallel. After 2 turns, bring 2 wires of WD2: PriBias to the pin side and terminate at pin 3. Using the remaining 3 wires, continue winding 9 turns, cut short the wires, and leave as NO CONNECT (NC) for WD3: Shield1.

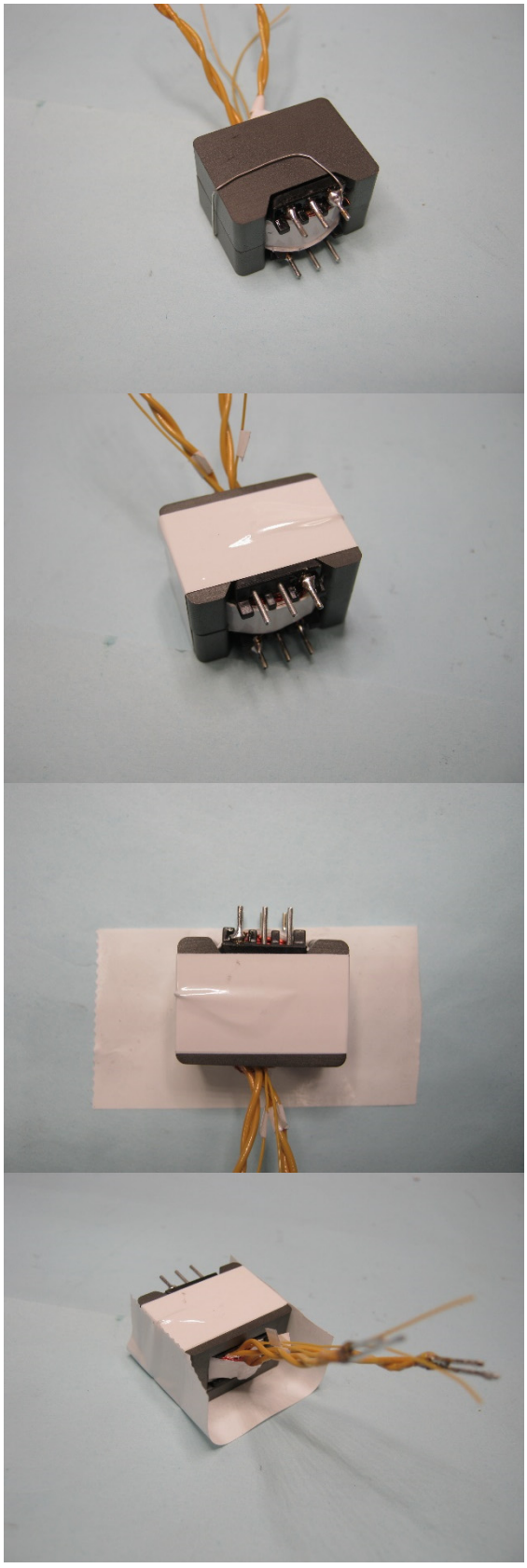
	  	
Insulation		1 layer of tape Item [8].

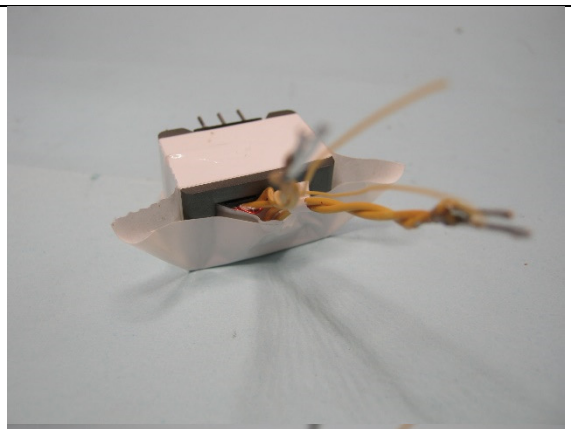
WD4: Secondary	   	Start at the slot on the left side of the bobbin, use 1 wire of Item [5], leaving ~40 mm floating, marked as FL1, and wind 5 turns in 1 layer. At the last turn, bring the wire at the slot on the right side while leaving ~30 mm floating, marked as FL2, for 1st half of WD4: Secondary. Repeat as instructed above for another winding for 2nd half of WD4: Secondary which is parallel with 1st half of WD4: Secondary.

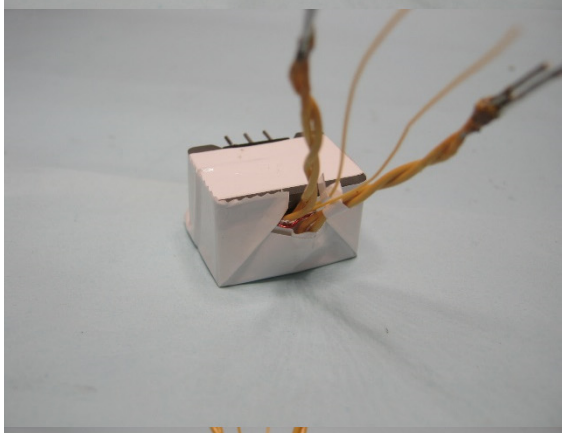
WD5: SecBias	 	Using 1 wire of Item [6], start from the right side of the bobbin, leaving ~30 mm and mark as FL3. Wind 2 turns and bring the wire to the right side of the bobbin, leaving ~30 mm and mark as FL4 for WD5: SecBias.
Insulation		1 layer of tape Item [8].
WD6: Shield2		Start at pin 2, wind 11 tri-filar turns of wire Item [4]. At the last turn, cut short the wires, and leave as NO CONNECT (NC) for WD6: Shield2.

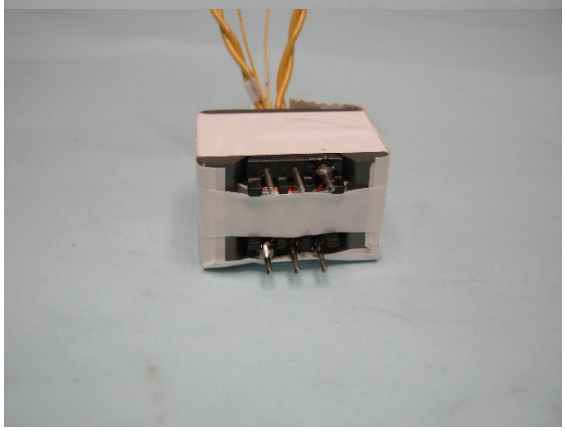
	 	
Insulation		1 layer of tape Item [8].
WD7: Primary2		Using the floating wires from WD1, wind 12 turns from left to right. At the last turn, terminate at pin 6 for WD7: Primary2.

		
Insulation	 	1 layer of tape Item [8] and bring the secondary wires FL1 to the right in between layers of tape.

Finish		Gap cores to get 610 µH, solder bus wire Item [7] to pin 3 and wrap around the core halves to the left side (*see illustration below*) and secure with tape Item [9]. Varnish with Item [11]. Place 2 layers of tape Item [10] at the bottom of transformer, completely covering the core (*see illustration below*), and wrap to cover the secondary side of transformer. Wrap 1 layer of tape Item [8] around the body of transformer *(see illustration below).*







9 Common-Mode Choke Specification

9.1 *Electrical Diagram*

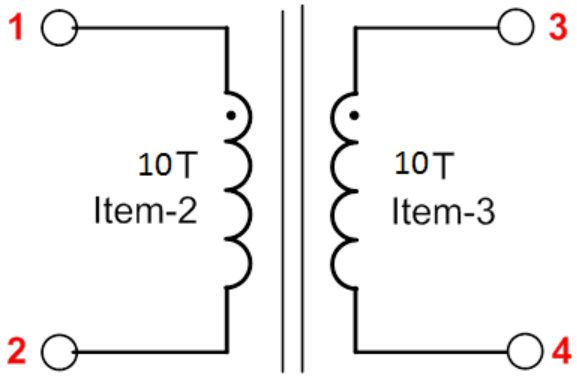


Figure 8 – CMC Build Diagram.

9.2 *Electrical Specifications*

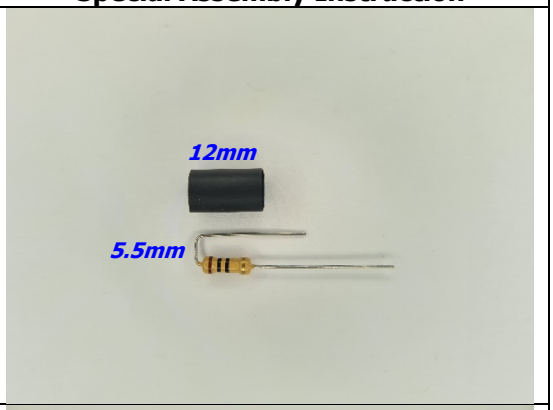
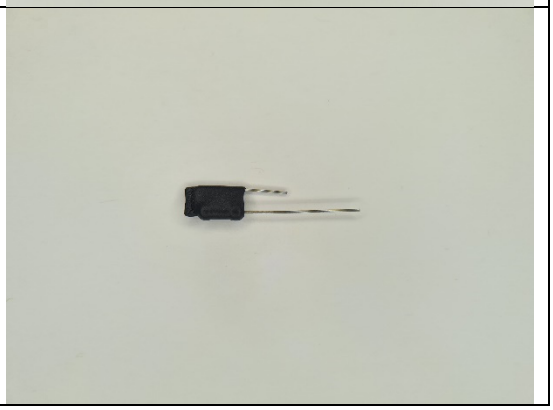
Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	415 µH ±30%

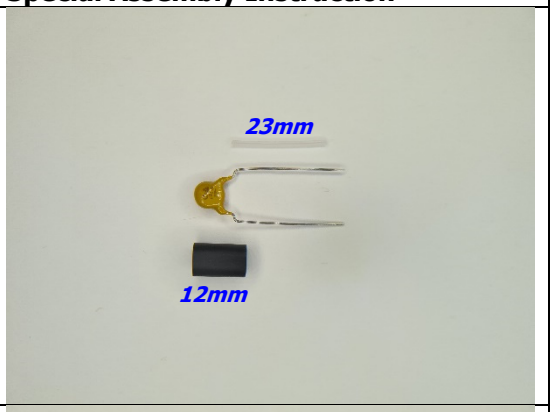
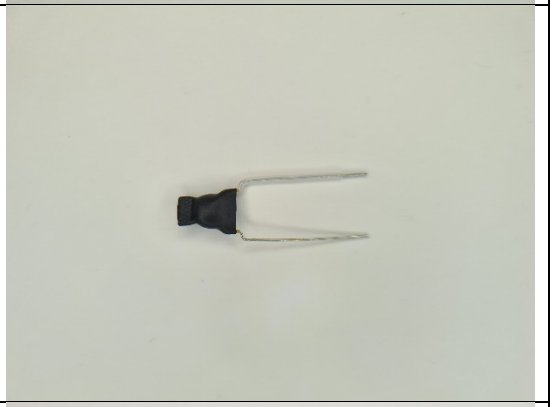
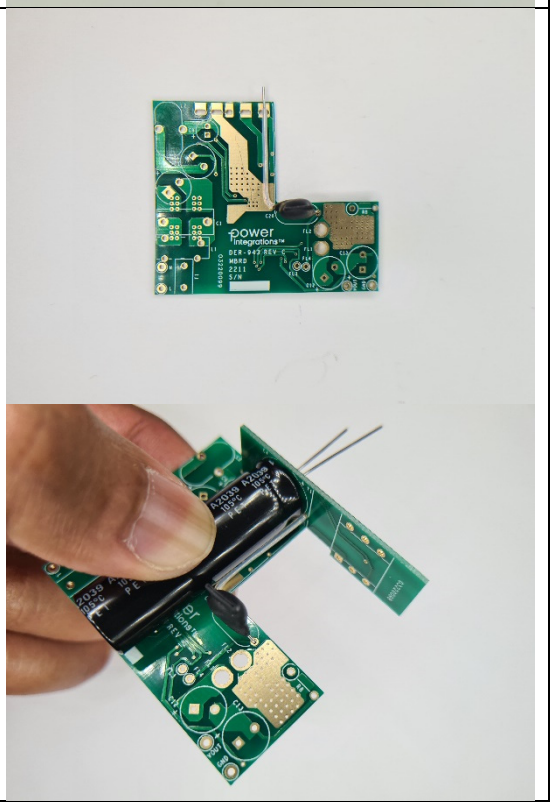
9.3 *Material List*

Item	Description
[1]	Toroidal Core: T9*5*3C-JL12, PI#: 32-00330-00.
[2]	Triple Insulated Wire: #26 AWG, Triple Coated.
[3]	Magnet Wire: #26 AWG, Double Coated.

9.4 *Assembled Picture*

10 PCB Assembly Instructions

R8	Special Assembly Instruction
Prepare 12 mm length of 1/4-inch heat shrink. Bend one leg of resistor R8 to a right angle and repeat the bend approximately 5.5 mm (see illustration on the right).	
Insert the formed resistor in the prepared heat shrink, completely covering the body of the resistor with the excess heat shrink being on the bent-leg side. Using a heat gun, heat up the heat shrink over the resistor and pinch the excess to completely seal it.	

C20	Special Assembly Instruction
Prepare 12 mm length of 1/4”-inch heat shrink. Prepare 23 mm length of AWG #22 PTFE tubing. Bend two legs of capacitor C20 to widen the lead spacing (see illustration on the right).	
Insert the formed capacitor in the prepared heat shrink, completely covering the body of the capacitor with the excess heat shrink being on the body side. Insert one leg of the capacitor C20 in the prepared PTFE tubing, completely covering the leg up to point where the body meets the leg. Using a heat gun, heat up the heat shrink over the capacitor and pinch the excess to completely seal it.	
Bend the leg covered with PTFE tubing to a right-angle pointing outward (see illustration on the right). Solder the leg covered with PTFE tubing on the primary side of the PCB, labeled as C20-1 on the daughter board (see illustration on the right). Solder the bare leg on the secondary side of the PCB on the main board (see illustration on the right). Note: C20 should be assembled after transformer T1 insertion on the daughter board.	

11 Performance Data

All the performance data were taken on the board unless otherwise specifically mentioned.

11.1 *No-Load Input Power*

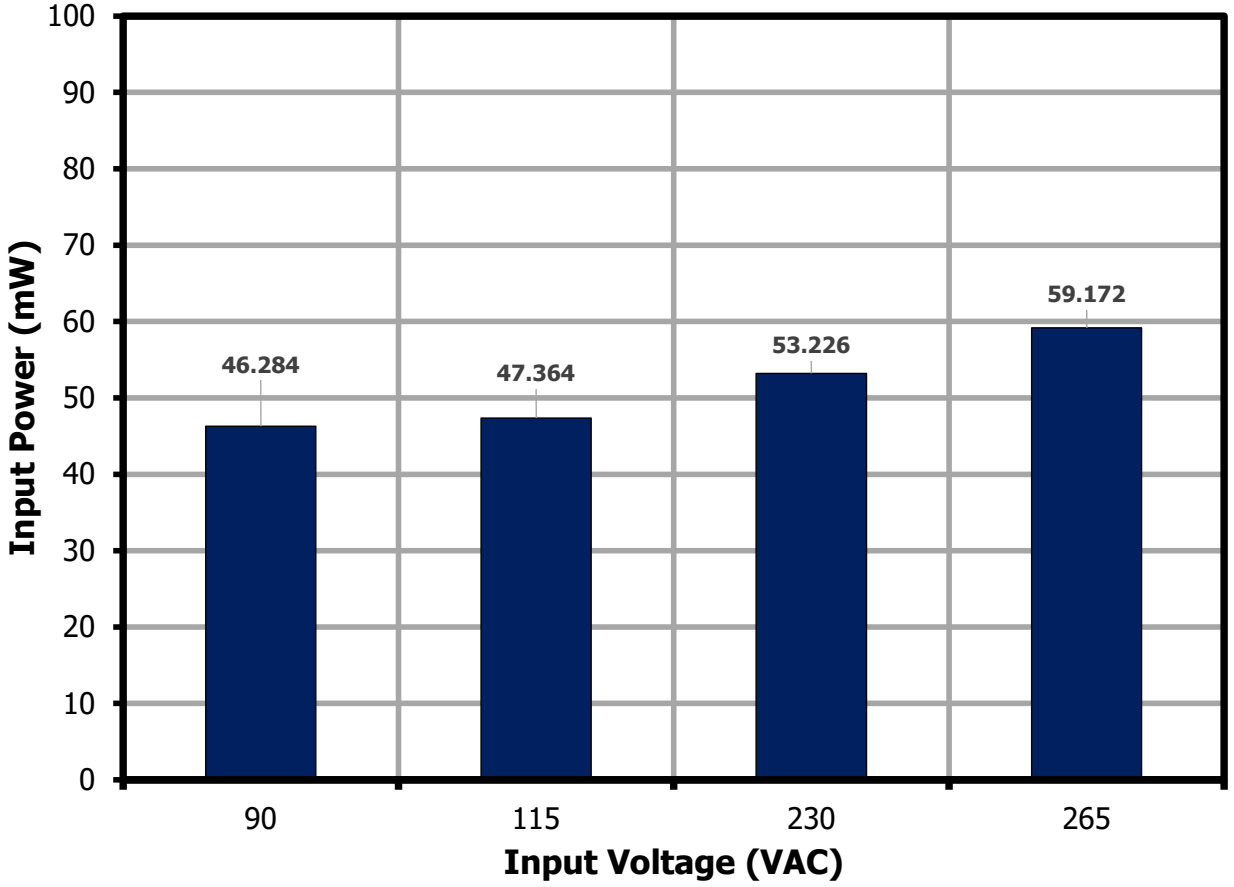


Figure 9 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

11.2 *Average Efficiency*

11.2.1 Average Efficiency Summary

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
20	60	94.21	94.88	90.37	91.11

11.2.2 Average and 10% Efficiency at 90 VAC Input

% Load	Power (W)	Efficiency (%)	Average Efficiency (%)
100	59.80	93.92	93.87
75	45.07	94.26	
50	30.20	94.02	
25	15.15	93.26	
10	6.05	90.49	

11.2.3 Average and 10% Efficiency at 115 VAC Input

% Load	Power (W)	Efficiency (%)	Average Efficiency (%)
100	59.98	94.60	94.21
75	45.14	94.52	
50	30.24	94.31	
25	15.16	93.40	
10	6.06	90.37	

11.2.4 Average and 10% Efficiency at 230 VAC Input

% Load	Power (W)	Efficiency (%)	Average Efficiency (%)
100	60.36	95.32	94.88
75	45.36	95.23	
50	30.31	94.89	
25	15.16	94.07	
10	6.06	91.11	

11.2.5 Average and 10% Efficiency at 265 VAC Input

% Load	Power (W)	Efficiency (%)	Average Efficiency (%)
100	60.42	95.18	94.65
75	45.41	95.03	
50	30.32	94.69	
25	15.16	93.71	
10	6.06	90.38	

11.3 *Full-Load Efficiency vs. Line*

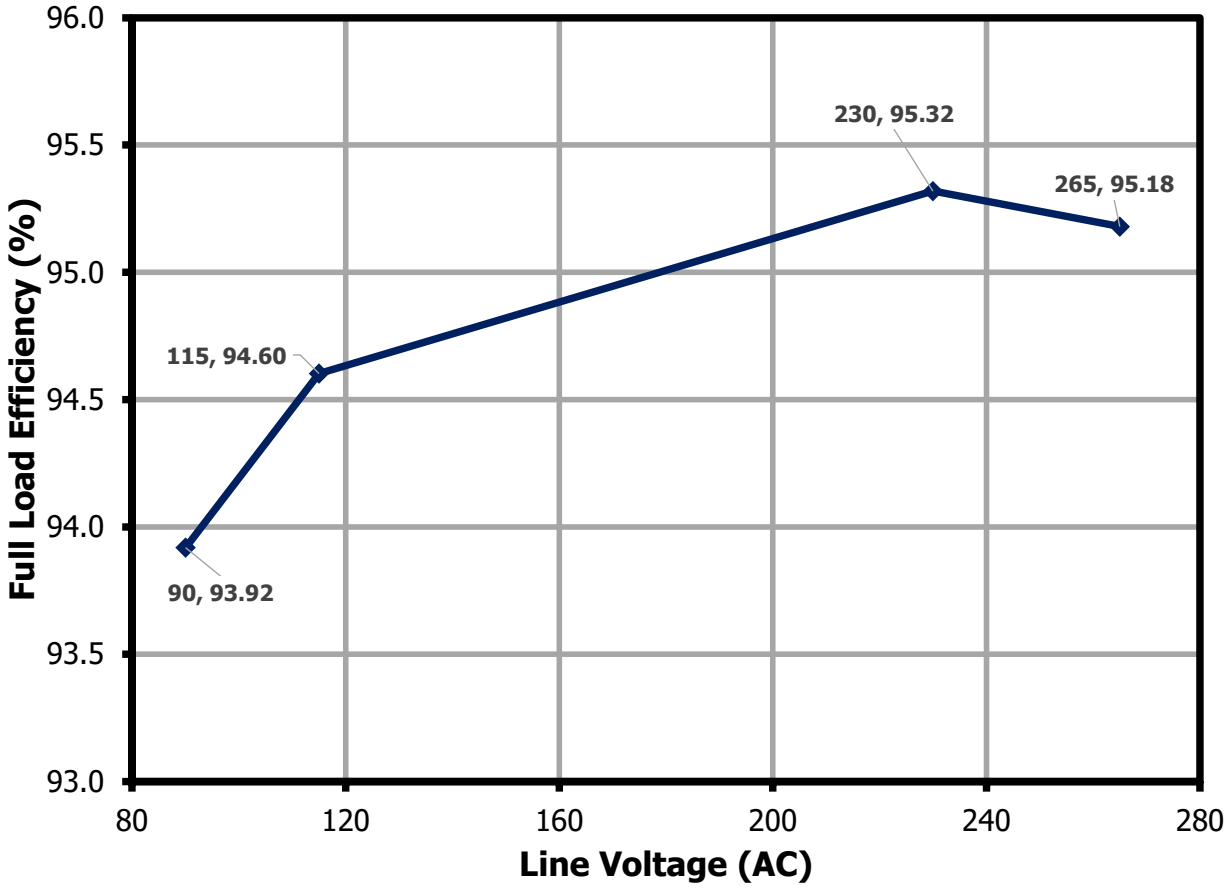


Figure 10 – Full-Load Efficiency vs. Input Line Voltage, Room Temperature.

11.4 *Efficiency vs. Load*

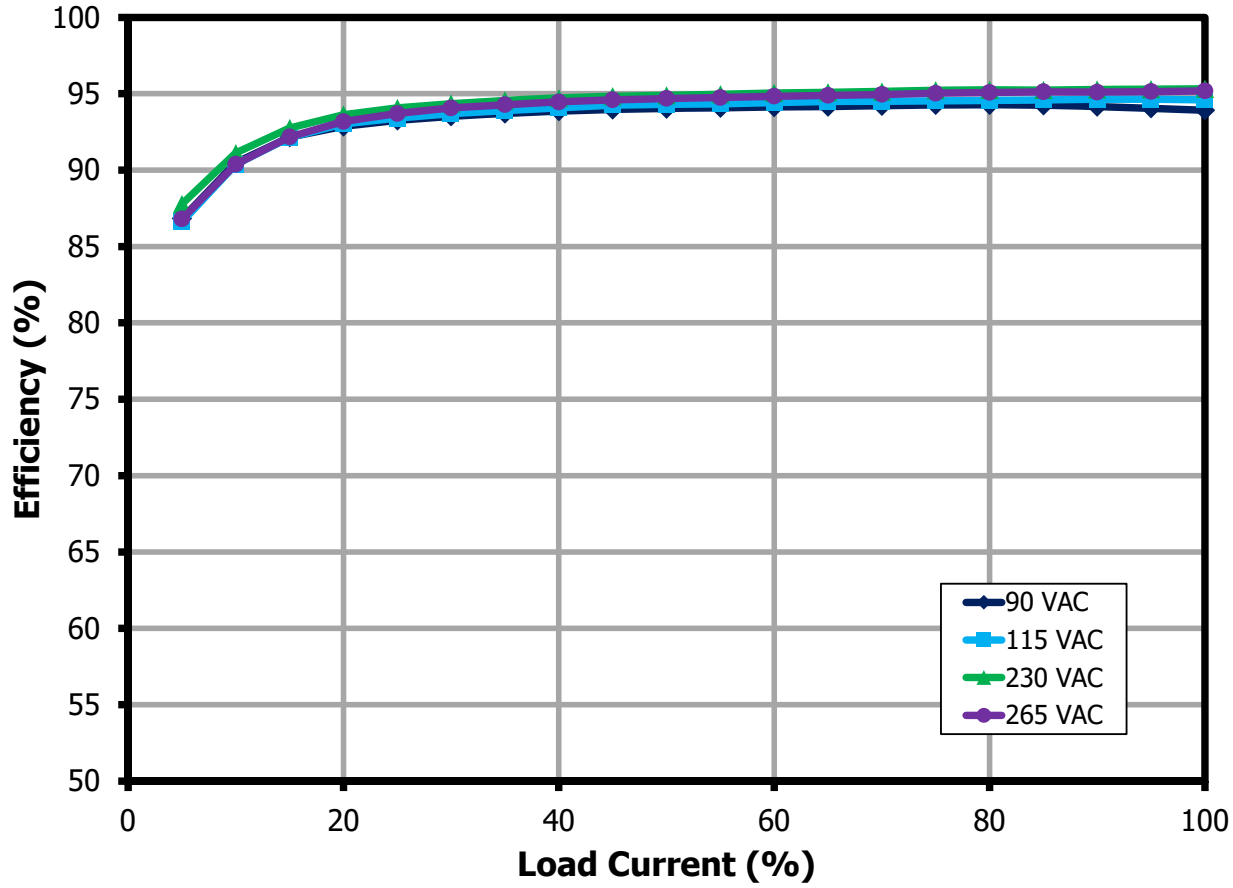


Figure 11 – Efficiency vs. Output Load, Room Temperature.

11.5 *Load Regulation*

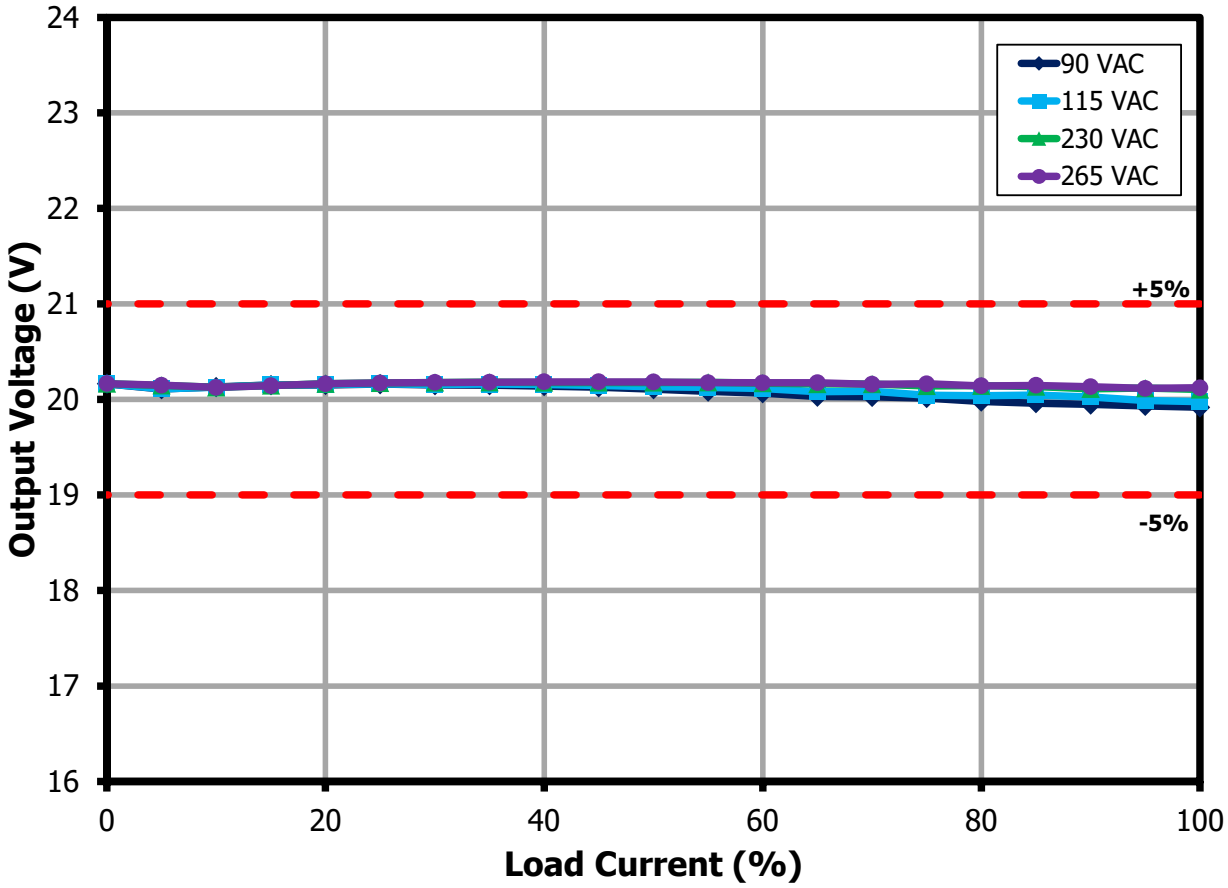


Figure 12 – Output Voltage vs. Output Load, Room Temperature.

11.6 *Line Regulation*

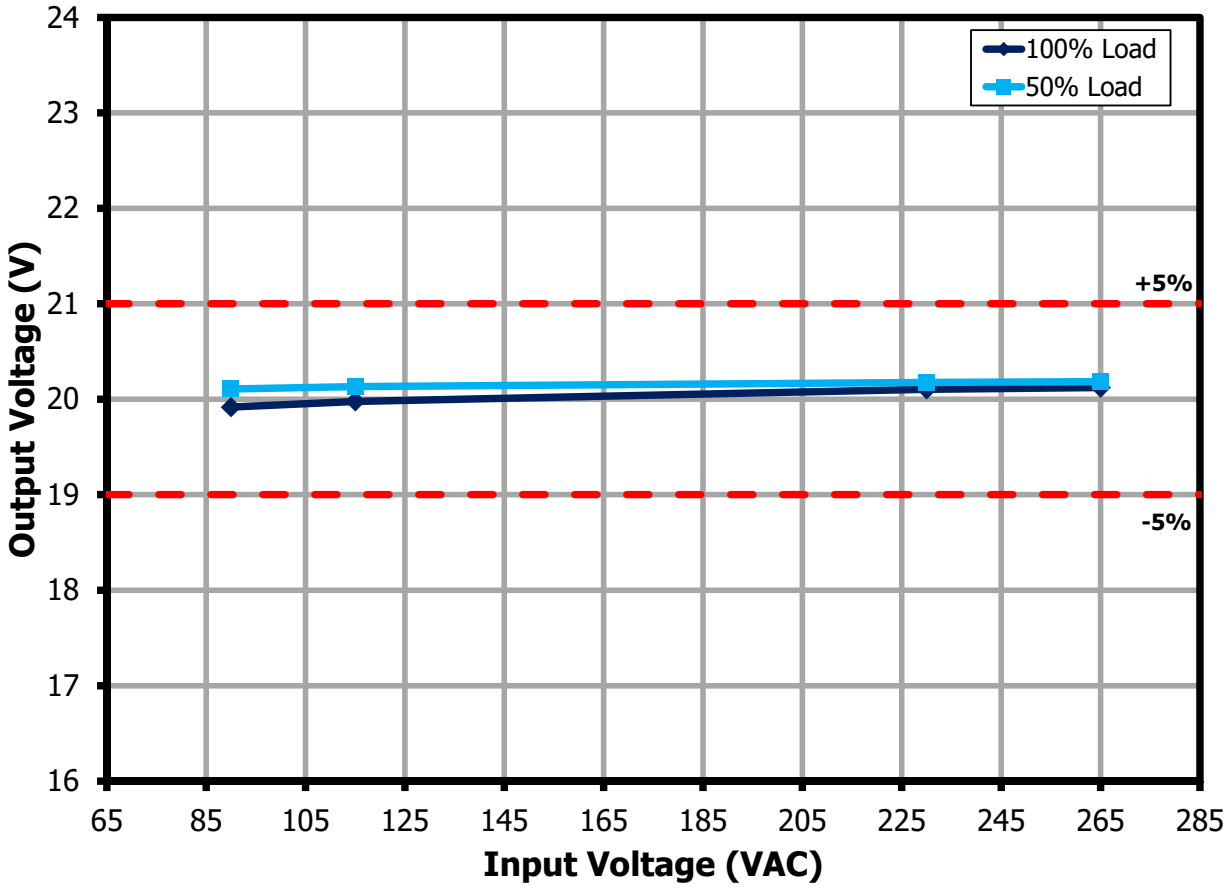


Figure 13 – Output Voltage vs. Input Line Voltage, Room Temperature.

12 Thermal Performance

12.1 *90 VAC, 20 V / 3 A*

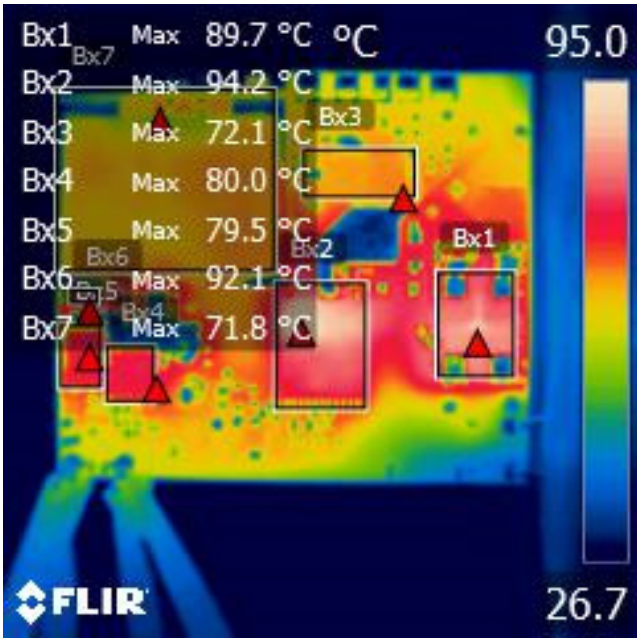


Figure 14 – Bottom Thermal Image, T_{AMB} = 26.7 ºC.
Bx1: Bridge Rectifier, BR1 = 89.7 ºC.
Bx2: InnoSwitch4-CZ, U2 = 94.2 ºC.
Bx3: ClampZero, U1 = 72.1 ºC.
Bx4: SR FET, Q1 = 80.0 ºC.
Bx5: Schottky Diode, D2 = 79.5 ºC.
Bx6: Snubber Diode, D1 = 92.1 ºC.
Bx7: Transformer Core, T1 = 71.8 ºC.

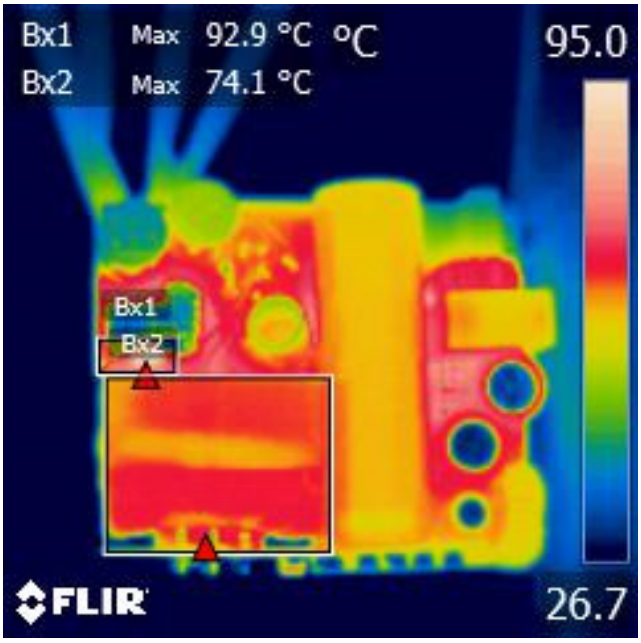


Figure 15 – Top Thermal Image, T_{AMB} = 26.7 ºC.
Bx1: Snubber Resistor, R3 = 92.9 ºC.
Bx2: Transformer Core, T1 = 74.1 ºC.

12.2 ***265 VAC, 20 V / 3 A***

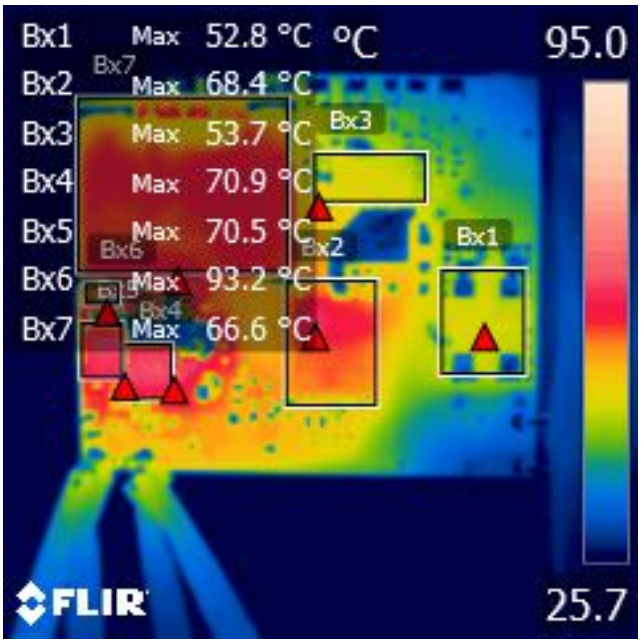


Figure 16 – Bottom Thermal Image, T_{AMB} = 25.7 ºC.
Bx1: Bridge Rectifier, BR1 = 52.8 ºC.
Bx2: InnoSwitch4-CZ, U2 = 68.4 ºC.
Bx3: ClampZero, U1 = 53.7 ºC.
Bx4: SR FET, Q1 = 70.9 ºC.
Bx5: Schottky Diode, D2 = 70.5 ºC.
Bx6: Snubber Diode, D1 = 93.2 ºC.
Bx7: Transformer Core, T1 = 66.6 ºC.

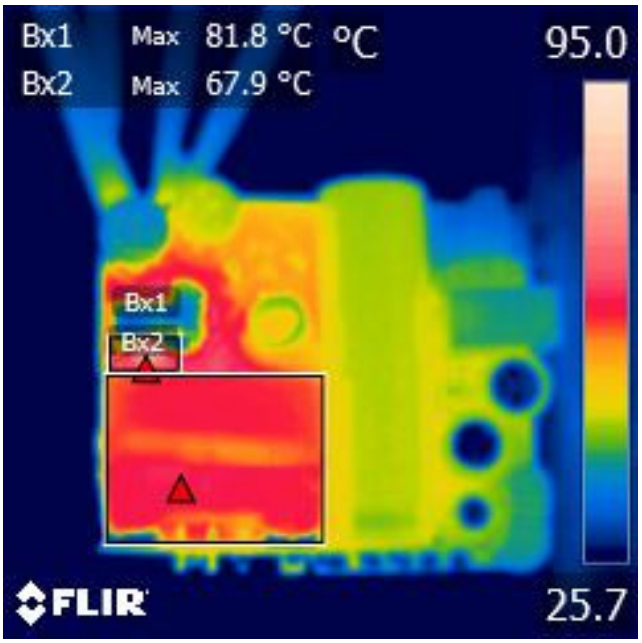


Figure 17 – Top Thermal Image, T_{AMB} = 25.7 ºC.
Bx1: Snubber Resistor, R3 = 81.8 ºC.
Bx2: Transformer Core, T1 = 67.9 ºC.

13 Waveforms

13.1 *Start-Up Waveforms*

13.1.1 Output Voltage and Current Waveforms

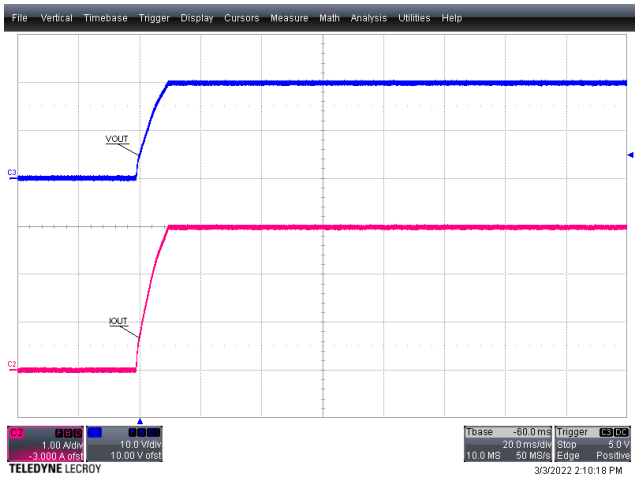


Figure 18 – Output Voltage and Current.
90 VAC, 100% CR Load.
CH2: I_{OUT}, 1 A / div.
CH3: V_{OUT}, 10 V / div.
Time: 20 ms / div.

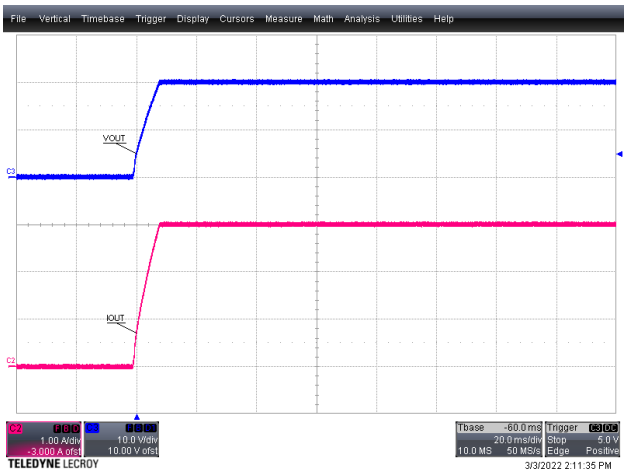


Figure 19 – Output Voltage and Current.
265 VAC, 100% CR Load.
CH2: I_{OUT}, 1 A / div.
CH3: V_{OUT}, 10 V / div.
Time: 20 ms / div.

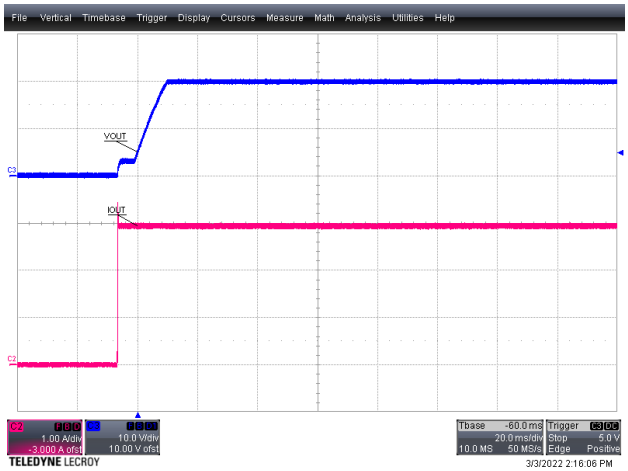


Figure 20 – Output Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{OUT}, 1 A / div.
CH3: V_{OUT}, 10 V / div.
Time: 20 ms / div.

Figure 21 – Output Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{OUT}, 1 A / div.
CH3: V_{OUT}, 10 V / div.
Time: 20 ms / div.

13.1.2 Primary Drain Voltage and Current Waveforms

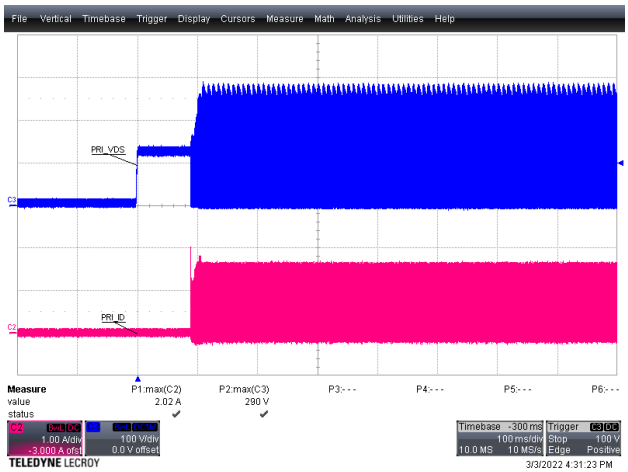


Figure 22 – Primary Drain Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{D_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 100 V / div.
V_{DS_PRI} = 290 V_{MAX}.
Time: 100 ms / div.

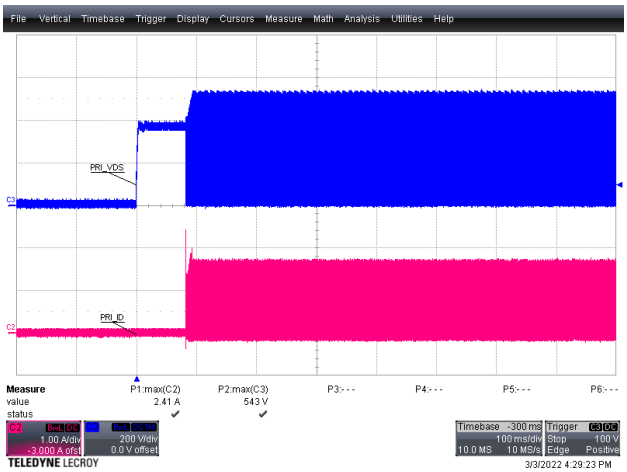


Figure 23 – Primary Drain Voltage and Current.
265 VAC, 100% CC Load.
CH2: I_{D_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 200 V / div.
V_{DS_PRI} = 543 V_{MAX}.
Time: 100 ms / div.

13.1.3 ClampZero Drain Voltage and Current Waveforms

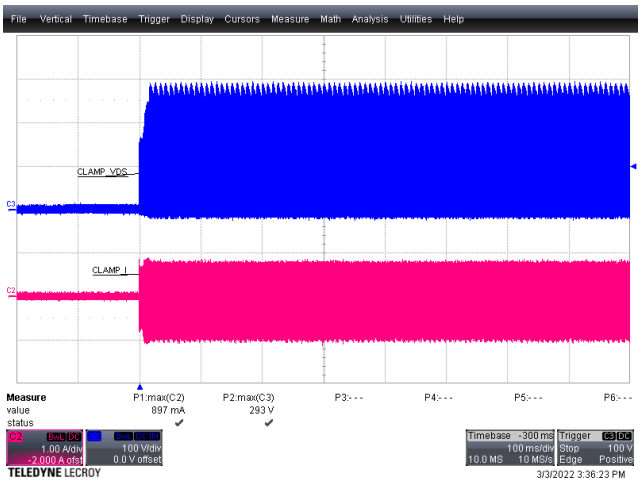


Figure 24 – ClampZero Drain Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{D_CLAMP}, 1 A / div.
CH3: V_{DS_CLAMP}, 100 V / div.
V_{DS_PRI} = 293 V_{MAX}.
Time: 100 ms / div.

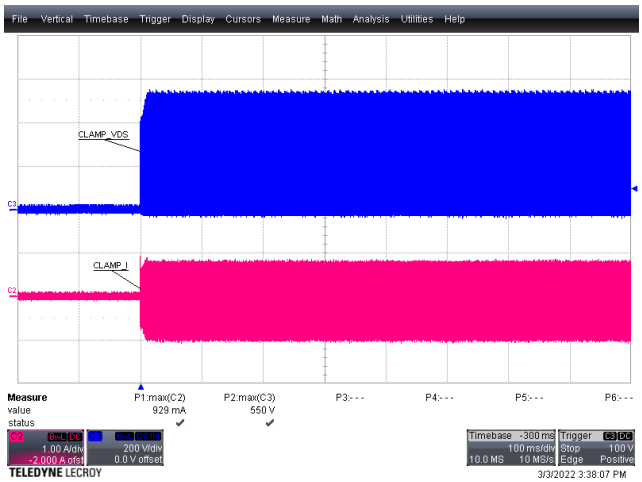


Figure 25 – ClampZero Drain Voltage and Current.
265 VAC, 100% CC Load.
CH2: I_{D_CLAMP}, 1 A / div.
CH3: V_{DS_CLAMP}, 100 V / div.
V_{DS_PRI} = 550 V_{MAX}.
Time: 100 ms / div.

13.1.4 SR FET Drain Voltage and Load Current Waveforms

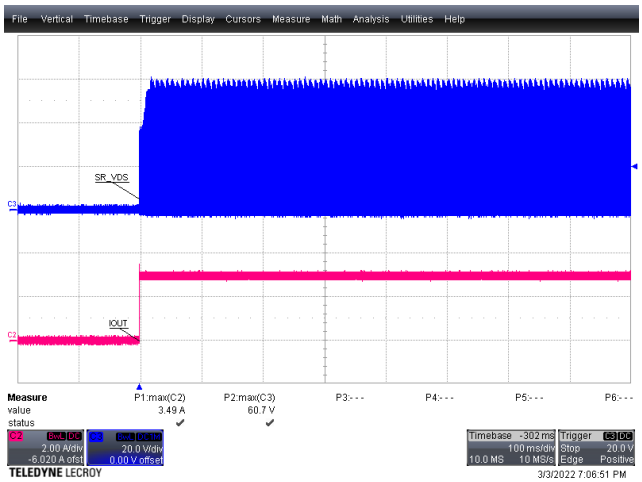


Figure 26 – SR FET Drain Voltage and Load Current.
90 VAC, 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: $V_{DS\_SR\ FET}$, 20 V / div.
V_{DS_PRI} = 60.7 V_{MAX}.
Time: 100 ms / div.

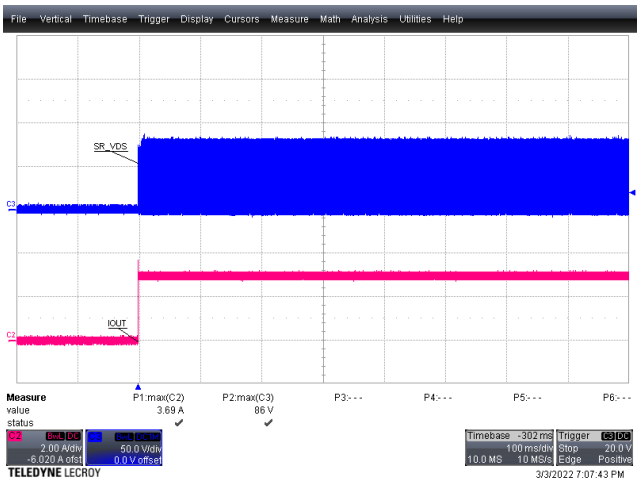


Figure 27 – SR FET Drain Voltage and Load Current.
265 VAC, 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: $V_{DS\_SR\ FET}$, 50 V / div.
V_{DS_PRI} = 86.0 V_{MAX}.
Time: 100 ms / div.

13.2 *Load Transient Waveforms*

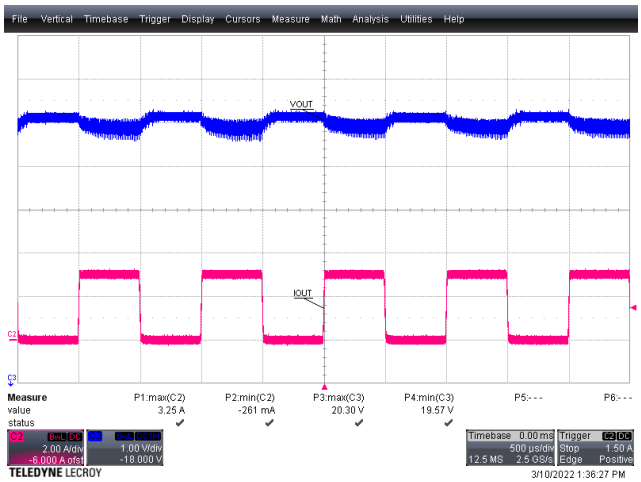


Figure 28 – Output Voltage and Current.
90 VAC, 0% to 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 1 V / div.
V_{OUT} = 20.30 V_{MAX}, 19.57 V_{MIN}.
Time: 500 µs / div.

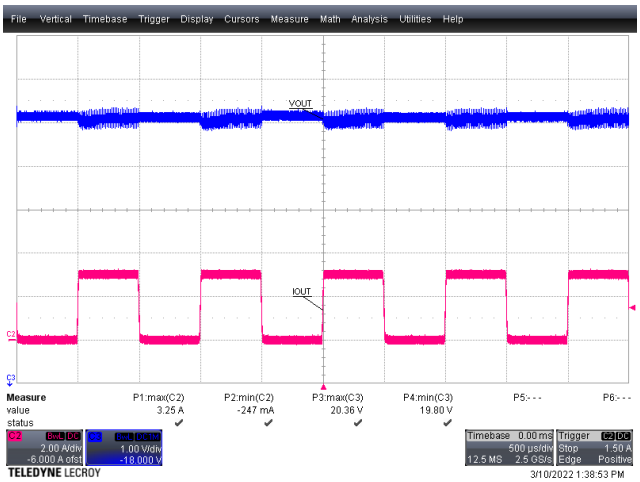


Figure 29 – Output Voltage and Current.
265 VAC, 0% to 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 1 V / div.
V_{OUT} = 20.36 V_{MAX}, 19.80 V_{MIN}.
Time: 500 µs / div.

13.3 ***Steady State Waveforms***

13.3.1 Primary Drain Voltage and Current Waveforms

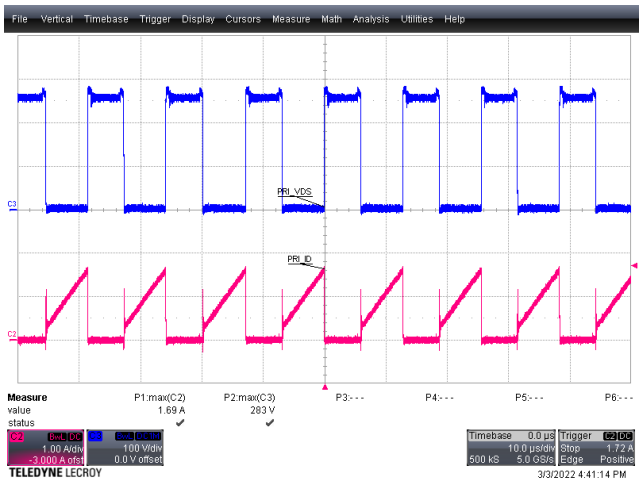


Figure 30 – Primary Drain Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{D_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 100 V / div.
V_{DS_PRI} = 283 V_{MAX}.
Time: 10 µs / div.

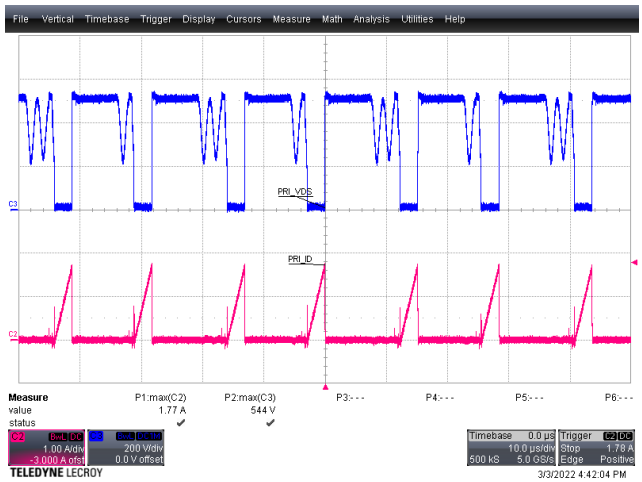


Figure 31 – Primary Drain Voltage and Current.
265 VAC, 100% CC Load.
CH2: I_{D_PRI}, 1 A / div.
CH3: V_{DS_PRI}, 200 V / div.
V_{DS_PRI} = 544 V_{MAX}.
Time: 10 µs / div.

13.3.2 ClampZero Drain Voltage and Current Waveforms

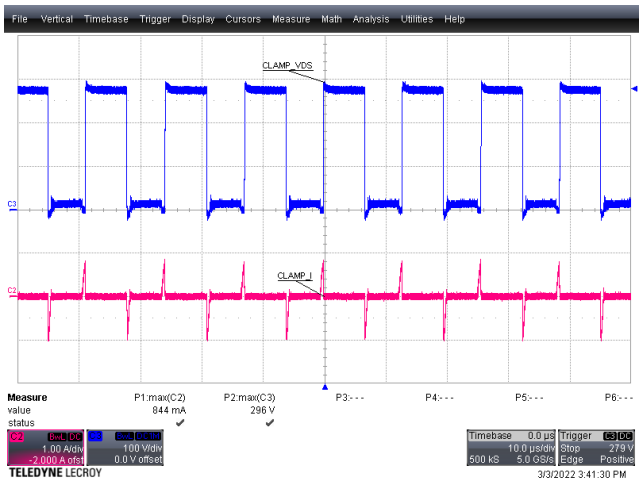


Figure 32 – ClampZero Drain Voltage and Current.
90 VAC, 100% CC Load.
CH2: I_{D_CLAMP}, 1 A / div.
CH3: V_{DS_CLAMP}, 100 V / div.
V_{DS_PRI} = 296 V_{MAX}.
Time: 10 µs / div.

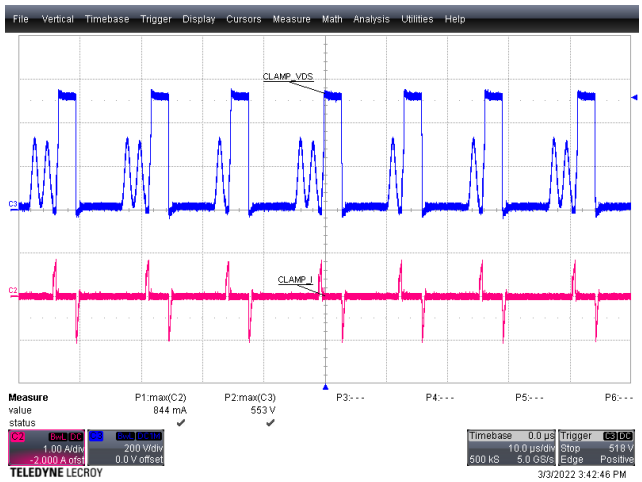


Figure 33 – ClampZero Drain Voltage and Current.
265 VAC, 100% CC Load.
CH2: I_{D_CLAMP}, 1 A / div.
CH3: V_{DS_CLAMP}, 200 V / div.
V_{DS_PRI} = 553 V_{MAX}.
Time: 10 µs / div.

13.3.3 SR FET Drain Voltage and Load Current Waveforms

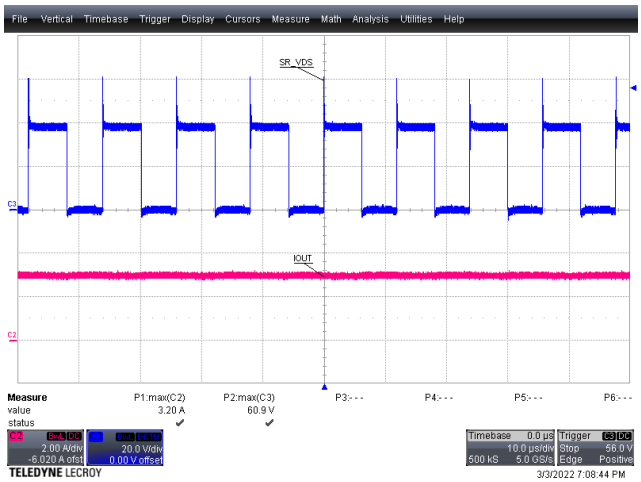


Figure 34 – SR FET Drain Voltage and Load Current.
90 VAC, 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: $V_{DS\_SR\ FET}$, 20 V / div.
V_{DS_PRI} = 60.9 V_{MAX}.
Time: 10 µs / div.

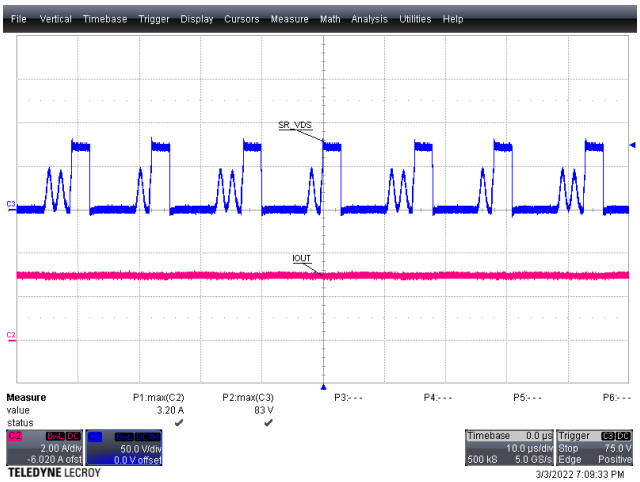


Figure 35 – SR FET Drain Voltage and Load Current.
265 VAC, 100% CC Load.
CH2: I_{OUT}, 2 A / div.
CH3: $V_{DS\_SR\ FET}$, 50 V / div.
V_{DS_PRI} = 83 V_{MAX}.
Time: 10 µs / div.

14 Output Ripple Measurements

To measure the ripple, Probe Master 4903-2 voltage probe was used (x1 30 MHz) coupled to a probe adapter (Probe Master 4987BA BNC adapter) affixed with 2 capacitors (0.1 μF / 50 V ceramic and 47 μF / 50 V E-cap) connected across the tip and ground as shown below. Oscilloscope was set to AC coupling with frequency bandwidth of 20 MHz. Voltage ripple was measured at the board terminals at room ambient temperature (25 ºC).

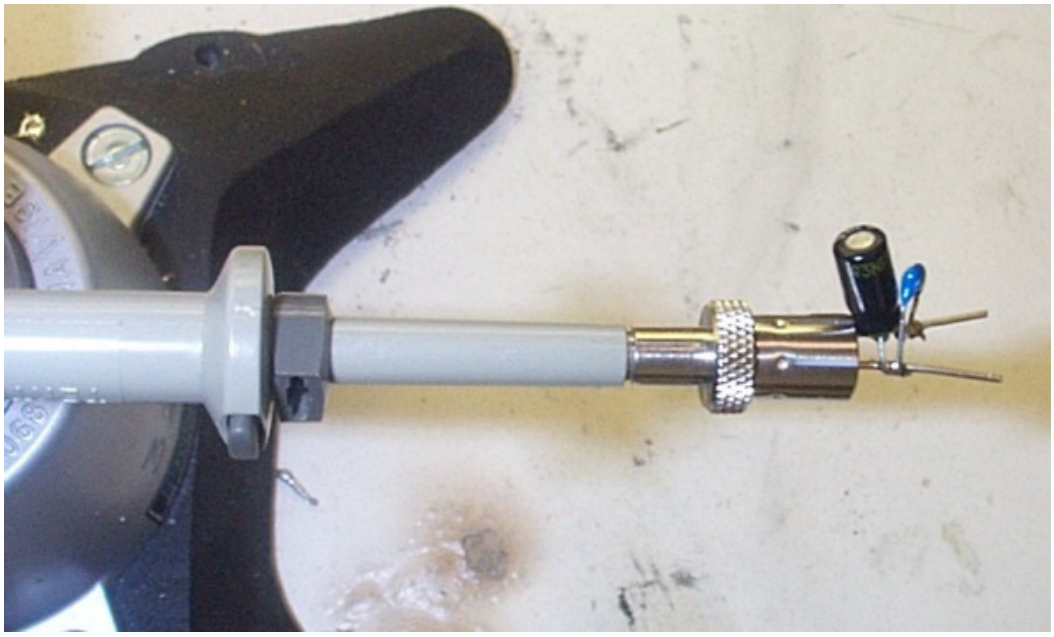


Figure 36 – Oscilloscope probe with Probe Master 4987A BNC adapter.
(Modified with two parallel decoupling capacitors for ripple measurement)

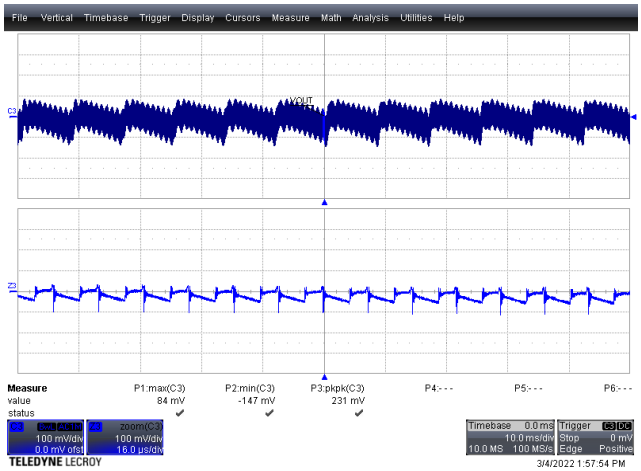


Figure 37 – Output Voltage Ripple.
90 VAC, 100% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 231 V_{PK-PK}.
Time: 10 ms / div.

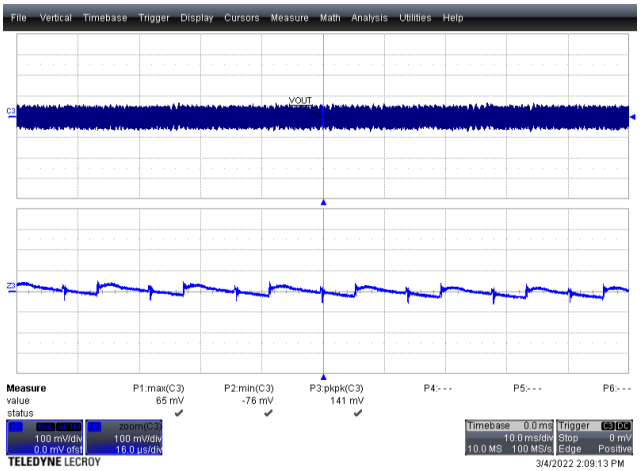


Figure 38 – Output Voltage Ripple.
90 VAC, 50% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 141 V_{PK-PK}.
Time: 10 ms / div.

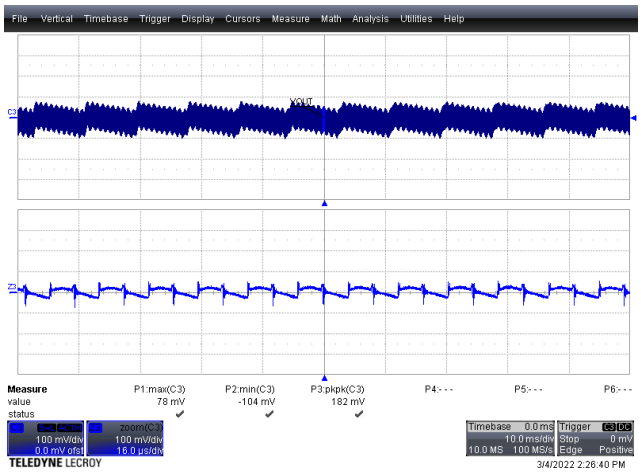


Figure 39 – Output Voltage Ripple.
115 VAC, 100% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 182 V_{PK-PK}.
Time: 10 ms / div.

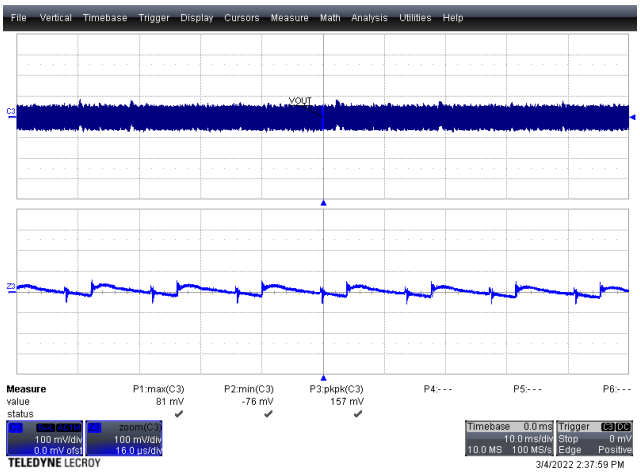


Figure 40 – Output Voltage Ripple.
115 VAC, 50% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 157 V_{PK-PK}.
Time: 10 ms / div.

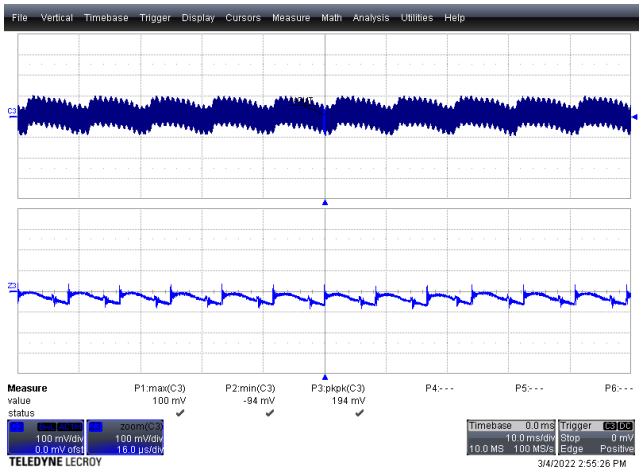


Figure 41 – Output Voltage Ripple.
230 VAC, 100% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 194 V_{PK-PK}.
Time: 10 ms / div.

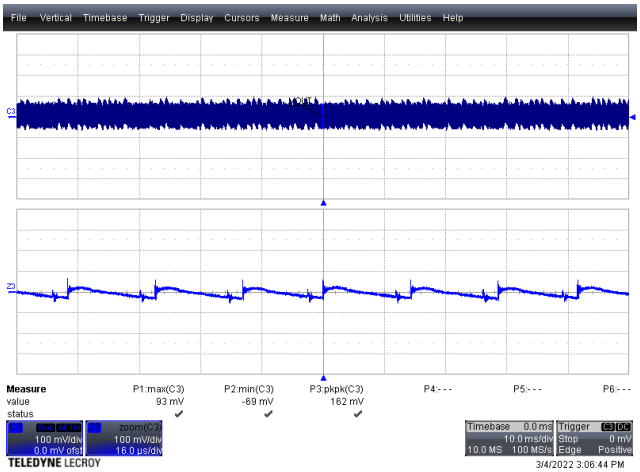


Figure 42 – Output Voltage Ripple.
230 VAC, 50% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 162 V_{PK-PK}.
Time: 10 ms / div.

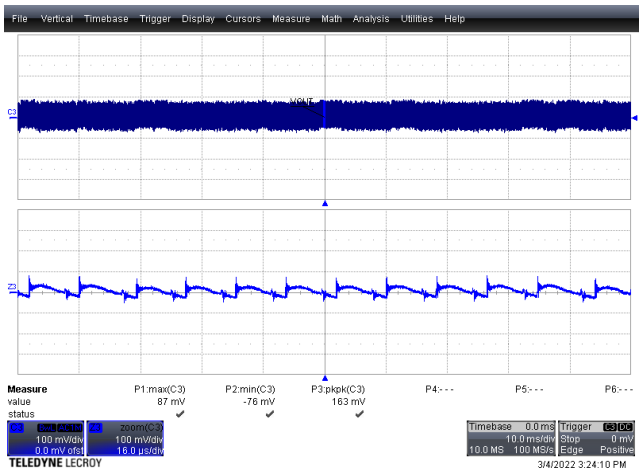


Figure 43 – Output Voltage Ripple.
265 VAC, 100% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 163 V_{PK-PK}.
Time: 10 ms / div.

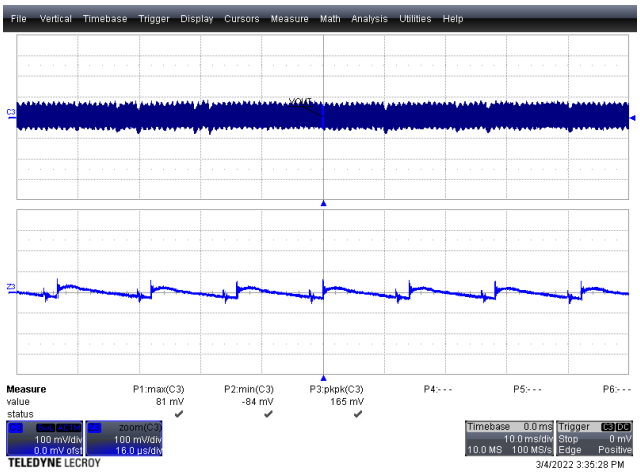


Figure 44 – Output Voltage Ripple.
265 VAC, 50% CC Load.
CH3: V_{OUT_RIPPLE}, 100 mV / div.
V_{OUT_RIPPLE} = 165 V_{PK-PK}.
Time: 10 ms / div.

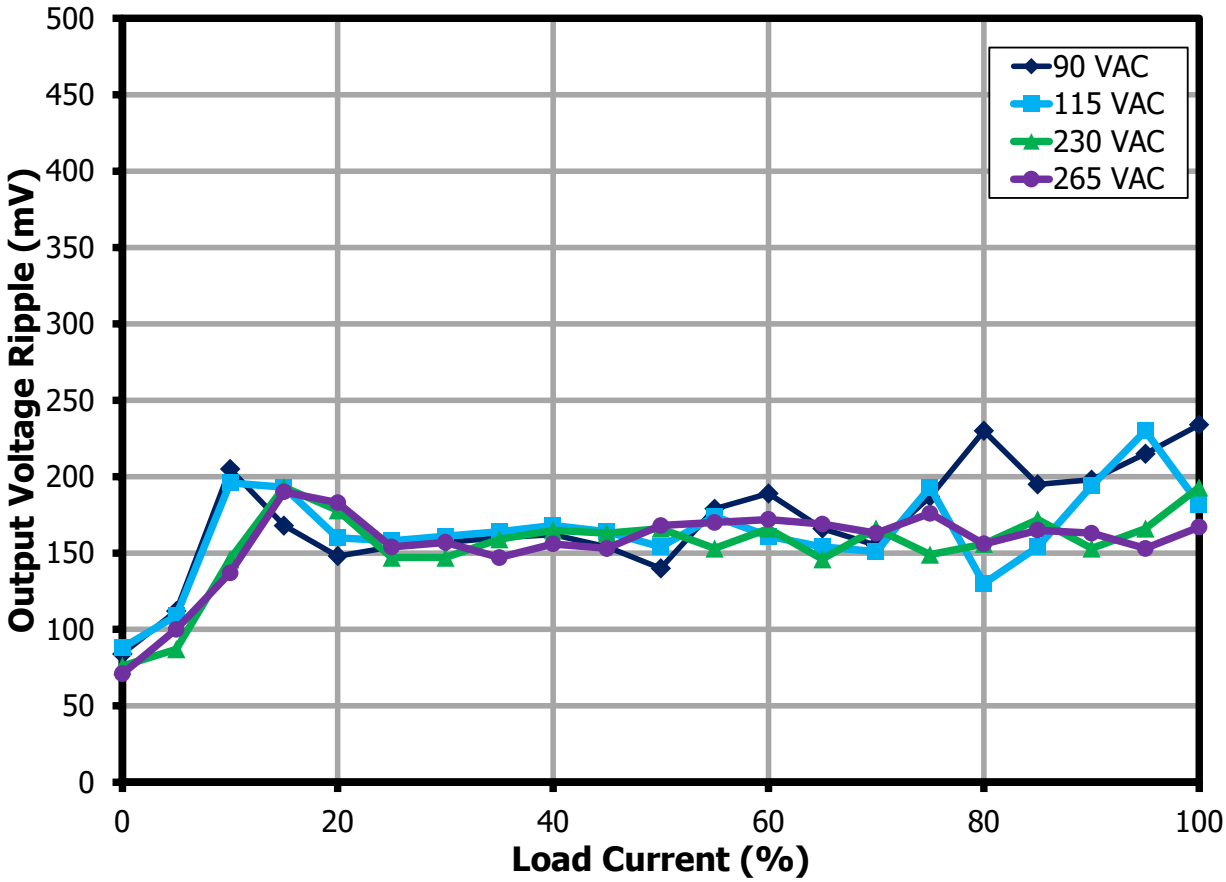


Figure 45 – Output Voltage Ripple vs. Output Load, Room Temperature.

15 CVCC Performance

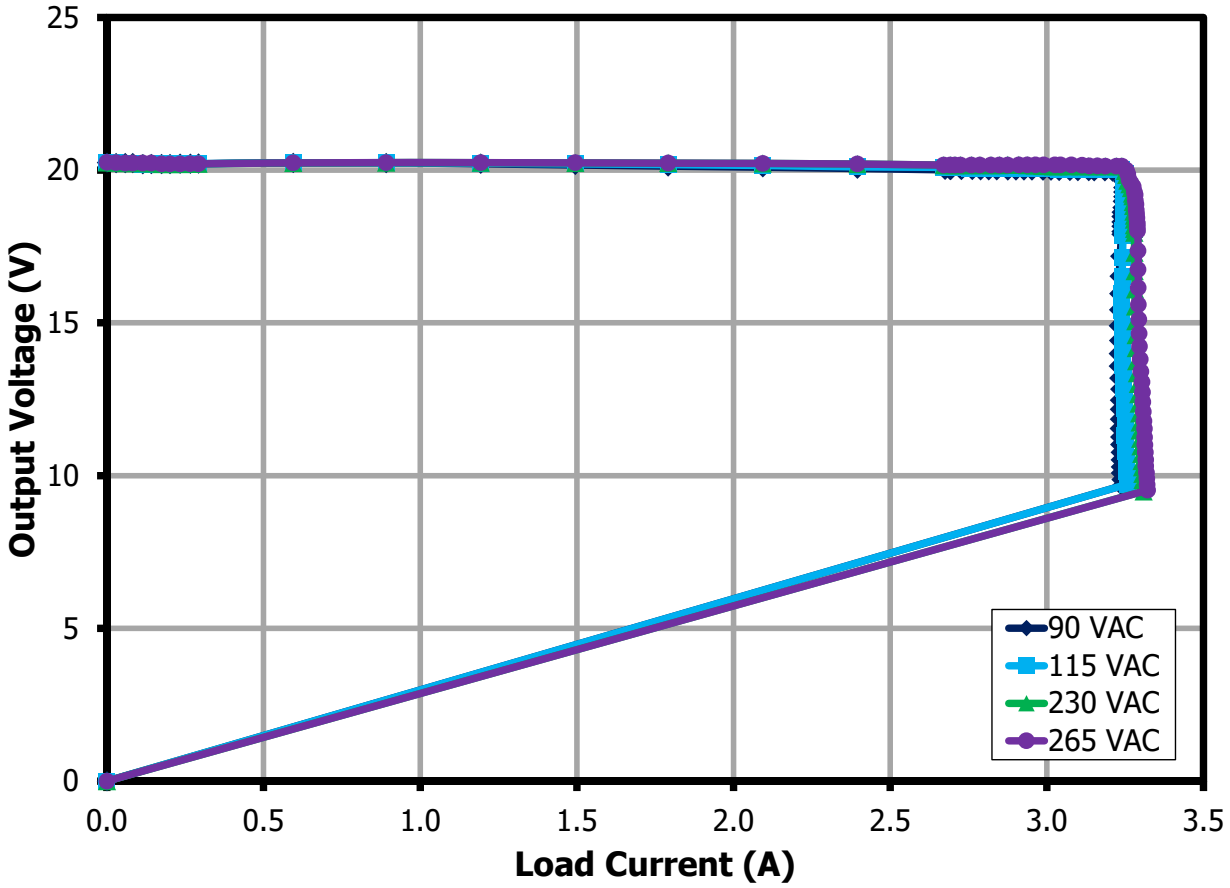


Figure 46 – Output Current vs. Output Voltage, Room Temperature.

16 Conducted EMI

16.1 *115 VAC Input*

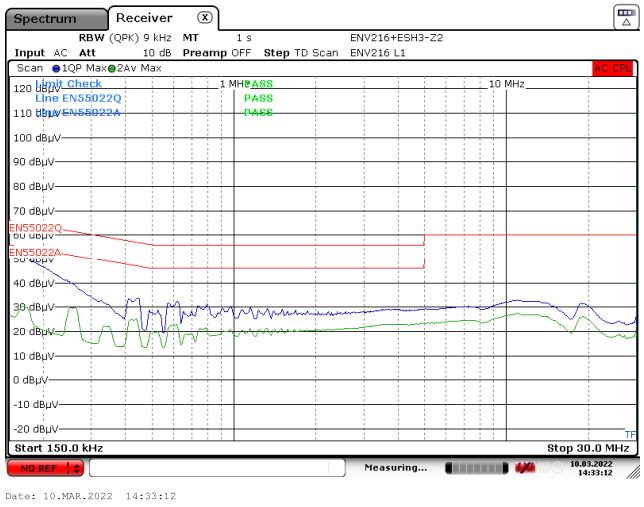


Figure 47 – 20 V / 3 A Load for 115 VAC – Line.

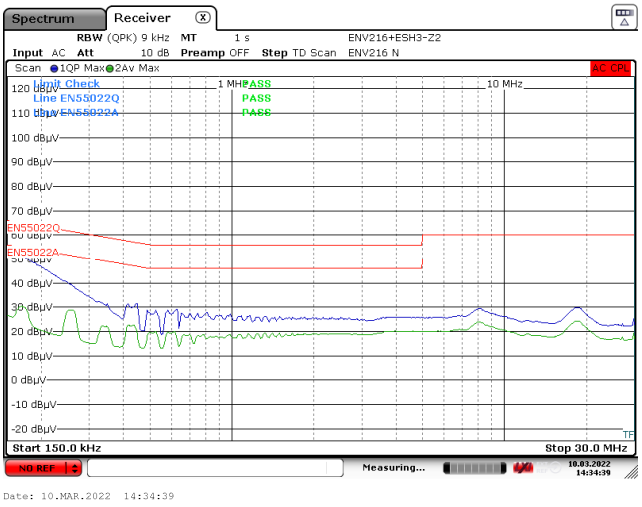


Figure 48 – 20 V / 3 A Load for 115 VAC – Neutral.

16.2 *230 VAC Input*

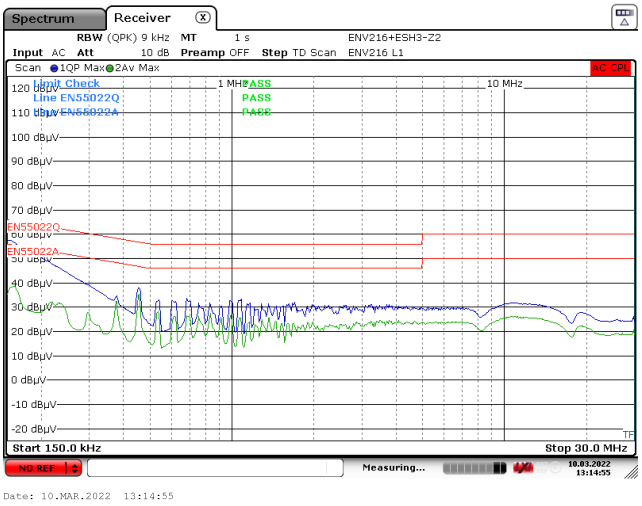


Figure 49 – 20 V / 3 A Load for 230 VAC – Line.

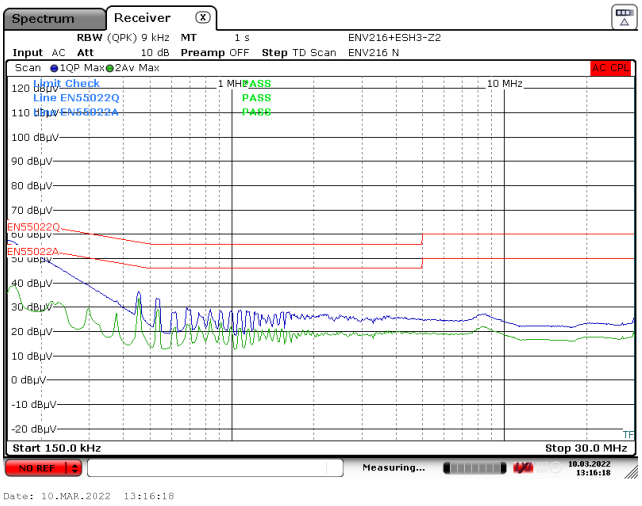


Figure 50 – 20 V / 3 A Load for 230 VAC – Neutral.

17 Line Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as a complete loss of function which is not recoverable.

17.1 *Differential Mode Surge (L to N), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+1000	0	10	Pass
-1000	0	10	Pass
+1000	90	10	Pass
-1000	90	10	Pass
+1000	180	10	Pass
-1000	180	10	Pass
+1000	270	10	Pass
-1000	270	10	Pass

17.2 *Common Mode Surge (L to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

17.3 *Common Mode Surge (N to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

17.4 *Common Mode Surge (L, N to PE), 230 VAC Input*

Surge Level (V)	Phase Angle (º)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

18 ESD

The unit was subjected to ±16.5 kV air discharge and ±8.8 kV contact discharge at the positive and negative nodes of the output with 10 strikes for each condition.

A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

18.1 *Air Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+16.5	VOUT	10	Pass
-16.5	VOUT	10	Pass
+16.6	GND	10	Pass
-16.5	GND	10	Pass

18.2 *Contact Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+8.8	VOUT	10	Pass
-8.8	VOUT	10	Pass
+8.8	GND	10	Pass
-8.8	GND	10	Pass

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
30-Jun-22	NAM/SS	1.0	Initial Release.	Apps & Mktg
24-Mar-23	NAM	1.1	Updated R12 in the Schematic, BOM and PCB Files	Apps & Mktg

For the latest updates, visit our website: www.power.com

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com