# Design Example Report

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|---|---|
| **Title** | **62 W Nominal Power Multi Output Flyback Converter with 3 CV Outputs Using InnoMux™2-EP IMX2379F** |
| **Specification** | 90 VAC – 265 VAC Input; 5 V / 4 A, 12 V / 1 A, 24 V / 1.25 A Outputs |
| **Application** | Appliances and Industrial |
| **Author** | Applications Engineering Department |
| **Document Number** | DER-716 |
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**Power Integrations**
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

## Summary and Features

Unique single-stage conversion, multiple-output, flyback architecture enabling:

- High efficiency across the universal line range
- High regulation accuracy - independently regulated 5 V / 4 A, 12 V / 1 A, 24 V / 1.25 A nominal current CV outputs
- Safety features
  - Output overvoltage protection (OVP), eliminating the need for a fault protection optocoupler
  - Output power limit set independently for each output
  - Accurate thermal protection with hysteretic shutdown
  - Input voltage monitor with accurate brown-in/brown-out and overvoltage protection\
  - Audible noise is 24dBA in operation mode, and 19 dBA in standby mode

InnoMux2-EP is the industry first single chip AC/DC with isolated, safety-rated integrated multiple feedbacks. In addition, the pulse sharing significantly reduces the audible noise to enable use in quiet appliances.

The control chip incorporates isolated feedback and communication channels, combining all the benefits of secondary-side control with the simplicity of primary-side regulation.

The new architecture achieves accurate cross regulation across multiple outputs and high overall efficiency while simplifying the overall system by obviating the need for post-regulation. The single-stage converter reduces board size significantly and reduces the part count compared to the equivalent conventional converter based on multiple conversion stage topology.

# Table of Contents

**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

# 1 Introduction

This engineering report describes a Switch Mode Power Supply (SMPS) intended for multi-output applications. The SMPS utilizes the Power Integration's InnoMux2-EP controller. The controller implements a multiplexing power control algorithm. Energy stored in the primary winding of the transformer during primary conduction interval is subsequently delivered to only one of the converter's main outputs (CV1, CV2 or CVHV). More specifically, this is achieved by controlling the switches SR FET, SEL1 and SEL2 (Figure 3). Utilizing a single magnetic component (transformer TX 1), the controller directs the energy flow as needed to all outputs based on respective loading requirements, thus keeping each output accurately controlled. If the energy pulse needs to be delivered to the CV1 output, SR FET and SEL1 are turned ON, if the energy pulse needs to be delivered to the CV2 output, SR FET and SEL2 are turned ON. Otherwise, if SEL1 and SEL2 are OFF, the energy is delivered to the CVHV output via the rectification diode.

The SMPS has three Constant Voltage (CV) outputs, 5 V / 4 A, 12 V / 1 A, 24 V / 1.25 A. The Power Supply Unit (PSU) can deliver a total maximum continuous output power of 62 W with universal mains input (from 90 VAC to 265 VAC).

**Figure 1 –** PCB, Top View.

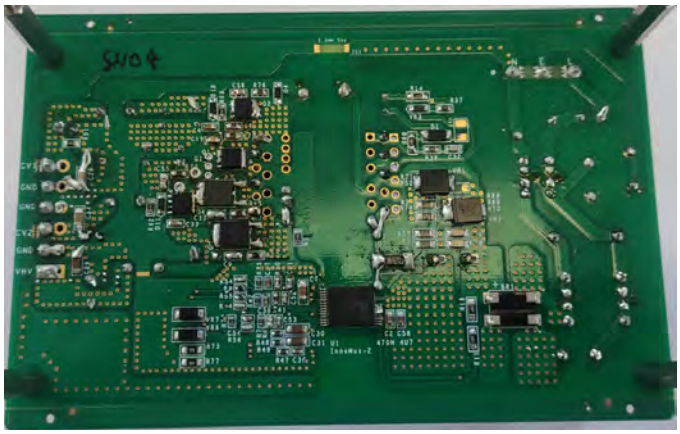


**Figure 2 –** PCB, Bottom View.

# 2 High Level Schematic

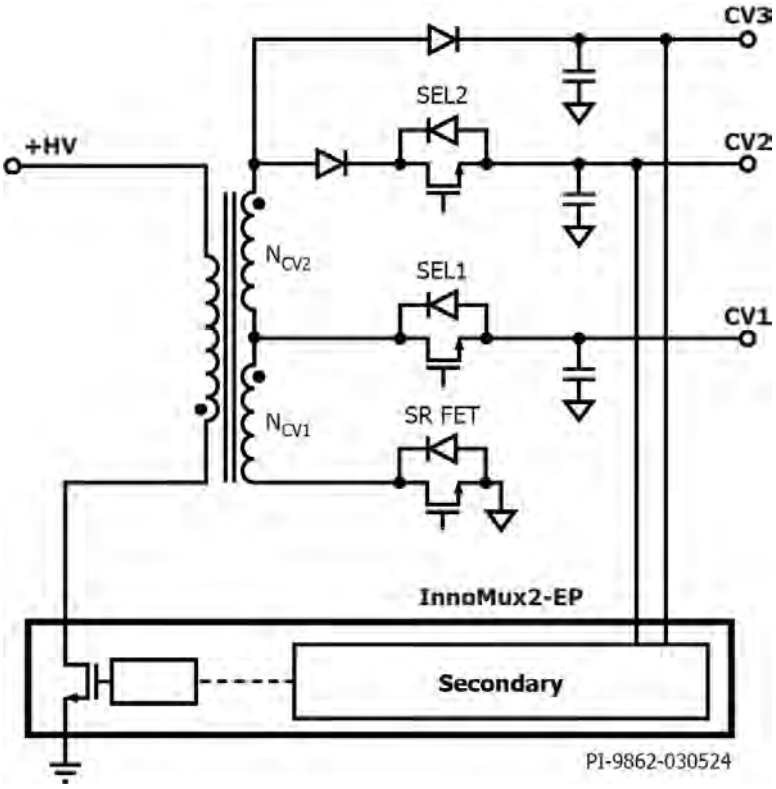



**Figure 3 –** DER-716 High Level Schematic.

The VCV1 and VCV2 and VCVHV FB pins continuously sense the output voltages. If the voltage of any of the outputs drops below regulation level, the multi-output controller InnoMux2-EP sends a request for pulse to primary-side controller. This type of pulse-by-pulse regulation results in quick response and excellent cross regulation. For the described multiplexing algorithm to work correctly, it is essential that the reflected voltage of each winding must be higher than that of the preceding lower output voltage winding to effectively steer the power:

$$\frac{V_{CV1}}{N_{CV1}} < \frac{V_{CV2}}{N_{CV1} + N_{CV2}} < \frac{V_{CVHV}}{N_{CV1} + N_{Cv2}}$$

Transformer with stacked or independent secondaries may be used as appropriate. The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

# 3 Power Supply Specification

The table below represents the minimum acceptable performance of the design. The actual performance is illustrated in the results section.

| Description | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Voltage | $V_{IN}$ | 90 | | 265 | VAC | 2 / 3 Wire Input. |
| Frequency | $f_{LINE}$ | 47 | 50/60 | 64 | Hz | |
| **Output** | | | | | | |
| Output Voltage 1 | $V_{OUT1}$ | 4.75 | 5 | 5.25 | V | ±5%. |
| Output Ripple Voltage 1 | $V_{RIPPLE1}$ | | | 150 | mV | 20 MHz Bandwidth. |
| Output Current 1 | $I_{OUT1}$ | 0 | | 4 | A | |
| Output Peak Current 1 | $I_{OUT1\_PK}$ | 0 | | 4 | A | |
| Output Voltage 2 | $V_{OUT2}$ | 11.4 | 12 | 12.6 | V | ±5%. |
| Output Ripple Voltage 2 | $V_{RIPPLE2}$ | | | 360 | mV | 20 MHz Bandwidth. |
| Output Current 2 | $I_{OUT2}$ | 0 | | 1 | A | |
| Output Peak Current 2 | $I_{OUT2\_PK}$ | 0 | | 1 | A | |
| Output Voltage 3 | $V_{OUT3}$ | 22.8 | 24 | 25.2 | V | ±5%. |
| Output Ripple Voltage 3 | $V_{RIPPLE3}$ | | | 720 | mV | 20 MHz Bandwidth. |
| Output Current 3 | $I_{OUT3}$ | 0 | | 1.25 | A | |
| Output Peak Current 3 | $I_{OUT3\_PK}$ | 0 | | 1.25 | A | |
| **Total Output Power** | | | | | | |
| Continuous Output Power | $P_{OUT}$ | | 62 | | W | |
| **Efficiency** | | | | | | |
| Full Load | η | 85 | | | % | Measured at 115 / 230 VAC, POUT 25 ºC. |
| No-Load Input Power | | | | <0.3 | W | Measured at 230 VAC 25 ºC, 5 V 30 mA |
| **Environmental** | | | | | | |
| Conducted EMI | | Meets CISPR22B / EN55022B | | | | |
| Safety | | | | | | |
| Surge Common Mode | | | | 2 | kV | Combination Wave, 12 Ω Common Mode. |
| Surge Differential Mode | | | | 1 | kV | Combination Wave, 2 Ω Differential Mode. |
| Ambient Temperature | $T_{AMB}$ | 0 | | 40 | ºC | Free Convection, Sea Level. |

# 4 Schematic

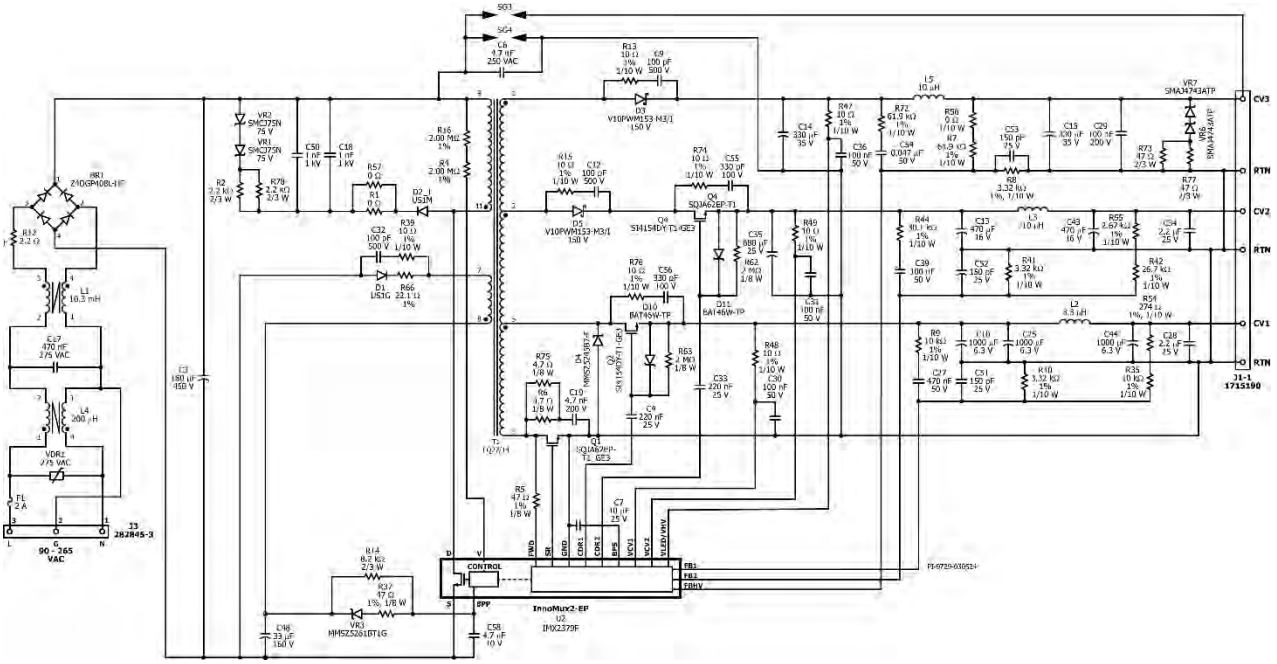



**Figure 4 –** Schematic.

# 5 Circuit Description

## *5.1 Input Rectifier and EMI Filter*

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode chokes L1 and L4 with capacitor C17 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC voltage across the filter capacitor C3. Varistor VDR1 provides protection against differential voltage surges. Resistor R12 (NTC) limits the inrush current. Capacitor C6 is used to mitigate the common mode EMI.

## *5.2 Primary-Side*

### 5.2.1 Primary Switch Arrangements

The transformer primary is connected between the input DC bus (TXPRI+) and the drain D of the integrated primary switch of InnoMux2-EP (U1 pin 28).

A Zener type primary clamp (VR1, VR2, R2, R78, C50, C18) is used to limit the peak drain voltage of U1 at the instant of turn-off of the switch inside U1.

### 5.2.2 Primary-Side Controller Power Source and OVP Protection

The primary-side controller is part of the InnoMux2-EP (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor C58, when AC voltage is first applied to the converter input. During normal operation (steady-state) the primary-side of the controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D1 and capacitor C48, and then connected to the BPP pin via a current limiting resistor R14.

### 5.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

A crude primary-side output overvoltage protection (OVP) is implemented by Zener diode VR3 and the series resistor R37. In the event of an uncontrolled overvoltage at the output, the auxiliary winding voltage increases and causes breakdown of VR3 which then causes a current to flow into the BPP pin of IC U1. If this current exceeds $I_{SD}$ threshold, InnoMux2-EP controller will latch off and prevent any further increase in output voltage.

Resistor R11 and R16 provide input voltage sense protection for undervoltage and overvoltage conditions.

### 5.2.4 Primary Peak Current Limit

The value of capacitor C58 is used to set the maximum primary current to STANDARD or to INCREASED level. In this case 4.7 µF capacitance sets the primary-side controller peak current limit to its INCREASED level of 2.45 A.

## *5.3 Secondary-Side*

The secondary-side of the InnoMux2-EP IC (U1) is powered from the 5 V BPS rail generated internally. Capacitor C7 is a local decoupling capacitor.

### 5.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoMux2-EP IC (U1) sends a request to the primary-side controller to initiate a switching cycle, by sending a pulse via the internal FluxLink™, a galvanically isolated communication channel.

### 5.3.2 InnoMux2-EP Power Supply

During start-up the InnoMux2-EP secondary-side controller is powered from FWD / VCVHV / VCV2 rail via R47 / R49. There is a local decoupling capacitor C36 and C31 connected close to the VCVHV and VCV2 pins of U1. Resistor R47 and R49 values and C36 and C31 are optional. An internal regulator reduces the VCVHV / VCV2 voltage to 5 V and outputs it to the BPS bus (U1 pin 6).

In steady-state the voltage on VCV1 is 5 V and there is a special case in the InnoMux2-EP (U1) IC, BPS direct power mode. When BPS voltage is within a suitable range (4.75 to 5.5 V), BPS voltage is supplied by CV1. Efficiency can be improved by using BPS direct power mode.

### 5.3.3 Selection MOSFETs Drive

The gate drive amplitude for the selection MOSFETs Q2 is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic level MOSFET is used. Capacitor C4 is charged up to the level of the $V_{CV1}$ from the CV1 via diode (D10) to the CDR1 pin. When the selection 1 MOSFET needs to be gated on, CDR1 pin voltage is raised from GND to BPS, and the selection MOSFET gate voltage (the other terminal of the capacitor C4) is lifted to $V_{CV1}+V_{BPS}$.

The gate drive amplitude for the selection MOSFETs Q4 is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic level MOSFET is used. Capacitor C33 is charged up to the level of the $V_{CV2}$ from the CV2 via diode (D11) to the CDR2 pin. When the selection 2 MOSFET needs to be gated on, CDR2 pin voltage is raised from GND to BPS, and the selection MOSFET gate voltage (the other terminal of the capacitor C33) is lifted to $V_{CV2}+V_{BPS}$.

The secondary control circuit in InnoMux2-EP IC needs access to the idle ring waveform to calculate its timing and facilitate valley switching. Such access is ensured through the FW pin by keeping Q1 on after the secondary conduction time has expired.

### 5.3.4 Output Control

Output rectification for the CV1 output is provided by the SR MOSFET Q1 and the CV1 selection MOSFET Q2. A Π – type LC filter (C10, C25, C44, C28 and L2) ensures low output ripple voltage. The first stage filter capacitors C10, C25, C44 have low ESR to minimize the switching noise. A small multilayer ceramic (MLCC) capacitor C28 is connected across the CV1 output terminals and provides low impedance bypass for any high frequency noise components.

Output rectification for the CV2 output is provided by the SR MOSFET Q1 and the CV2 selection MOSFET Q4 and diode D5. A Π – type LC filter (C35, C13, C43, C34 and L3) ensures low output ripple voltage. The first stage filter capacitors C35, C13, C43 have low ESR to minimize the switching noise. A small multilayer ceramic (MLCC) capacitor C34 is connected across the CV2 output terminals and provides low impedance bypass for any high frequency noise components.

Output rectification for the CVHV output is provided by the SR MOSFET Q1 and the CVHV rectifying diode D3. A Π – type LC filter (C14, C15, C29 and L5) ensures low output ripple voltage. The first stage filter capacitors C14 and C15 have low ESR to minimize the switching noise. A small multilayer ceramic (MLCC) capacitor C29 is connected across the CVHV output terminals and provides low impedance bypass for any high frequency noise components.

The V_CV1 output voltage is set by R54, R35 and R10 to FB1 (U1 pin 1). Loop compensation is provided by R9 and C27 due to the inclusion of L2. High frequency noise is decoupled by capacitor C51.

The V_CV2 output voltage is set by R55, R42 and R41 to FB2 (U1 pin 3). Loop compensation is provided by R44 and C39 due to the inclusion of L3. High frequency noise is decoupled by the capacitor C52.

The V_CVHV output voltage is set by R56, R7 and R8 to FB3 (U1 pin 8). Loop compensation is provided by R72 and C54 due to the inclusion of L5. High frequency noise is decoupled by capacitor C53.

High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced in SR MOSFET via an RC snubber formed by resistors R6 and R75 and capacitor C19.

High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced in SEL1 MOSFET via an RC snubber formed by resistors R76 and capacitor C56.

High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced in SEL2 MOSFET via an RC snubber formed by resistors R74 and capacitor C55.

High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced in CV2 diode via an RC snubber formed by resistors R15 and capacitor C12.

High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced in CVHV diode via an RC snubber formed by resistors R13 and capacitor C9.

Zener diode D4 is used as a voltage clamp for the transformer CV1 winding.

Zener diodes VR6 and VR7 are used to limit the maximum CVHV voltage which can be predominantly caused by the leakage in the transformer.

### 5.3.5 Output Power Limiting

A power limit is implemented individually for each output and set by controller configuration (InnoMux2-EP IC). Power limit is disabled by default. The power delivered to any of the outputs is restricted by limiting the maximum average frequency at which an output can receive. Namely, power limit bits set the frequency limit for output CV1, CV2 and CVHV. If the frequency is exceeded for a predetermined time interval, the InnoMux2-EP controller will execute auto-restart or latch-off.

### 5.3.6 Start-Up Sequence

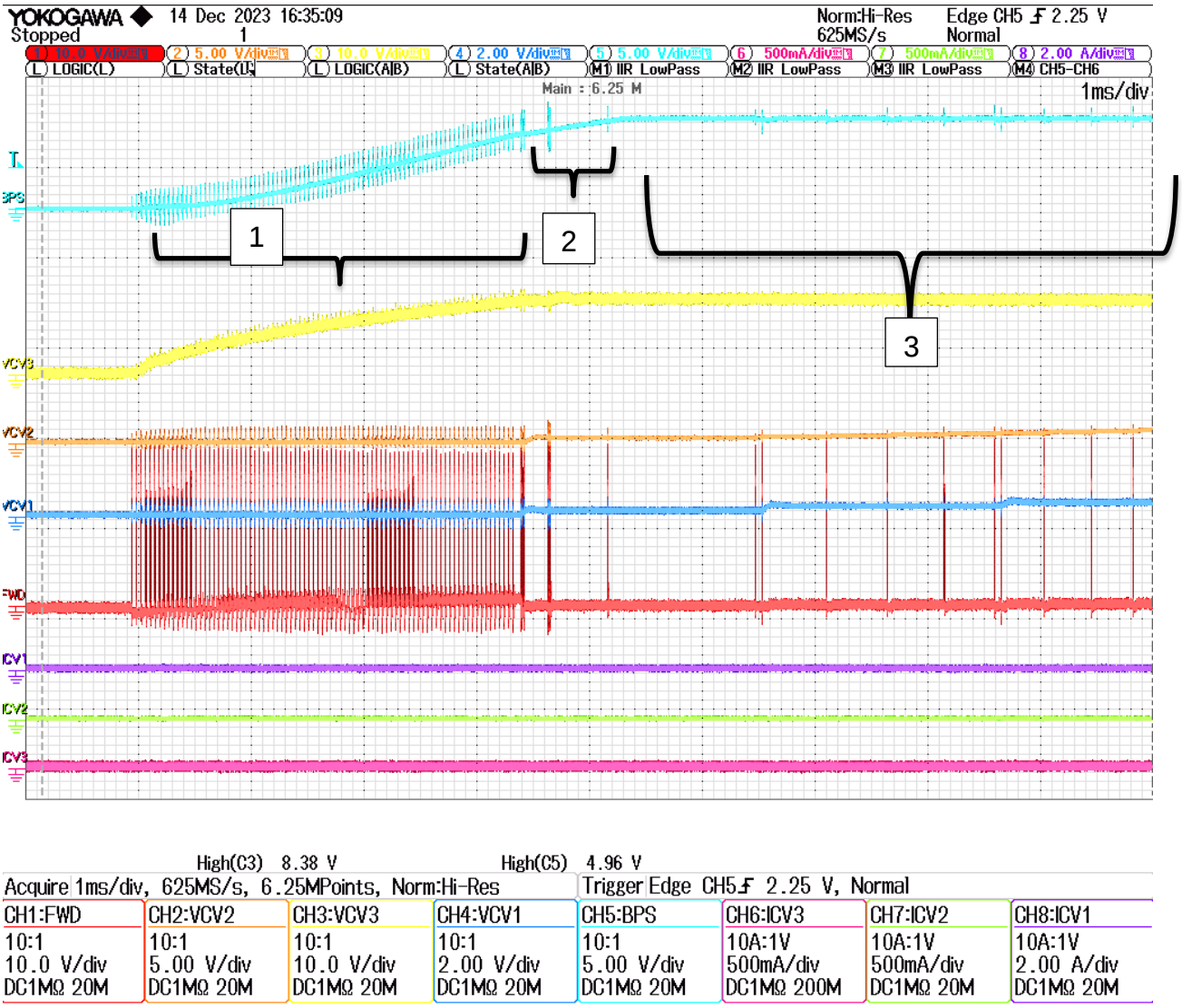



**Figure 5 –** First 10 ms of Start-Up.

1. The secondary-side controller is powered-down (asleep). The primary-side controller operates open-loop at a fixed frequency of about 25 kHz. The peak current is set to approximately 30% of its maximum level. If the secondary-side does not wake up and respond, the primary-side will:
   a. time out and shut down, or
   b. the primary-side bias voltage will rise high enough to trigger a bias OVP shutdown.

2. The CVHV output is the only output to rise significantly during interval 1. It can provide power to InnoMux2-EP (U1) internal secondary voltage regulator (BPS regulator), which generates the internal supply bus BPS (+5 V). Eventually the internal voltage regulator establishes 5 V at the BPS pin. IC U1 secondary-side controller then wakes up from its power-on-reset and start hand-shaking with the primary controller to take over the control of InnoMux2-EP IC. Hand-shaking pulse and SEL signals to indicate the handshake. Also need to point out what happens to secondary if handshake failed.

3. After hand-shaking, the fixed 25 kHz switching frequency is ended, and InnoMux2-EP (U1) switching according to the feedback and reference voltages on CV1, CV2 and CVHV(CV3). The CV1 and CV2 voltages are linearly raised, while the CV3 voltage is maintained at the stay-alive voltage ($V_{STAYALIVE}$, ~8.0 V) to provide input to the internal BPS regulator. While the VCV1 and VCV2 are raised to the same reference percentage as the VCV3, InnoMux2-EP IC (U1) starts ramping up both of the three output voltages simultaneously (VCV1, VCV2 and VCV3) to their references.

4. CV1, CV2 and CV3 output voltages can be seen to rise simultaneously at interval 4 until reaching their FB voltage levels .

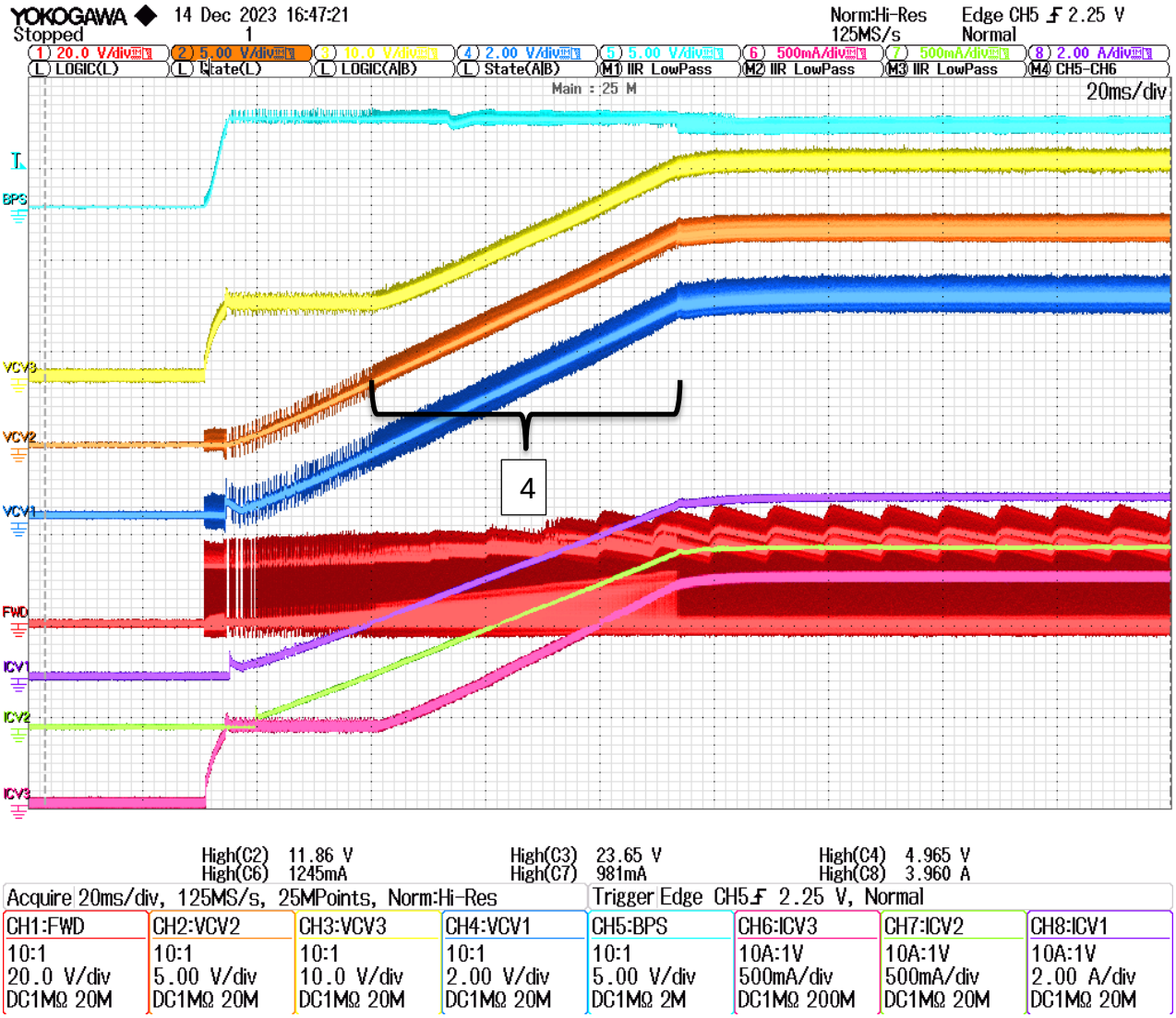



**Figure 6 –** Complete Start-Up Cycle.

# 6 PCB Layout

The converter PCB layout is illustrated in Figures 7, 8 and 9 below. PCB copper thickness is 2 oz (2.8 mils / 70 μm) was used for the PCB.

(1) FWD pin: FWD signal has large dv/dt, which can be one of the major noise source on the secondary circuit. Its PCB route should be kept away from the other signals.

(2) Ground plane: The impedance from InnoMux2-EP controller's ground to ANODE terminal of auxiliary rectifier diode (D1) should be minimized or separated from the power return ground. Star connection ground can be used here, to prevent the large secondary discharge current from affecting the ground level of the InnoMux2-EP controller.

(3) Thermal: The primary switch in InnoMux2-EP IC (U1) is cooled through the exposed pad and SOURCE pin of the IC. Care should be taken that their thermal impedance to the cooling copper of the PCB is kept to a minimum.

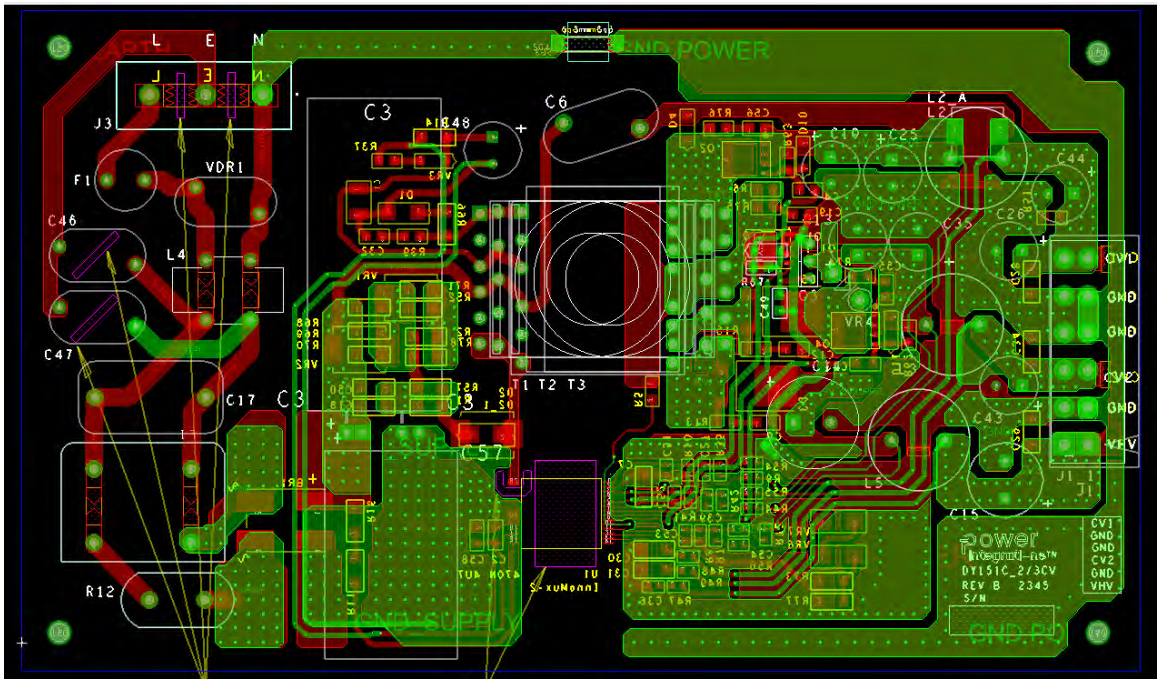



**Figure 7 –** Printed Circuit Layout.

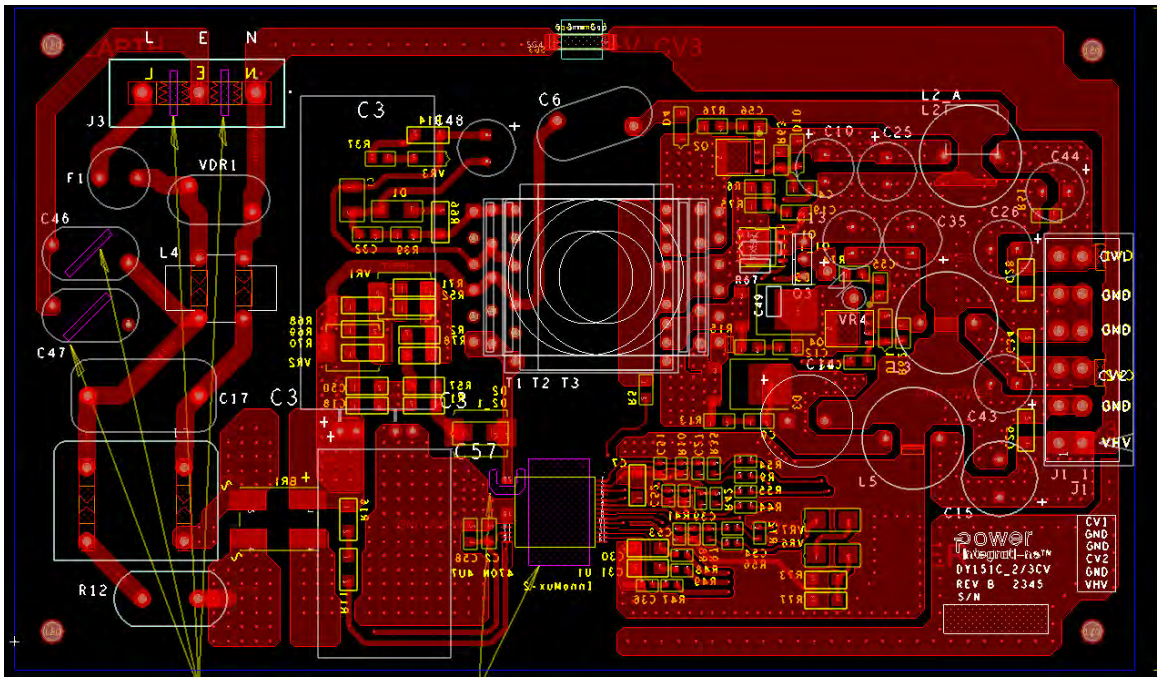



**Figure 8 –** Printed Circuit Layout, Bottom.

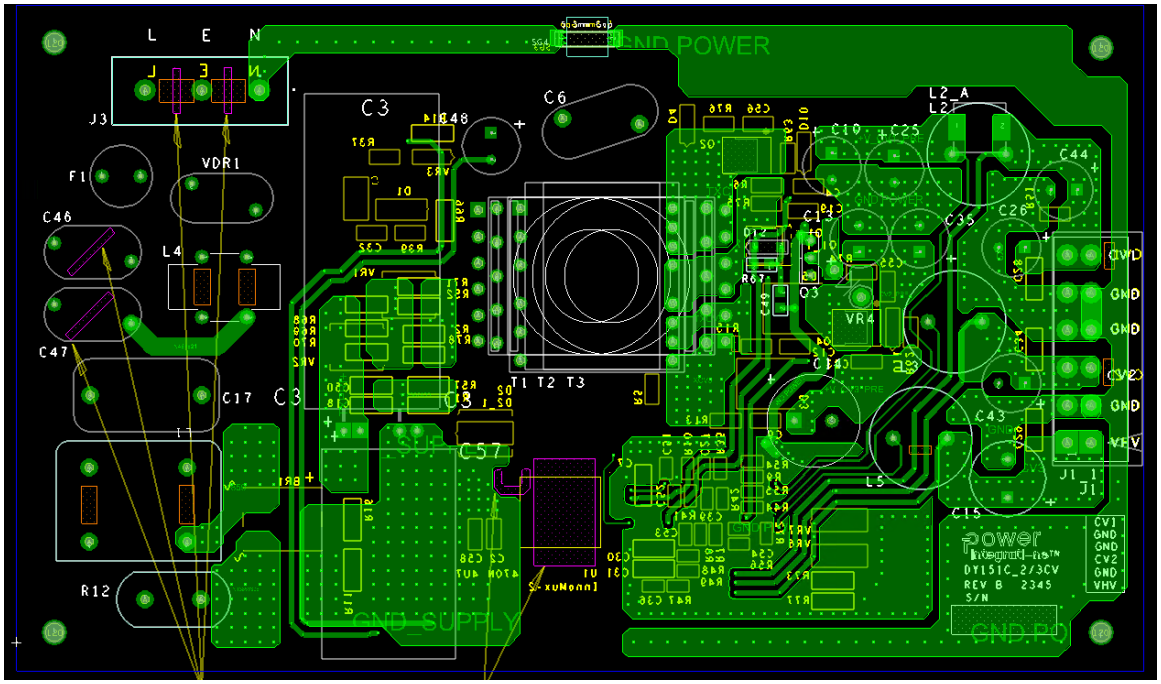



**Figure 9 –** Printed Circuit Layout, Top.

# 7 Bill of Materials

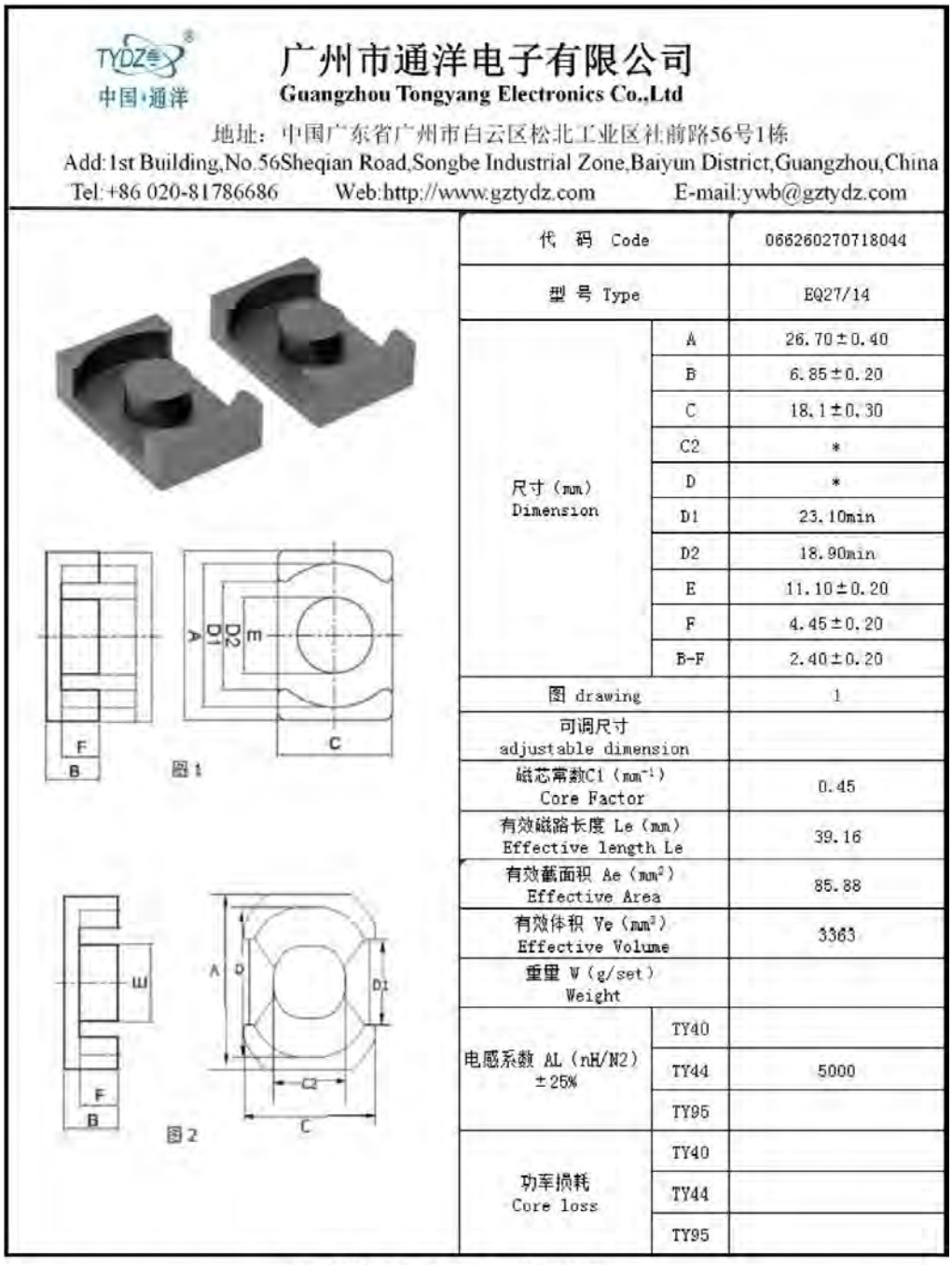
| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | BR1 | RECT BRIDGE, GP, 800 V, 4 A, Z4-D | Z4DGP408L-HF | Comchip |
| 2 | 1 | C3 | 150 µF, 450 V, Electrolytic, (18 x 40) | UPH2W151MHD | Nichicon |
| 3 | 2 | C4 C33 | 220 nF, 25 V, Ceramic, X7R, 0805 | CC0805KRX7R8BB224 | Yageo |
| 4 | 1 | C6 | 4.7 nF, Ceramic, Y1 | 440LD47-R | Vishay |
| 5 | 1 | C7 | 10 µF, ±10%, 25 V, Ceramic Capacitor X7R, 1206 | C1206C106K3RACAUTO | KEMET |
| 6 | 3 | C9 C12 C32 | 100 pF, 500 V, Ceramic, NP0, 0805 | 501R15N101KV4T | Johanson Dielectrics |
| 7 | 2 | C10 C25 | 1000 µF,20%, 6.3 V, Al Organic Polymer, Gen. Purpose, 2000 Hrs @ 105°C, (8 x 8 mm) | RL80J102MDN1KX | Nichicon |
| 8 | 1 | C13 | 470 µF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5) | RNE1C471MDN1 | Nichicon |
| 9 | 2 | C14 C15 | 330 µF, ±20%, 35 V, Aluminium Polymer Capacitor Radial, Can, 18 mΩ, 1000 Hrs @ 125°C | 35SEK330M | Panasonic |
| 10 | 1 | C17 | 470 nF, 275 VAC, Film, X2 | 80-R46KI347050P1M | Kemet |
| 11 | 2 | C18 C50 | 1 nF, 1000 V, Ceramic, X7R, 1206 | CC1206KKX7RCBB102 | Yageo |
| 12 | 1 | C19 | 4700 pF, ±10%, 200 V, Ceramic Capacitor, X7R, 0805 | C0805C472K2RECAUTO | KEMET |
| 13 | 1 | C27 | 470 nF, 50 V, Ceramic, X7R, 0603 | UMK107B7474KA-TR | Taiyo Yuden |
| 14 | 2 | C28 C34 | 2.2 µF, ±10%, 25 V, Ceramic, X7R, 1206 | 12063C225K4Z2A | AVX Murata |
| 15 | 1 | C29 | 100 nF, 200 V, Ceramic, X7R, 1206 | VJ1206Y104KXCAT | Vishay |
| 16 | 2 | C30 C31 | 100 nF, 50 V, Ceramic, X7R, 1206 | CC1206KRX7R9BB104 | Yageo |
| 17 | 1 | C35 | 680 µF, 25 V, Aluminium-Polymer, 16mΩ, 2000 Hrs @ 105 °C, (8 x 16) | A750KW687M1EAAE016 | KEMET |
| 18 | 2 | C36 C39 | 0.1 µF (100 nF) ±10% 50 V Ceramic Capacitor X7R 0603 | GCM188R71H104KA57D | Murata |
| 19 | 1 | C43 | 470 µF, 16 V, Electrolytic, Very Low ESR, 53 mΩ, (8 x 15) | EKZE160ELL471MH15D | Nippon Chemi-Con |
| 20 | 1 | C44 | 1000 µF, 6.3 V, Electrolytic, Gen Purpose, (8 x 11.5) | ECA-0JHG102 | Panasonic |
| 21 | 1 | C48 | 33 µF, ±20%, 160 V, Al Electrolytic, (8 x 14) | EGW2CM330F14OT | AiSHi |
| 22 | 3 | C51 C52 C53 | 150 pF, 5%, 250 V, Ceramic, COG, 0603 | C1608C0G2E151J080AA | TDK |
| 23 | 1 | C54 | 0.047 µF, ±10%, 50 V, Ceramic Capacitor X7R, 0603 | C0603C473K5RAC7867 | KEMET |
| 24 | 1 | C55 | 330 pF, 500 V, Ceramic, X7R, 0805 | C0805C331KCRACTU | Panasonic |
| 25 | 1 | C56 | 330 pF, ±10%, 100 V, Ceramic, X7R, 0805 | C0805C331K1RACTU | Kemet |
| 26 | 1 | C58 | 4.7 µF ±10% 10V Ceramic Capacitor X7R 0805 | LMK212B7475KGHT | Taiyo Yuden |
| 27 | 1 | D1 | Diode ULTRA FAST, GPP, 400 V, 1 A SMA | US1G-13-F | Diodes, Inc. |
| 28 | 1 | D2_1 | Diode, Standard, 1000 V, 1 A, SMT DO-214AC (SMA) | US1M-TP | Micro Commercial |
| 29 | 2 | D3 D5 | Diode, Schottky, 150 V, 10 A, SMT Slim DPAK, TO-252AE | V10PWM153-M3/I | Vishay |
| 30 | 1 | D4 | Diode ZENER 15 V 500 mW SOD123 | MMSZ5245B-7-F | Diodes, Inc. |
| 31 | 2 | D10 D11 | Diode, Schottky, 100 V, 0.075 A, SOD123 | BAT46W-TP | Micro Commercial |
| 32 | 1 | F1 | 2 A, 250 V, Slow, TR5 | 37212000411 | Wickman |
| 33 | 1 | J1_1 | 6 Position (1 x 6) header, 5 mm (0.196) pitch, Vertical | 1715190 | Phoenix Contact |
| 34 | 1 | J3 | 3 Position Wire to Board Terminal Block (7.62 mm) | 282845-3 | TE Connectivity |
| 35 | 1 | L1 | CMC 10.3 MH 2.0 A 0.15 Ω WIDE IMP | SSR21NVS-M20103 | KEMET |
| 36 | 1 | L2 | FIXED IND, 3.3 µH, ±20%, 5.2 A, 16 MΩ, TH | ELC10D3R3E | Panasonic |
| 37 | 2 | L3 L5 | 10 µH, Unshielded Wirewound Inductor, 3.45 A, 15 mΩ Max, Radial, Vertical Cylinder | 18R103C | Murata Power |

| | | | | | |
|---|---|---|---|---|---|
| 38 | 1 | L4 | 200 µH @ 100 kHz Common Mode Choke | 30-00512-00 | Power Integrations |
| 39 | 2 | Q1 Q4 | MOSFET, N-Channel, 60 V, 60 A (Tc), 68 W (Tc), PowerPAK® SO-8 | SQJA62EP-T1_GE3 | Vishay |
| 40 | 1 | Q2 | MOSFET, N-Channel, 40 V, 36 A (Tc), 3.5 W (Ta), 7.8 W (Tc), SO-8 | SI4154DY-T1-GE3 | Vishay |
| 41 | 2 | R1 R57 | RES, 0 Ω, Jumper, ¼ W, Chip Resistor 1206 | RC1206JR-070RL | Yageo |
| 42 | 2 | R2 R78 | RES, 2.2 kΩ, 5%, 2/3 W, Thick Film, 1206 | ERJ-P08J222V | Panasonic |
| 43 | 2 | R5 R37 | RES, 47.0 Ω, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF47R0V | Panasonic |
| 44 | 2 | R6 R75 | RES, 4.7 Ω, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ4R7V | Panasonic |
| 45 | 2 | R7 R72 | RES, 61.9 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF6192V | Panasonic |
| 46 | 3 | R8 R10 R41 | RES, 3.32 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF3321V | Panasonic |
| 47 | 2 | R9 R35 | RES, 10.0 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF1002V | Panasonic |
| 48 | 2 | R11 R16 | RES, 2.00 MΩ, 1%, ¼ W, Thick Film, 1206 | ERJ-8ENF2004V | Panasonic |
| 49 | 1 | R12 | NTC Thermistor, 1.3 Ω, 7 A | MF72-001.3D13 | Cantherm |
| 50 | 5 | R13 R15 R39 R74 R76 | RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF10R0V | Panasonic |
| 51 | 1 | R14 | RES, 8.2 kΩ, 5%, 2/3 W, Thick Film, 1206 | ERJ-P08J822V | Panasonic |
| 52 | 1 | R42 | RES, 26.7 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF2672V | Panasonic |
| 53 | 1 | R44 | RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF3012V | Panasonic |
| 54 | 3 | R47 R48 R49 | RES, 10 Ω, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF10R0V | Panasonic |
| 55 | 1 | R54 | RES, 274 Ω, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF2740V | Panasonic |
| 56 | 1 | R55 | RES, 2.67 kΩ, 1%, 1/10 W, Thick Film, 0603 | ERJ-3EKF2671V | Panasonic |
| 57 | 1 | R56 | RES,0 Ω Jumper, 1/10 W Chip Resistor 0603 | RC0603FR-070RL | Yageo |
| 58 | 2 | R62 R63 | RES, 2 MΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ205V | Panasonic |
| 59 | 1 | R66 | RES, 22.1 Ω, 1%, ¼ W, Thick Film, 1206 | ERJ-8ENF22R1V | Panasonic |
| 60 | 2 | R73 R77 | RES, 47 Ω, 5%, 2/3 W, Thick Film, 1206 | ERJ-P08J470V | Panasonic |
| 61 | 1 | T1 | Bobbin, EQ27/14, 11 pins, 6pri, 5sec | YT-2701 | www.dgytdz.com |
| 62 | 1 | U2 | InnoMux2-EP, InSOP-T28D (No EP) | IMX2379F | Power Integrations |
| 63 | 1 | VDR1 | 275 VAC, 5 J, 10 mm, RADIAL | V275LA10P | Littlefuse |
| 64 | 2 | VR1 VR2 | TVS Diode, Unidirectional, 75 V Reverse Standoff, 121 V Clamp (DO-214AB) | SMCJ75A | Littelfuse |
| 65 | 1 | VR3 | Diode ZENER 47 V 500 mW SOD123 | MMSZ5261BT1G | ON Semi |
| 66 | 2 | VR6 VR7 | Zener Diode, 13 V, 1 W, ±5%, SMT DO-214AC (SMA) | SMAJ4743A-TP | Micro Commercial |

# 8 Transformer (T1) and CMC (L4) Specification

## *8.1 Core Information*

Core EQ27/14, Guangzhou Tongyang Electronics Part No. 066260270718044



广州市通洋电子有限公司
Guangzhou Tongyang Electronics Co.,Ltd
地址：中国广东省广州市白云区松北工业区社前路56号1栋
Add:1st Building,No.56Sheqian Road,Songbe Industrial Zone,Baiyun District,Guangzhou,China
Tel:+86 020-81786686 Web:http://www.gztydz.com E-mail:ywb@gztydz.com



| 代 码 Code | | 066260270718044 |
|---|---|---|
| 型 号 Type | | EQ27/14 |
| 尺寸（mm） Dimension | A | 26.70±0.40 |
| | B | 6.85±0.20 |
| | C | 18.1±0.30 |
| | C2 | * |
| | D | * |
| | D1 | 23.10min |
| | D2 | 18.90min |
| | E | 11.10±0.20 |
| | F | 4.45±0.20 |
| | B-F | 2.40±0.20 |
| 图 drawing | | 1 |
| 可调尺寸 adjustable dimension | | |
| 磁芯常数C1（$mm^{-1}$） Core Factor | | 0.45 |
| 有效磁路长度 Le（mm） Effective length Le | | 39.16 |
| 有效截面积 Ae（$mm^2$） Effective Area | | 85.88 |
| 有效体积 Ve（$mm^3$） Effective Volume | | 3363 |
| 重量 W（g/set） Weight | | |
| 电感系数 AL（nH/N2） ±25% | TY40 | |
| | TY44 | 5000 |
| | TY95 | |
| 功率损耗 Core loss | TY40 | |
| | TY44 | |
| | TY95 | |

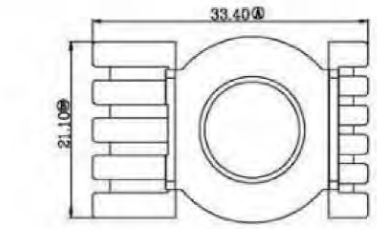
磁芯可按客户尺寸开模，可以开气隙。
We can open the mould or grind air gap for the ferrite core as per customer's requirement and size.

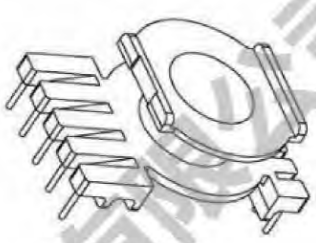
**Figure 10 –** EQ27/14 Core.

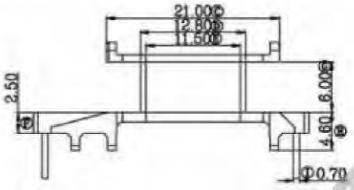
## 8.2 Bobbin Information

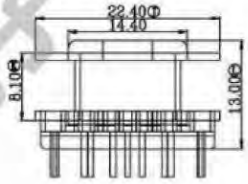
RoHS

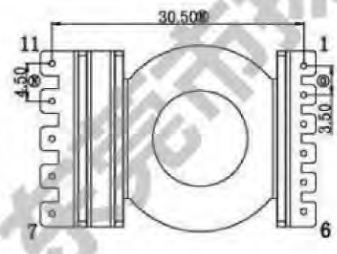
EQ27变压器骨架电木骨架高频骨架电源骨架YT-2701

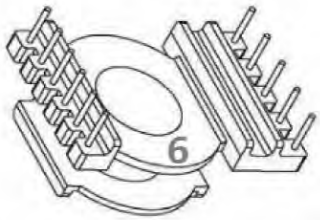





| | | | | | | |
|---|---|---|---|---|---|---|
| 东莞市洋通电子有限公司<br>广东省东莞市石碣镇,刘屋工业区 | | | NAME | | EQ27变压器骨架YT-2701<br>http://www.dgytdz.com/ | |
| TEL.电话 | 0769-86309483 | TOLERANCE | MATERIAL | | | PHENOLIC |
| FAX.传真 | 0769-89026473 | 0<L≤4 ±0.2<br>4<L≤16 ±0.3<br>16<L≤63±0.4 | SCALE | | DRWA BY | 张 阳 |
| | | | 4/1 | | CHECK | 张 艺 |
| E--mail | wydz001@126.com | Pin pitch±0.2 | UNIT | mm | DATE | 2014.03.2 |

**Figure 11 –** Guangzhou Tongyang Electronics – 11 Pin Bobbin – YT-2701.

### *8.3 Electrical Diagram*

Pin number 5 and pin number 6 need to be short-circuited on PCB board.

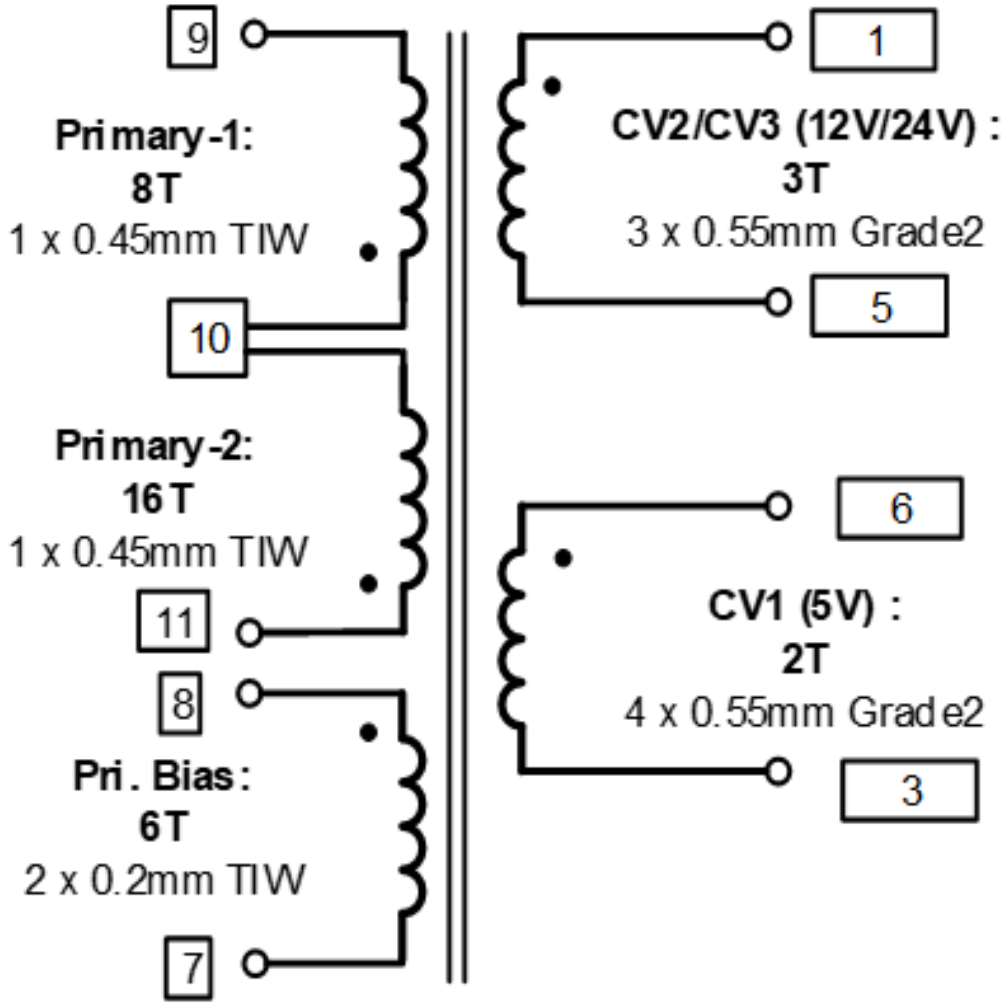



**Figure 12 –** Transformer Electrical Diagram.

## 8.4 Winding Stack Diagram

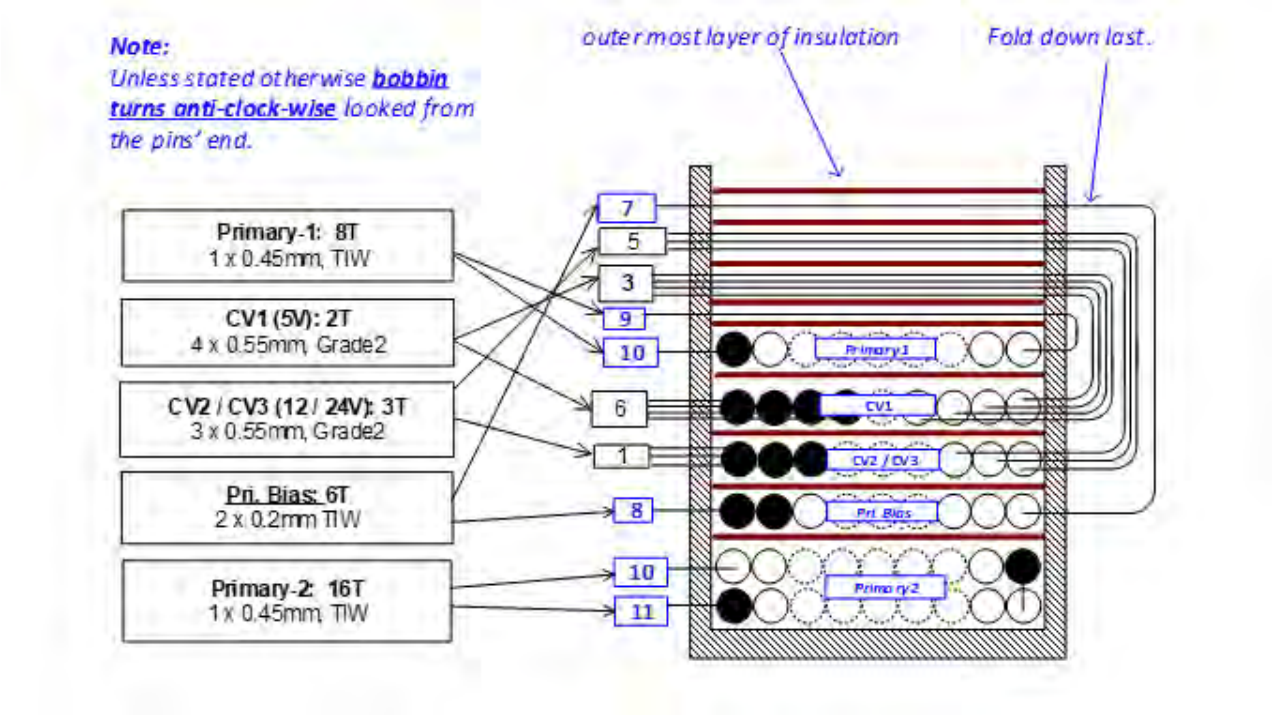



**Figure 13 –** Transformer Build Diagram.

## 8.5 Transformer Electrical Specification

| Parameter | Condition | Spec. |
|---|---|---|
| **Electrical strength** | 1 second, 60 Hz from pins 1-6 to 7-13. | 3000 VAC |
| **Nominal Primary Inductance** | Measured at 1 VPK-PK, 100 kHz switching frequency, between pin 9 and 11, with all other windings open. | 188 µH ±5% |
| **Resonant Frequency** | Between pin 9 and 11, other windings open. | 1100 kHz (Min.) |
| **Primary Leakage Inductance** | Between pin 9 and 11, with all secondary 1,3,5 and 6 are shorted. | 9 µH (Max.) |

## 8.7 List of Materials

| Item | Description | Quantities |
|---|---|---|
| [1] | Core: Ferroxcube Part No. EQ27/14 TY44. | 2 |
| [2] | Bobbin: EQ27 YT-2701. | 1 |
| [3] | Magnet Wire: 0.55 mm ECW Gr 2. | |
| [4] | Magnet Wire: 0.45 mm, Triple Insulated Wire. | |
| [5] | Magnet Wire: 0.2 mm, Triple Insulated Wire. | |
| [6] | Barrier Tape: Polyester Film, 2.5±0.5 mil thickness, 6 mm Wide. | |
| [7] | Varnish: MR8008B - Varnish, Insulating, Polyurethane, Transparent/Amber EMR8008B250ML Or BC-359. | |

## 8.8 Transformer Construction

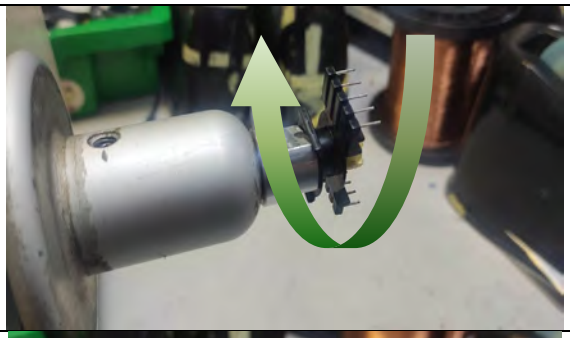
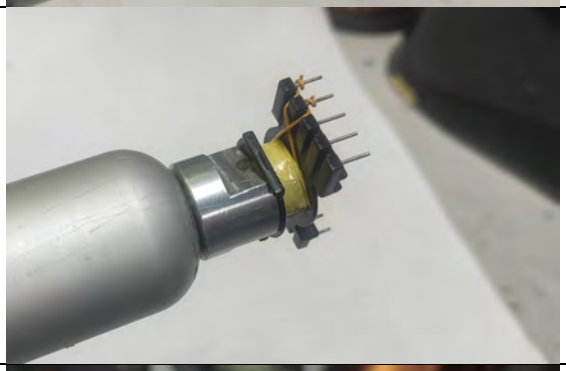
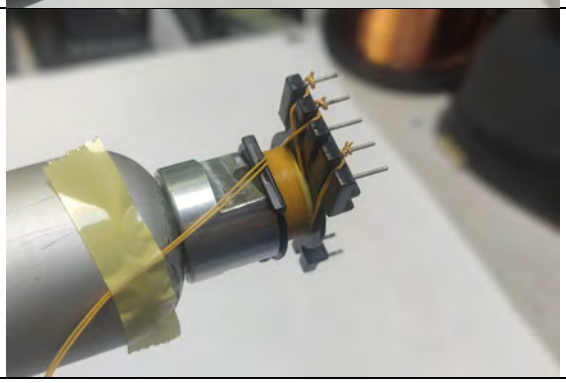
| | |
|---|---|
| **Layer 1&2 Primary-1** | Start at pin 11, wind 16 turns of 1 wire Item [4] in 2 layers with tight tension. Terminate at pin 10. |
| **Insulation** | Place 1 layers of tape Item [6] for insulation. |
| **Layer 3 Primary Bias** | Start at pin 8, wind 6 turns of 2 wire Item [5] in 1 layer with tight tension. Cut to leave about 5cm and tape to mandrel bobbin |
| **Insulation** | Place 1 layer of tape Item [6] for insulation. |
| **Layer 3 CV2&CV3** | Start at pin 1, wind 3 turns of 3 wire Item [3] in 1 layer with tight tension. Cut to leave about 5 cm and tape to mandrel bobbin |
| **Insulation** | Place 1 layer of tape Item [6] for insulation. |
| **Layer 4 CV1** | Start at pin 6, wind 2 turns of 4 wire Item [3] in 1 layer with tight tension. Cut to leave about 5 cm and tape to mandrel bobbin |
| **Insulation** | Place 1 layer of tape Item [6] for insulation. |
| **Layer 6 Primary-2** | Start at pin 10, wind 8 turns of 1 wire Item [4] in 1 layer with tight tension. Terminate at pin 9. |
| **Insulation** | Place 1 layer of tape Item [6] for insulation. |
| **Termination** | Terminate the CV1 windings at pin number 3. |
| **Termination** | Terminate the CV2/CV3 winding at pin number 5. |
| **Termination** | Terminate primary bias winding at pin number 7. |
| **Insulation** | Place 2 layers of tape Item [6] for insulation. |
| **Finish Assembly** | Gap core halves to 188 μH ±3% inductance.<br>Insert cores and tape tightly together Item [8].<br>Label “XXX.X μH” (XXX.X = measured primary inductance value in μH)<br>Varnish – Item [11]. |

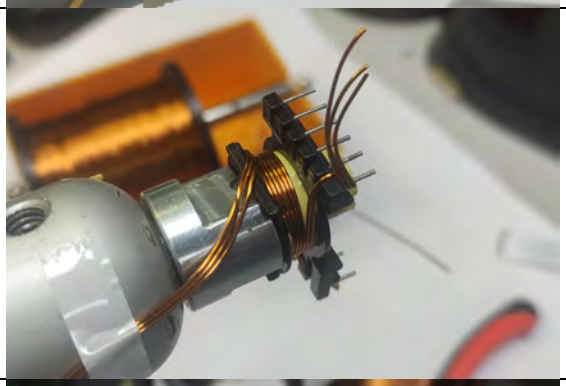
## 8.9 Transformer Test

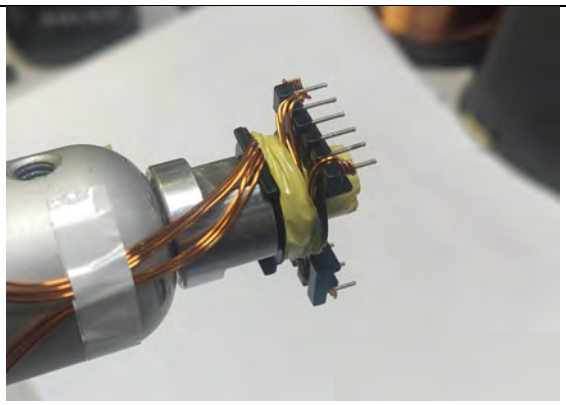
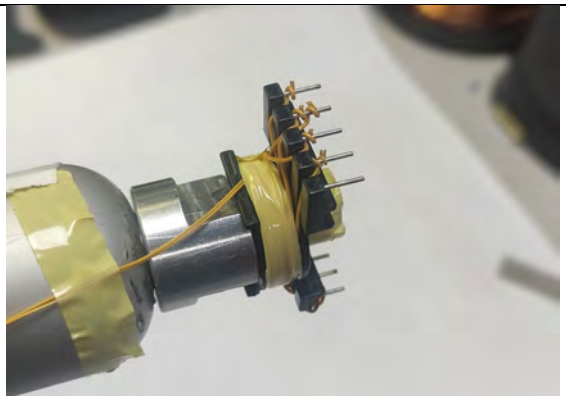
The winding measured inductance of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

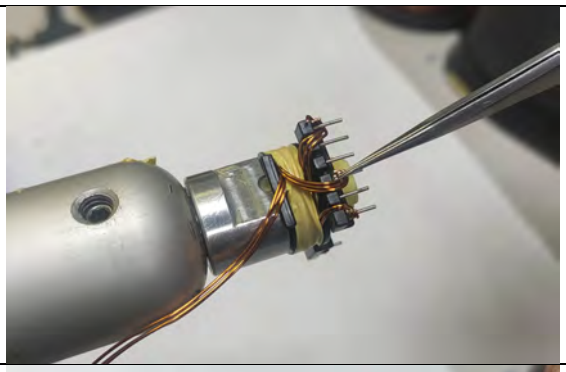
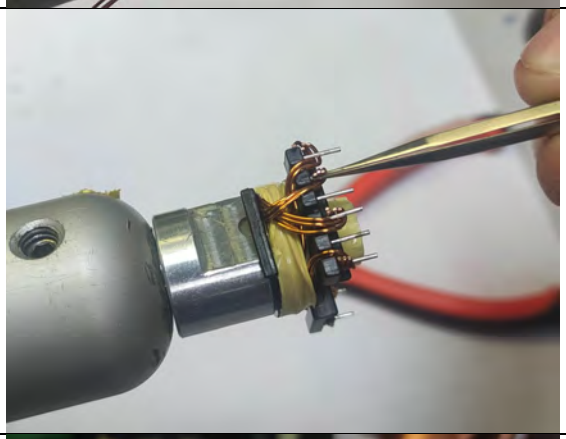
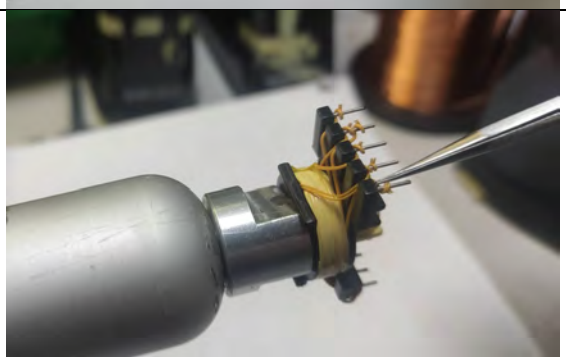
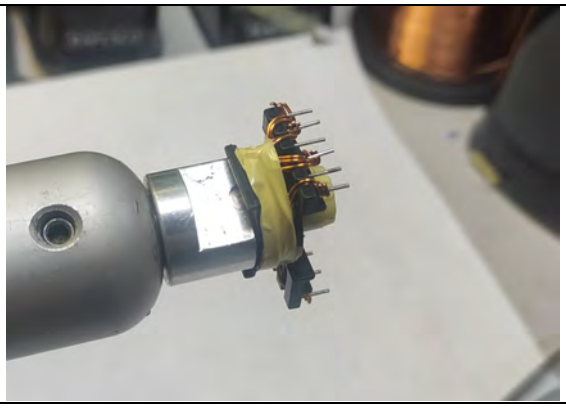
| | | Between Pins | Pins Shorted |
|---|---|---|---|
| Lpri [µH] | 186.4 | 9 - 11 | |
| LCV1 [µH] | 1.61 | 3 - 6 | |
| LCV2/CV3 [µH] | 8.5 | 1 - 3 | |
| L1aux [µH] | 10.3 | 7 - 8 | |
| Llkg1 [µH] | 7.5 | 9 - 11 | 1, 3, 5 and 6 |

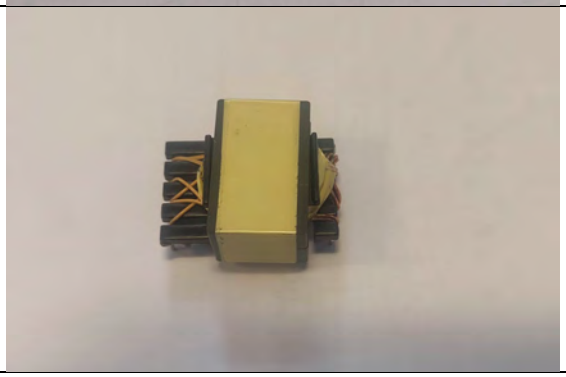
## 8.10 Winding Illustration

| | | |
|---|---|---|
| |  | Place the bobbin on the mandrel with the pin side to the right.<br>Winding direction is in the clockwise direction i.e. |
| **Wind 1**<br>**Primary 1**<br>**2 / 3 Primary** |  | Start at pin 11, wind 16 turns of 1 wire Item [4] in 2 layers with tight tension. Terminate at pin 10. |
| **Insulation layer** |  | Place 1 layers of tape Item [6] for insulation. |
| **Wind 2**<br>**Primary Bias** |  | Start at pin 8, wind 6 turns of 2 wire Item [5] in 1 layer with tight tension. Cut to leave about 5cm and tape to mandrel bobbin. |

| | | |
|---|---|---|
| **Insulation layer** |  | Place 1 layers of tape Item [6] for insulation. |
| **Wind 3**<br>**CV2/CV3 Winding** |  | Start at pin 1, wind 3 turns of 3 wire Item [3] in 1 layer with tight tension. Cut to leave about 5 cm and tape to mandrel bobbin |
| **Insulation layer** |  | Place 1 layers of tape Item [6] for insulation. |
| **Wind 4**<br>**CV1 Winding** |  | Start at pin 6, wind 2 turns of 4 wire Item [3] in 1 layer with tight tension. Cut to leave about 5 cm and tape to mandrel bobbin |

| | | |
|---|---|---|
| **Insulation layer** |  | Place 1 layers of tape Item [6] for insulation. |
| **Wind 5**<br>**Primary 2**<br>**1/3 Primary** |  | Start at pin 10, wind 8 turns of 1 wire Item [4] in 1 layer with tight tension. Terminate at pin 9. |
| **Insulation layer** |  | Place 1 layers of tape Item [6] for insulation. |

| | | |
|---|---|---|
| **Termination** |  | Terminate the CV1 windings at pin number 3. |
| **Termination** |  | Terminate the CV2/CV3 winding at pin number 5. |
| **Termination** |  | Terminate primary bias winding at pin number 7. |
| **Insulation** |  | Place 2 layers of tape Item [6] for insulation. |

| | | |
|---|---|---|
| **Insert core** |  | Gap core to achieve 188µH. Tape core tightly together. |
| |  | Cover with 1 layer of tape Item [8].<br><br>Varnish dip and cure Item [11] |

## *8.11 CMC Specification*

### 8.11.1 Electrical Diagram

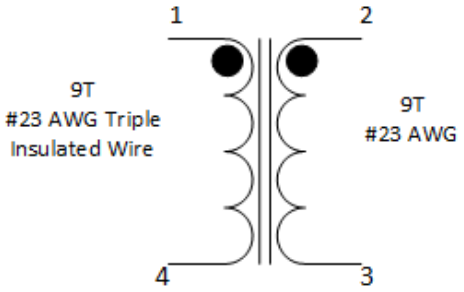



**Figure 14 –** Inductor Electrical Diagram.

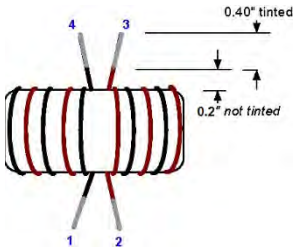
### 8.11.2 Electrical Specifications

| | | |
|---|---|---|
| **Inductance** | Pins 1-4 measured at 100 kHz, 0.4 RMS. | 200 µH ±10% |
| **Primary Leakage Inductance** | Pins 1-4, with 2-3 shorted. | 1 µH |

### 8.11.3 List of Materials

| Item | Description |
|---|---|
| **[1]** | Core: GL50 T 12X6X4-C, PI Part # 32-00315-00 BIPOLAR ELECTRONIC CO., LTD. |
| **[2]** | Magnet Wire: #23 AWG. |
| **[3]** | Triple Insulated wire #23 AWG. |

### 8.11.4 Illustration




Note: Add Teflon sleeving for terminations.

## *8.12 CMC Winding Illustration*

| | | |
|---|---|---|
| |  | Start as pin 1 for Item [3] and pin 2 for Item [2].<br><br>Wind together 9 turns on core Item [1].<br><br>Mark end of Item [3] as pin 4 and end of Item [2] as pin 3. |

# 9 Performance

## *9.1 Current Limit Characteristic Curve*

Current Limit Characteristic curve is verified in specific load points with calculating primary peak current at measured switching frequency points.

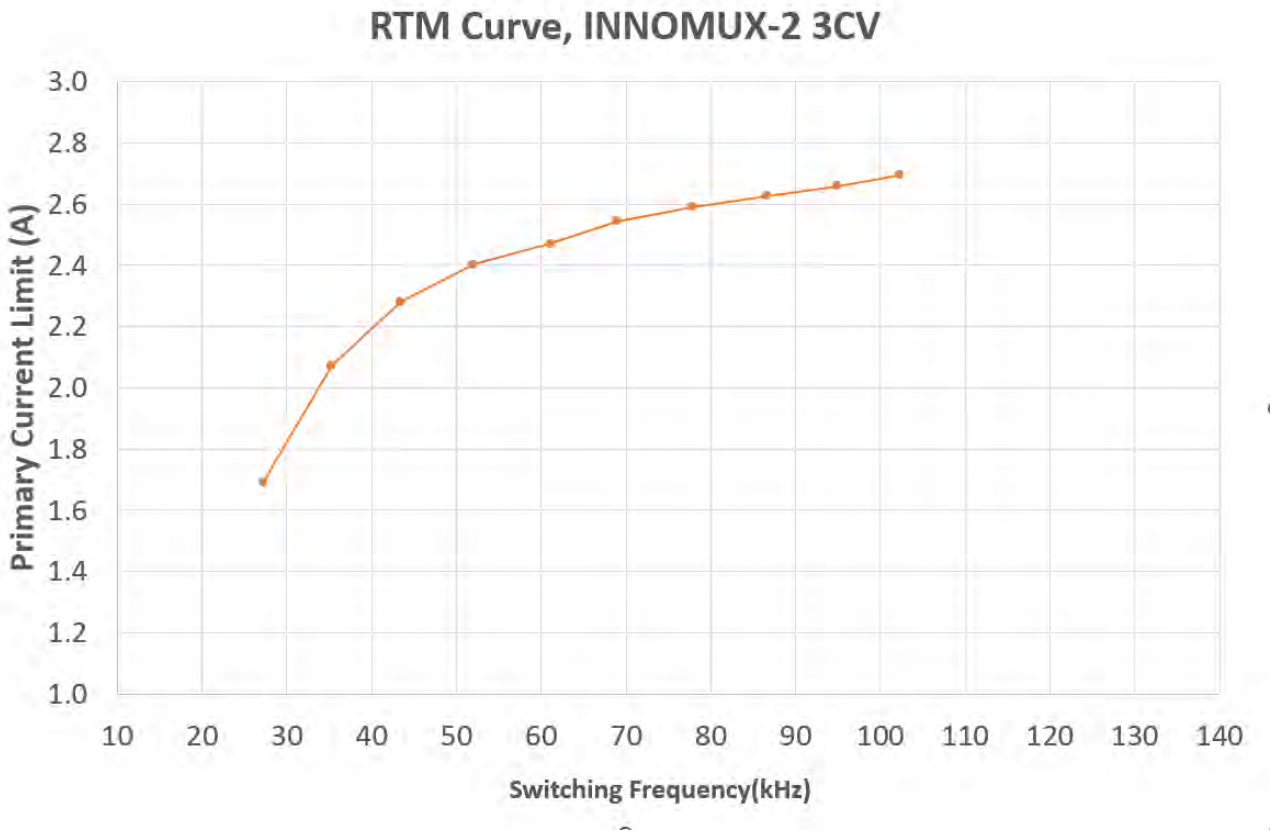



**Figure 15 –** Primary Current (A) vs. SW frequency at Room Temperature.

## 9.2 Full Load Efficiency vs. Line Input Voltage

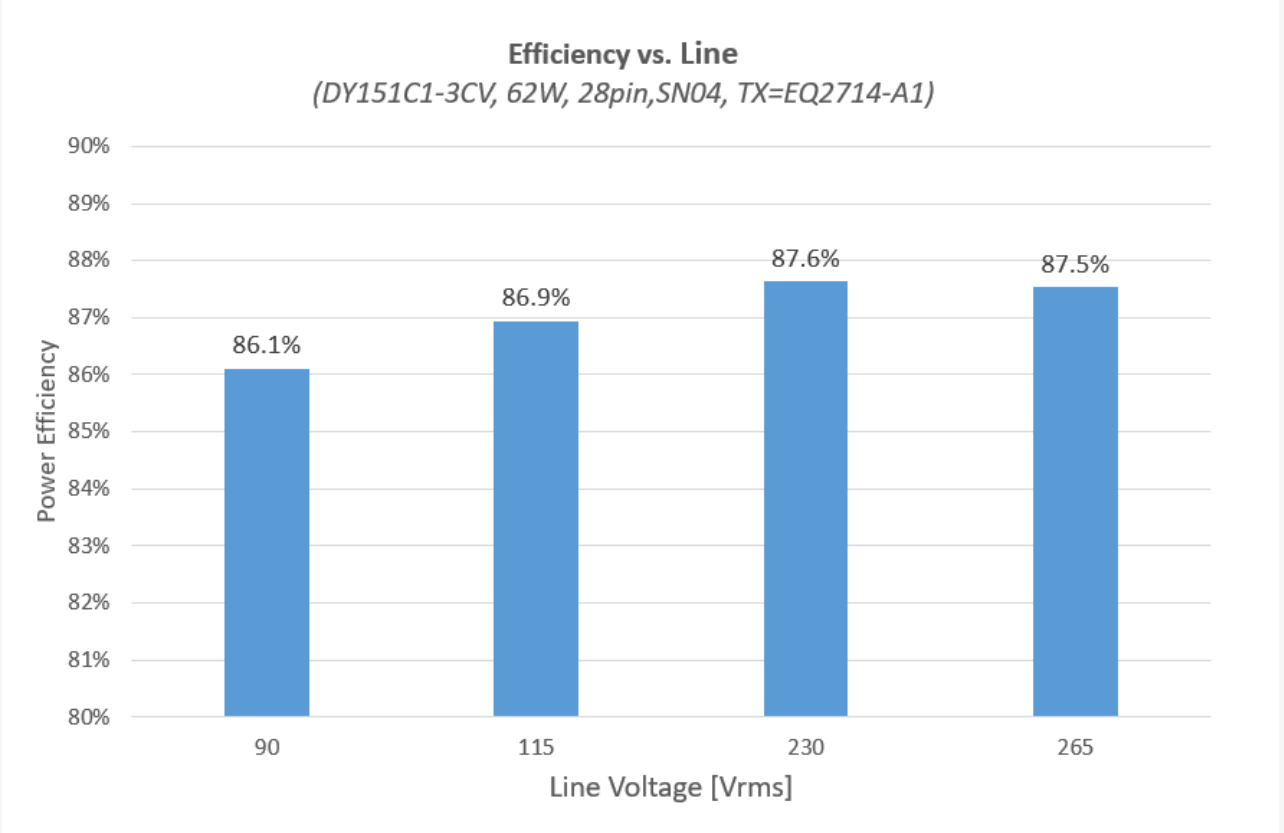



**Figure 16 –** Full Power Efficiency vs. Line Voltage at Room Temperature.

## *9.3 Efficiency vs. Load*

The efficiency vs. load measurements is shown below. These were obtained for all combinations of:

- All (nominal) line voltages (90 V, 115 V, 230 V, 265 V)
- CV1, CV2 and CV3 have total over thousand test points (load combinations) for the efficiency result.

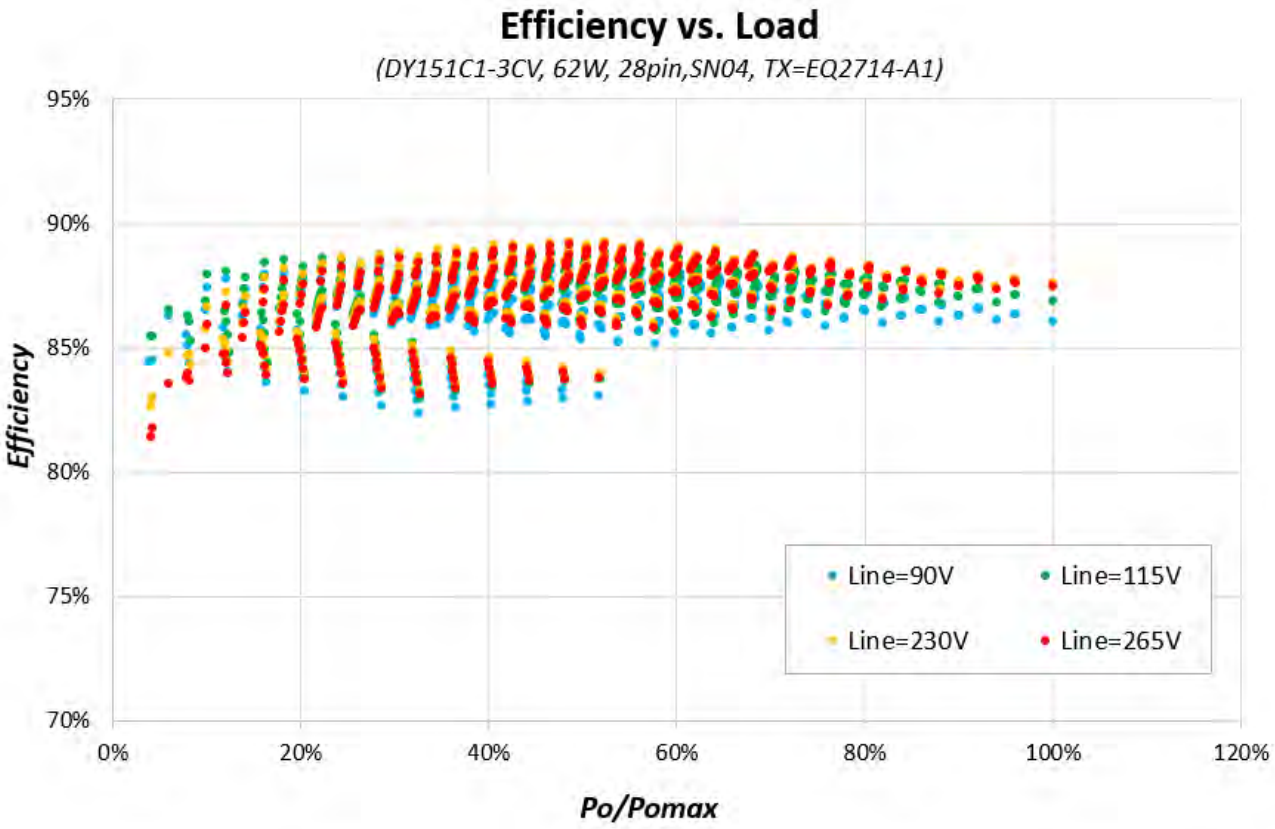



**Figure 17 –** Efficiency vs. Load for all line and $V_{LED}$ variations, Room Temperature.

## *9.4 Output Load Regulation*

The output-voltage regulation error was measured for all CV outputs

- The current at CV1 output was increased from 0% to 100% of its rating in 8 steps
- The current at CV2 output was increased from 0% to 100% of its rating in 5 steps
- The current at CV3 output was increased from 12% to 100% of its rating in 7 steps
- all (nominal) line voltages

The load regulation errors for the CV outputs are shown below.

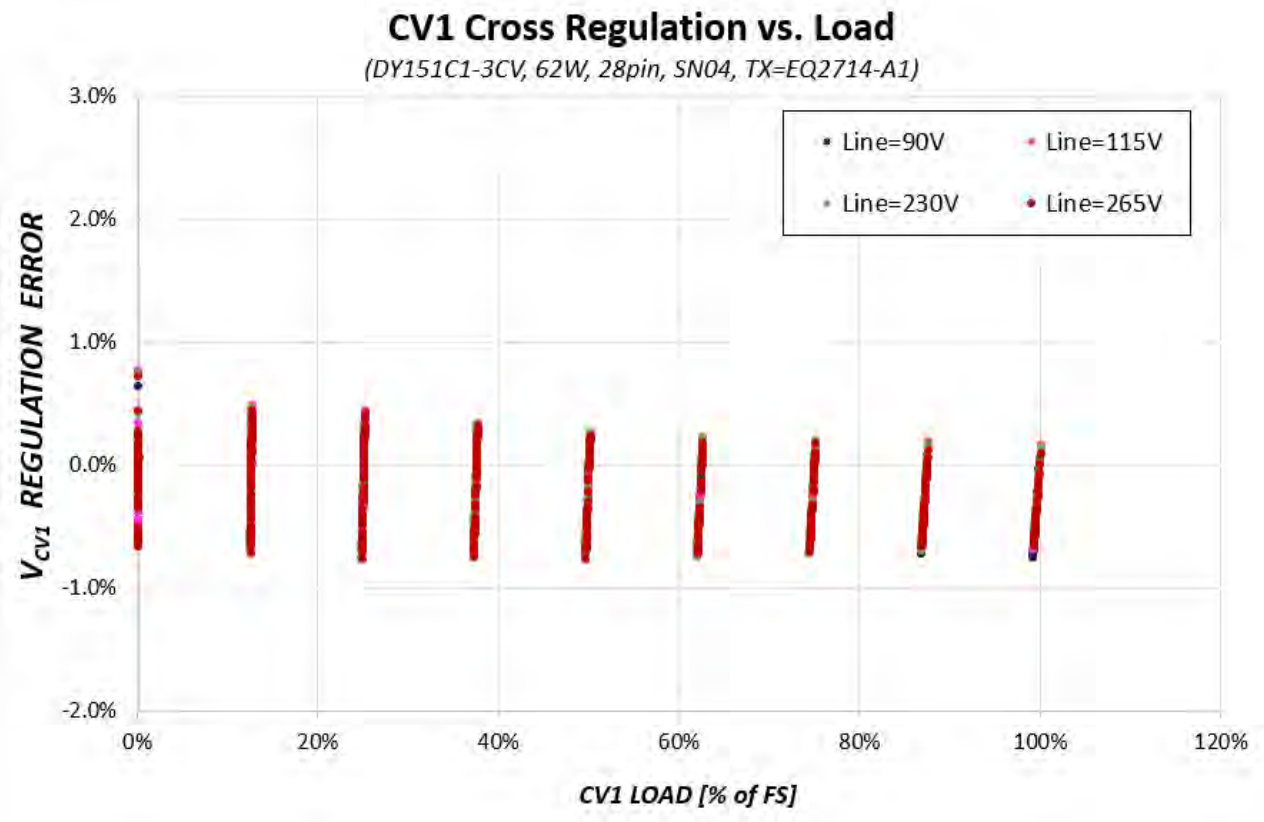



**Figure 18 –** VCV1 Output Error vs. Percentage Load, at Room Temperature.

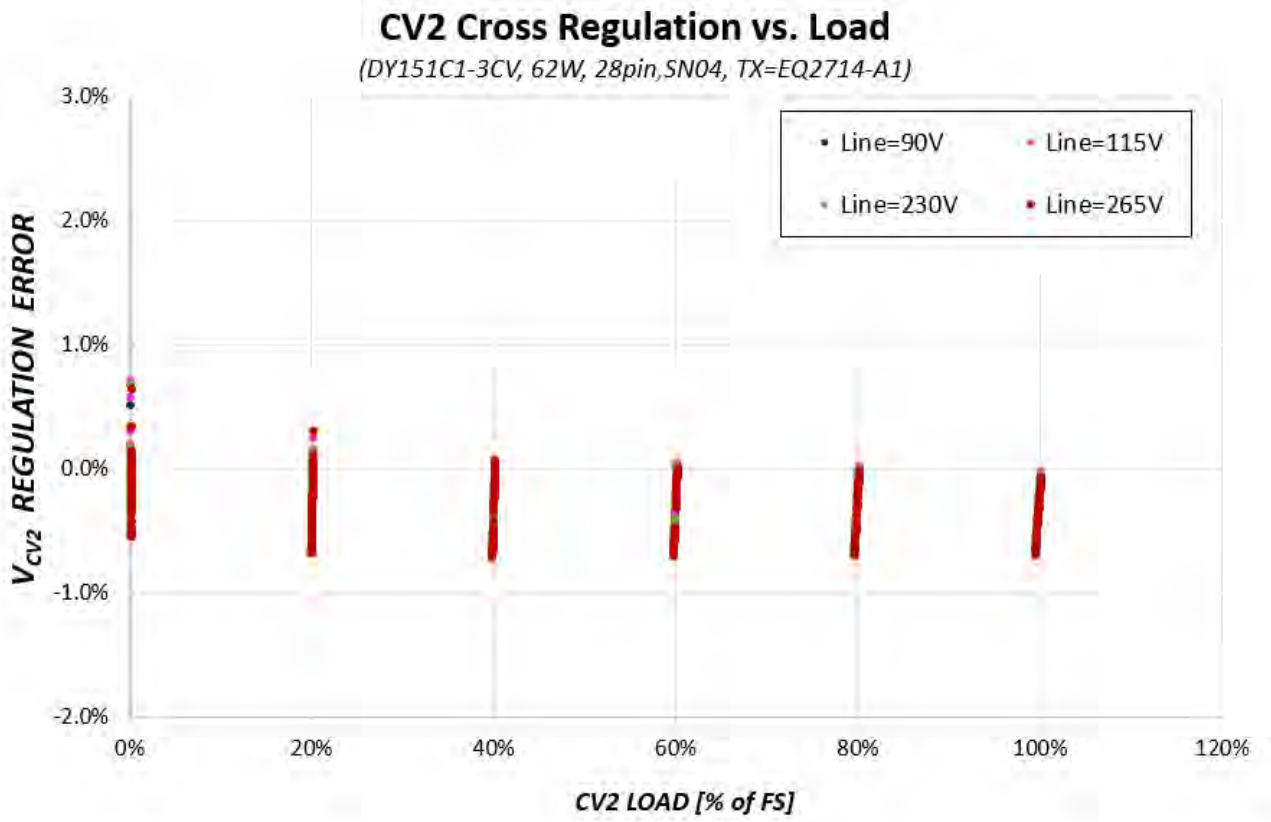



**Figure 19 –** VCV2 Output Error vs. Percentage Load, at Room Temperature.

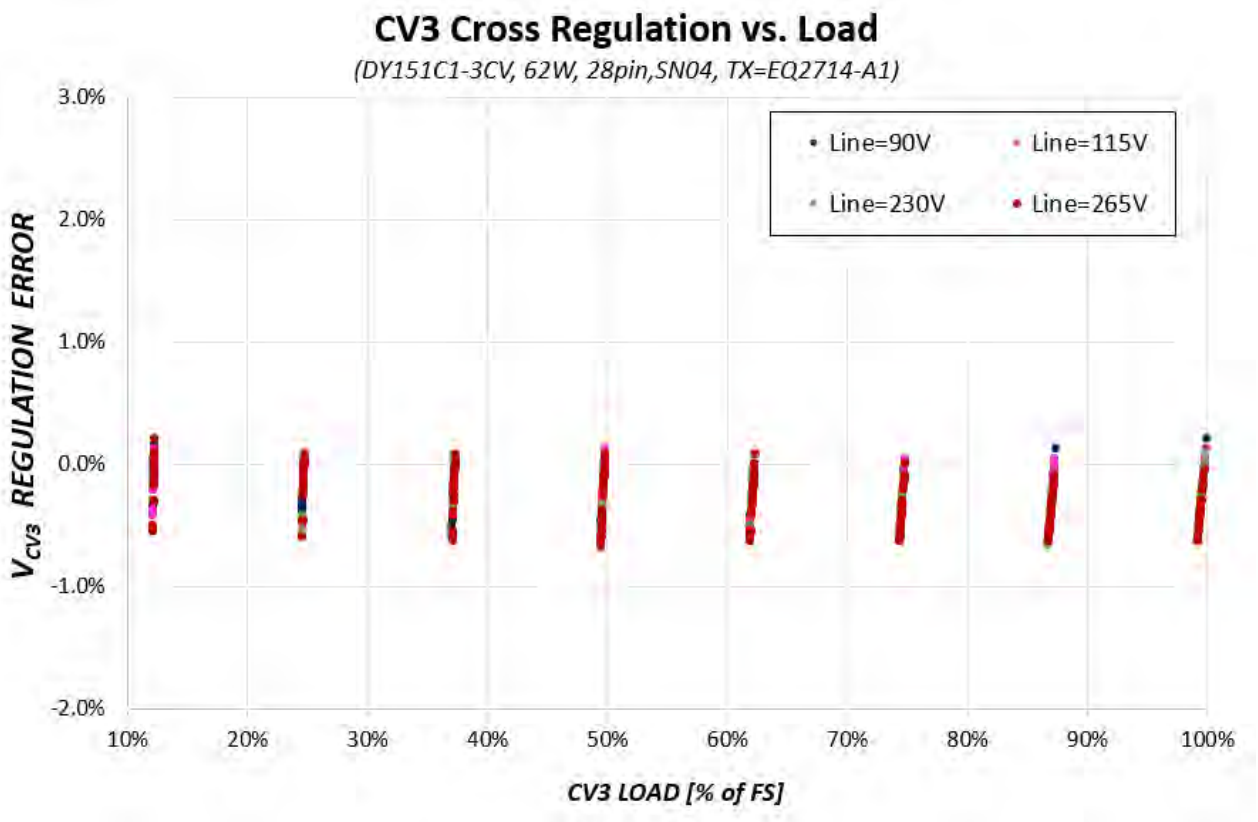



**Figure 20 –** VCV3 Output Error vs. Percentage Load, at Room Temperature.

## *9.5 Standby Input Power*

The converter standby power was measured for all (nominal) line voltages; with CV2 and CV3 no-load and for 0 mW ~ 250 mW load on the CV1 output. The results are shown in the Figure below.

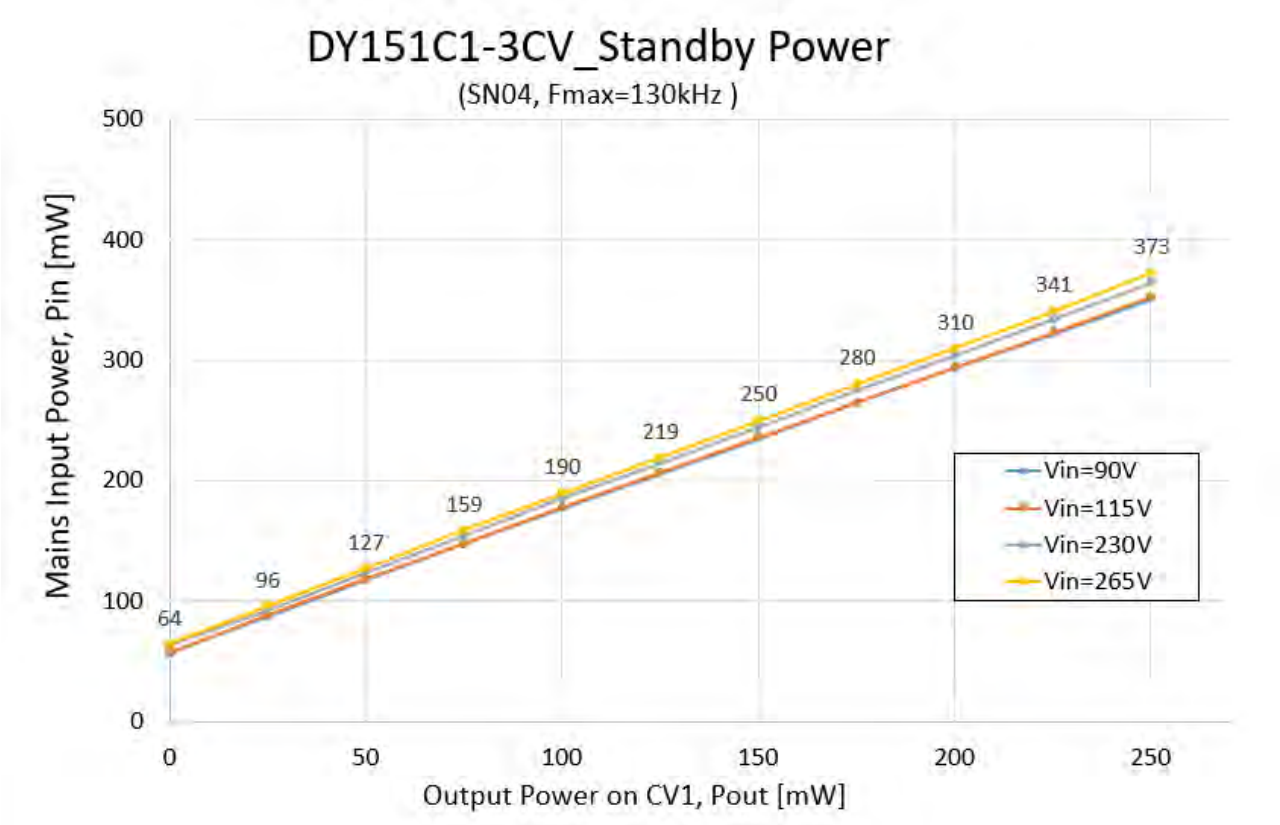



**Figure 21 –** Standby Power Consumption vs. Line Voltage, Room Temperature.

## *9.6 CV Load Transient Response*

CV output voltages are measured at load transient from 0.05 A to 4 A for CV1, 0 A to 1 A for CV2, 0 A to 1.25 A for CV3. Measurement has been done at 90 VAC and 265 VAC with full load on other channels while the one supplied with load step and no-load on other channels when the one supplied with load step. In all cases less than 5% voltage drop observed on CV outputs.

Bandwidth of the channels are 20 MHz.

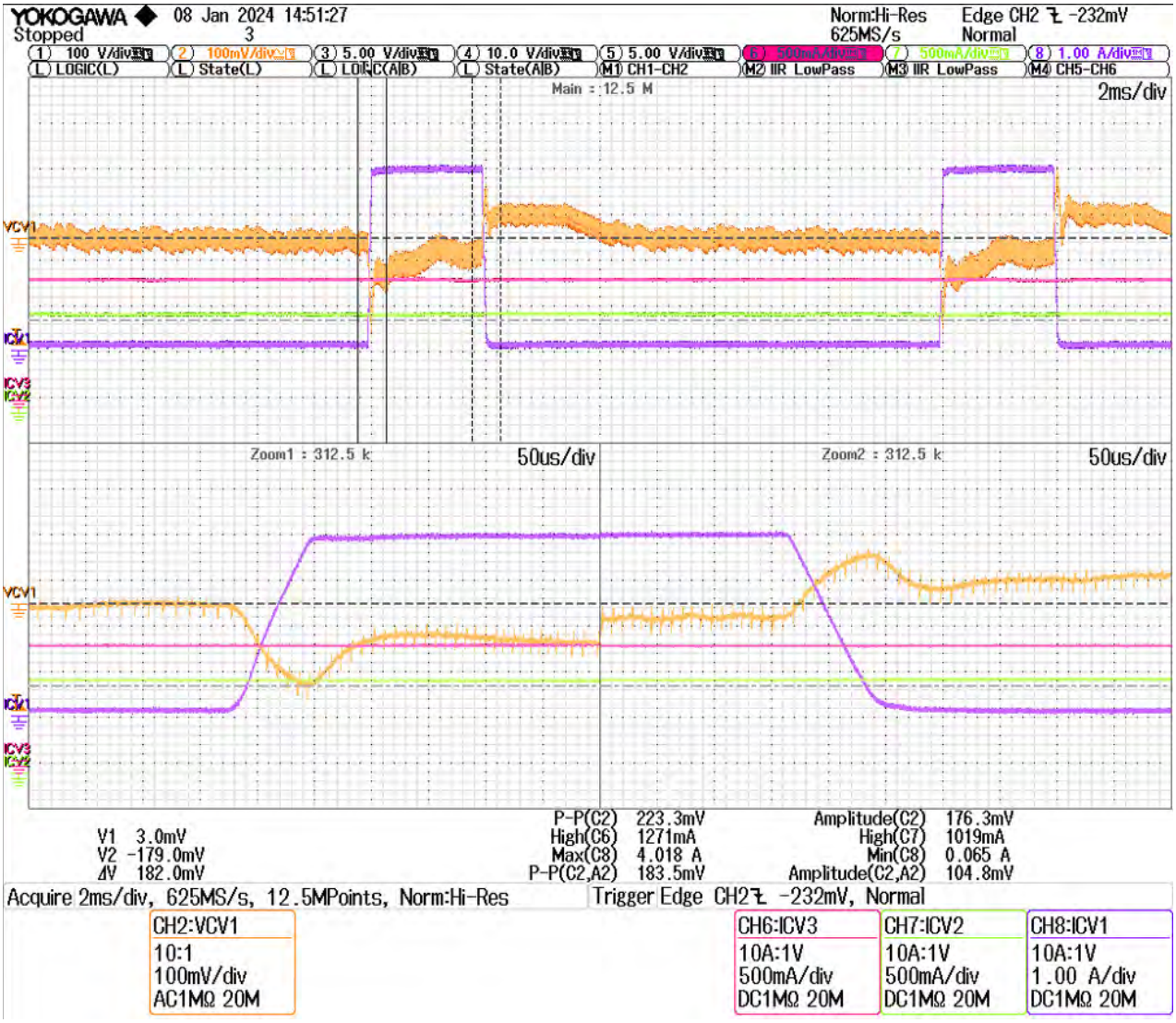



**Figure 22 –** CV1 (5 V) Output - Load Transient Under Full Load on CV2 and CV3 at 90 VAC.
$I_{CV1}$ = 0.05 A – 4 A; Undershoot 223 mV, 4.46%; Overshoot = 184 mV, 3.68%
CH2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

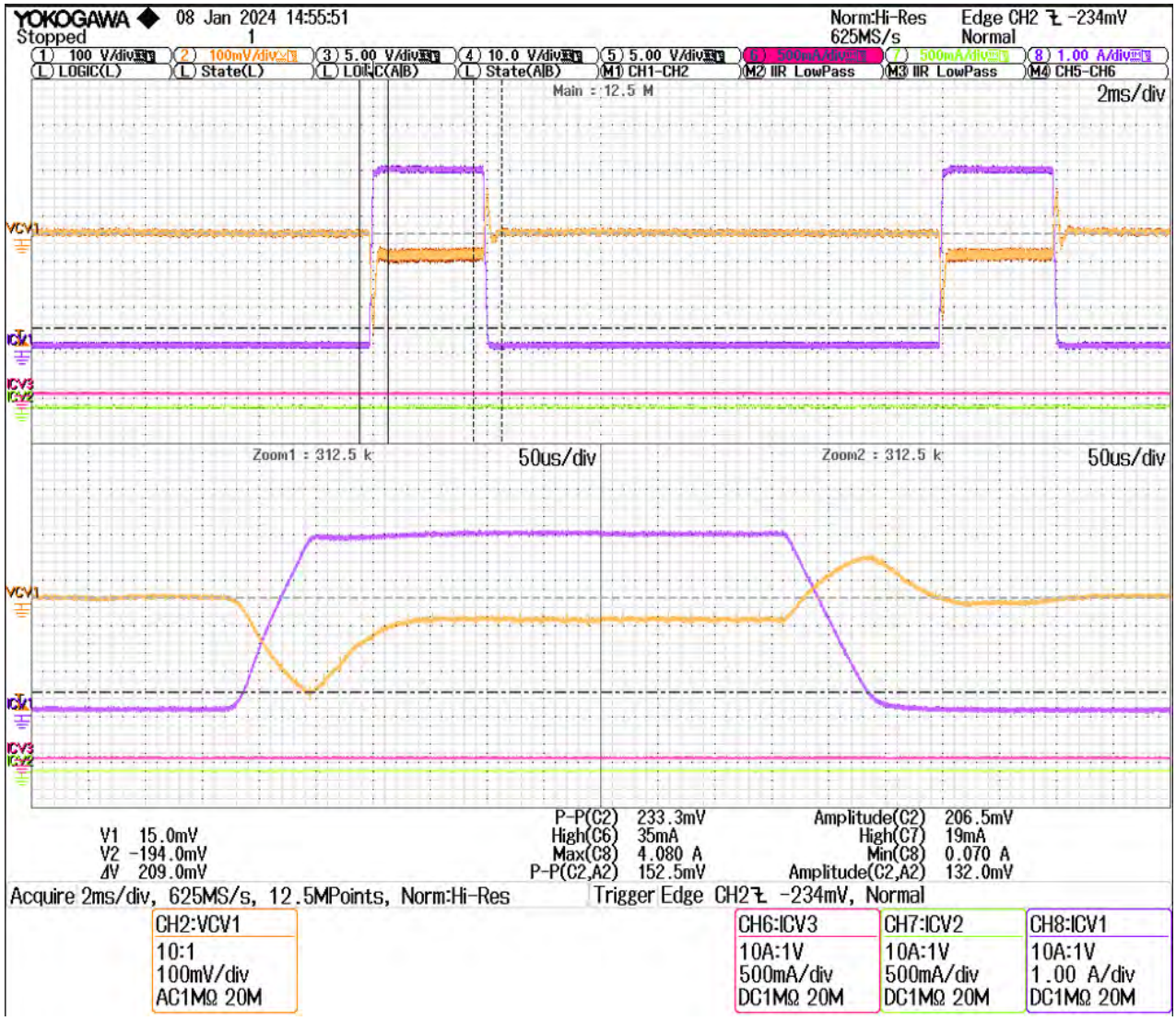



**Figure 23 –** CV1 (5 V) Output - Load Transient Under No-Load on CV2 and CV3 at 90 VAC.
$I_{CV1}$ = 0.05 A – 4 A; Undershoot 233 mV, 4.66%; Overshoot = 152 mV, 3.04%
CH2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$


**Figure 24 –** CV1 (5 V) Output - Load Transient Under Full Load on CV2 and CV3 at 265 VAC.
$I_{CV1}$ = 0.05 A - 4 A; Undershoot 222 mV, 4.44%; Overshoot = 230 mV, 4.6%
CH2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

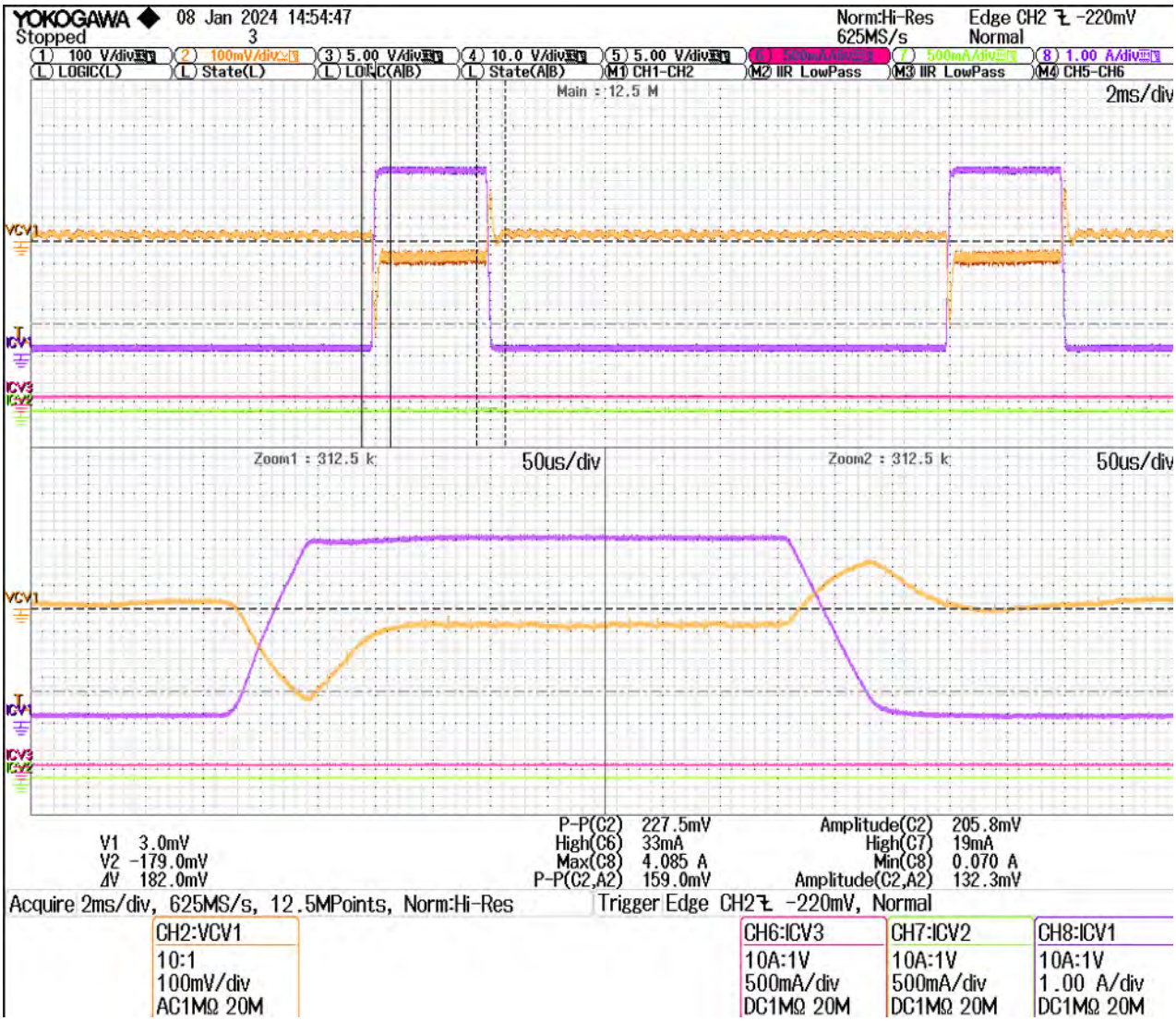



**Figure 25 –** CV1 (5 V) Output - Load Transient Under No-Load on CV2 and CV3 at 265 VAC.
$I_{CV1}$ = 0.05 A - 4 A; Undershoot 228 mV, 4.56%; Overshoot = 159 mV, 3.18%
CH2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$


**Figure 26 –** CV2 (12 V) Output - Load Transient Under Full Load on CV1 and CV3 at 90 VAC.
$I_{CV2}$ = 0 A – 1 A; Undershoot 214 mV, 1.78%; Overshoot = 185 mV, 1.54%
CH2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$


**Figure 27 –** CV2 (12 V) Output - Load Transient Under No-Load on CV1 and CV3 at 90 VAC.
$I_{CV2}$ = 0 A - 1 A; Undershoot 175 mV, 1.46%; Overshoot = 144mV, 1.2%
CH2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

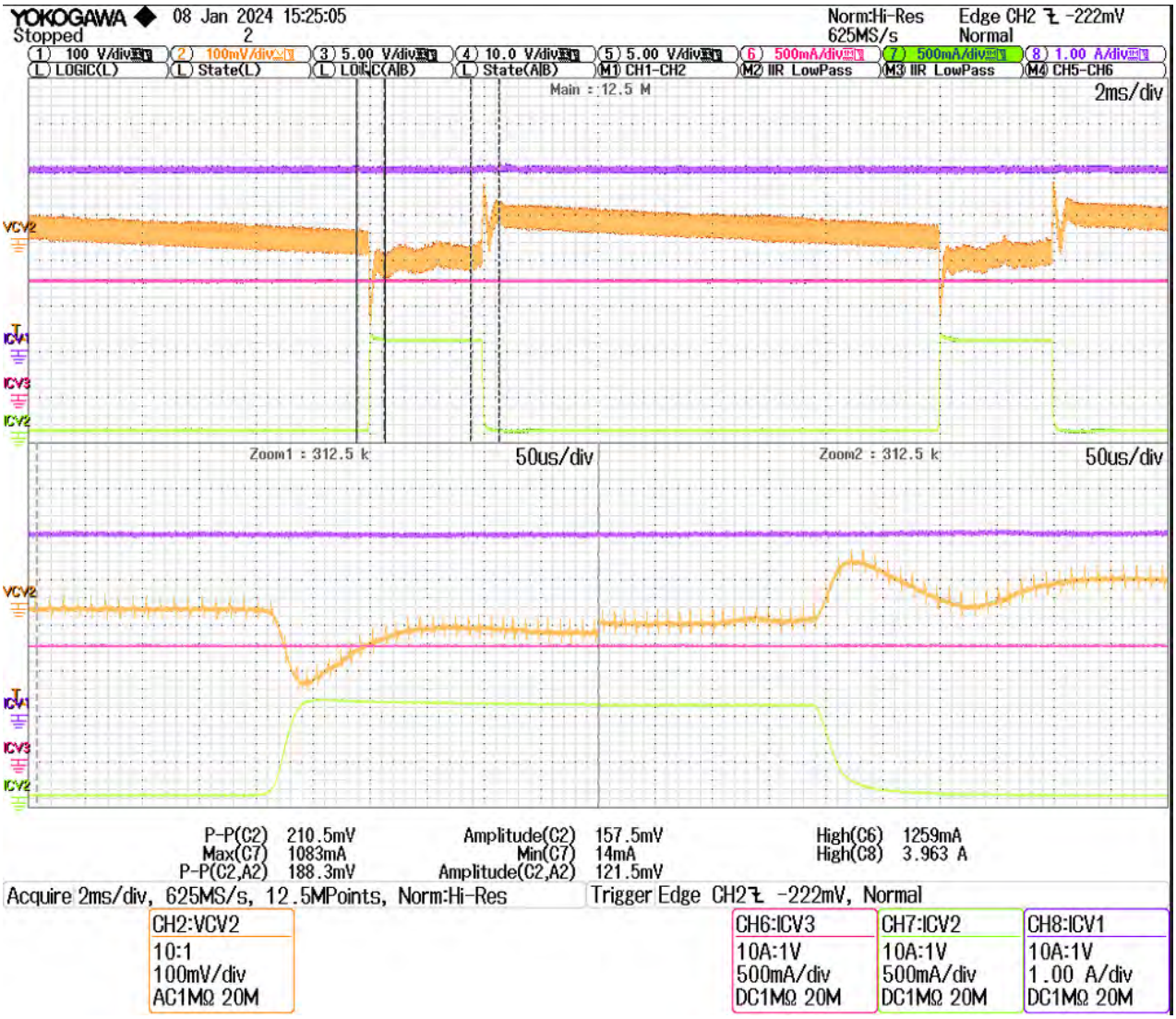



**Figure 28 –** CV2 (12 V) Output - Load Transient Under Full Load on CV1 and CV3 at 265 VAC.
$I_{CV2}$ = 0 A - 1 A; Undershoot 211 mV, 1.76%; Overshoot = 188 mV, 1.57%
CH2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

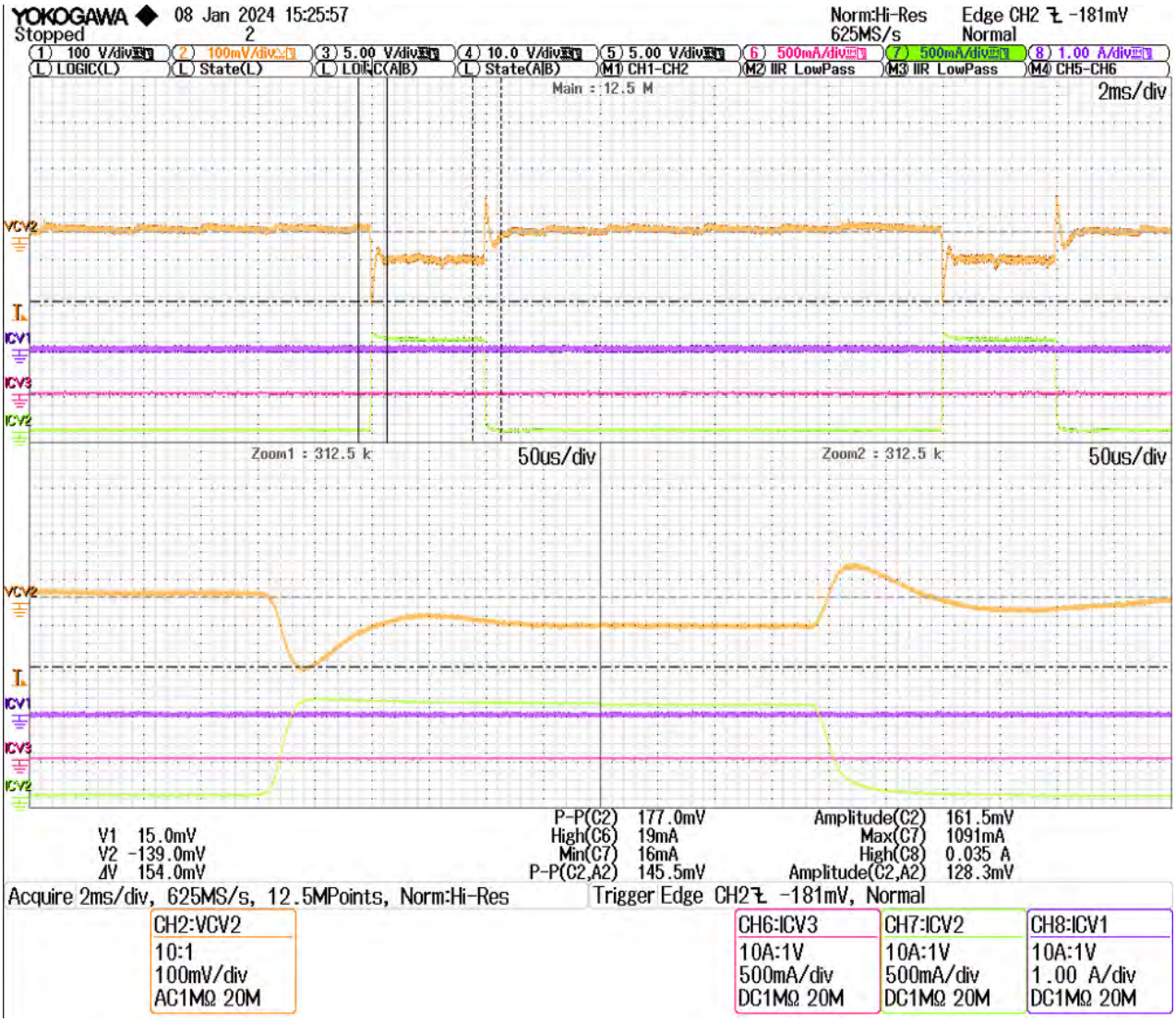



**Figure 29 –** CV2 (12 V) Output - Load Transient Under No-Load on CV1 and CV3 at 265 VAC.
$I_{CV2}$ = 0 A - 1 A; Undershoot 177 mV, 1.47%; Overshoot = 146 mV, 1.22%
CH2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$


**Figure 30 –** CV3 (24 V) Output - Load Transient Under Full Load on CV1 and CV2 at 90 VAC.
$I_{CV2}$=0.1A - 1.25 A; Undershoot 839 mV, 3.49%; Overshoot = 514 mV, 2.14%
CH2: $V_{CV3}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

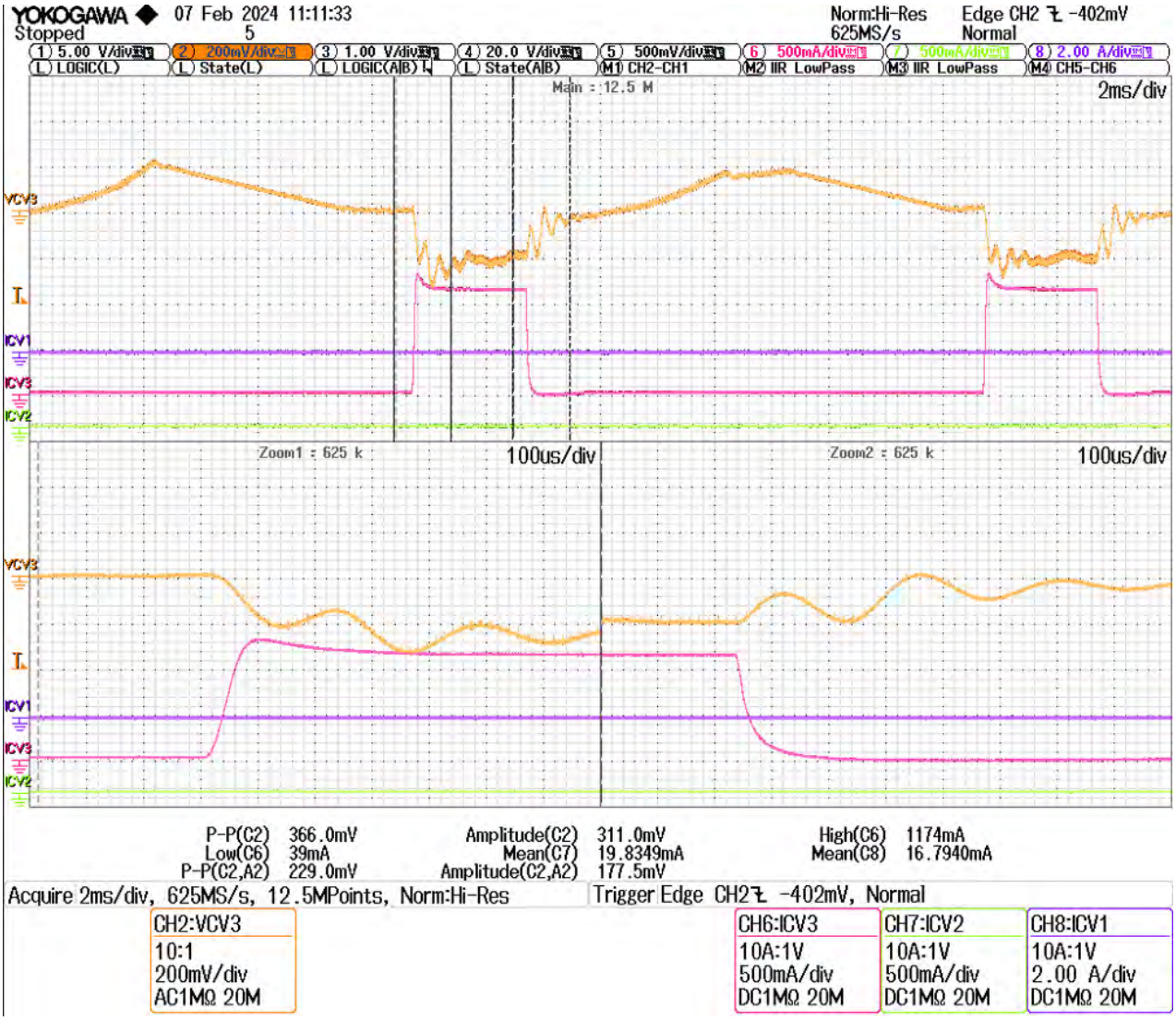



**Figure 31 –** CV3 (24 V) Output - Load Transient Under No-Load on CV1 and CV2 at 90 VAC.
$I_{CV2}$ = 0.1 A - 1.25 A; Undershoot 366 mV, 1.53%; Overshoot = 229 mV, 0.96%
CH2: $V_{CV3}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

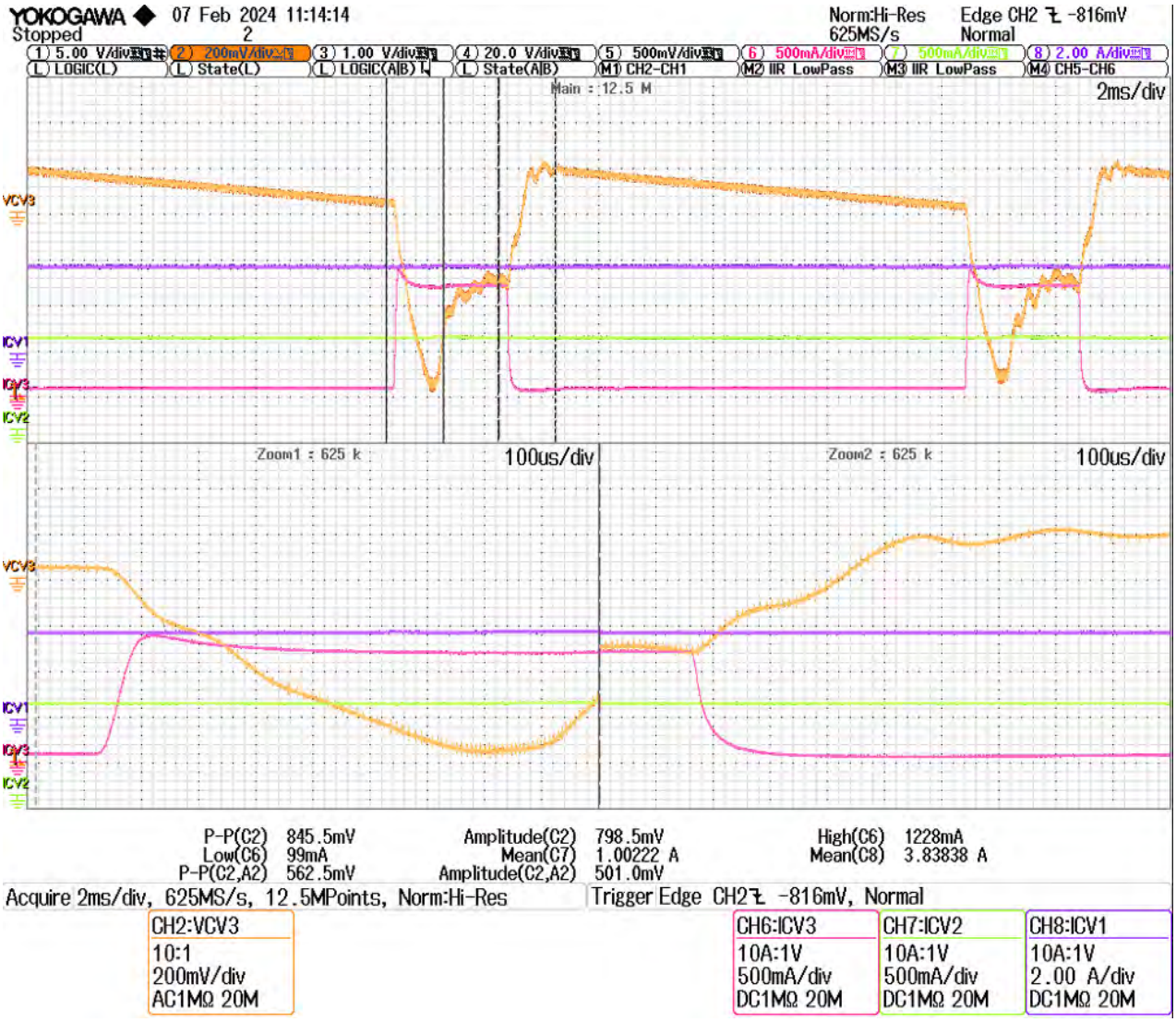



**Figure 32 –** CV3 (24 V) Output - Load Transient Under Full Load on CV1 and CV2 at 265 VAC.
$I_{CV2}$ = 0.1 A - 1.25 A; Undershoot 846 mV, 3.5%; Overshoot = 563 mV, 2.35%
CH2: $V_{CV3}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$ , CH8: $I_{CV1}$

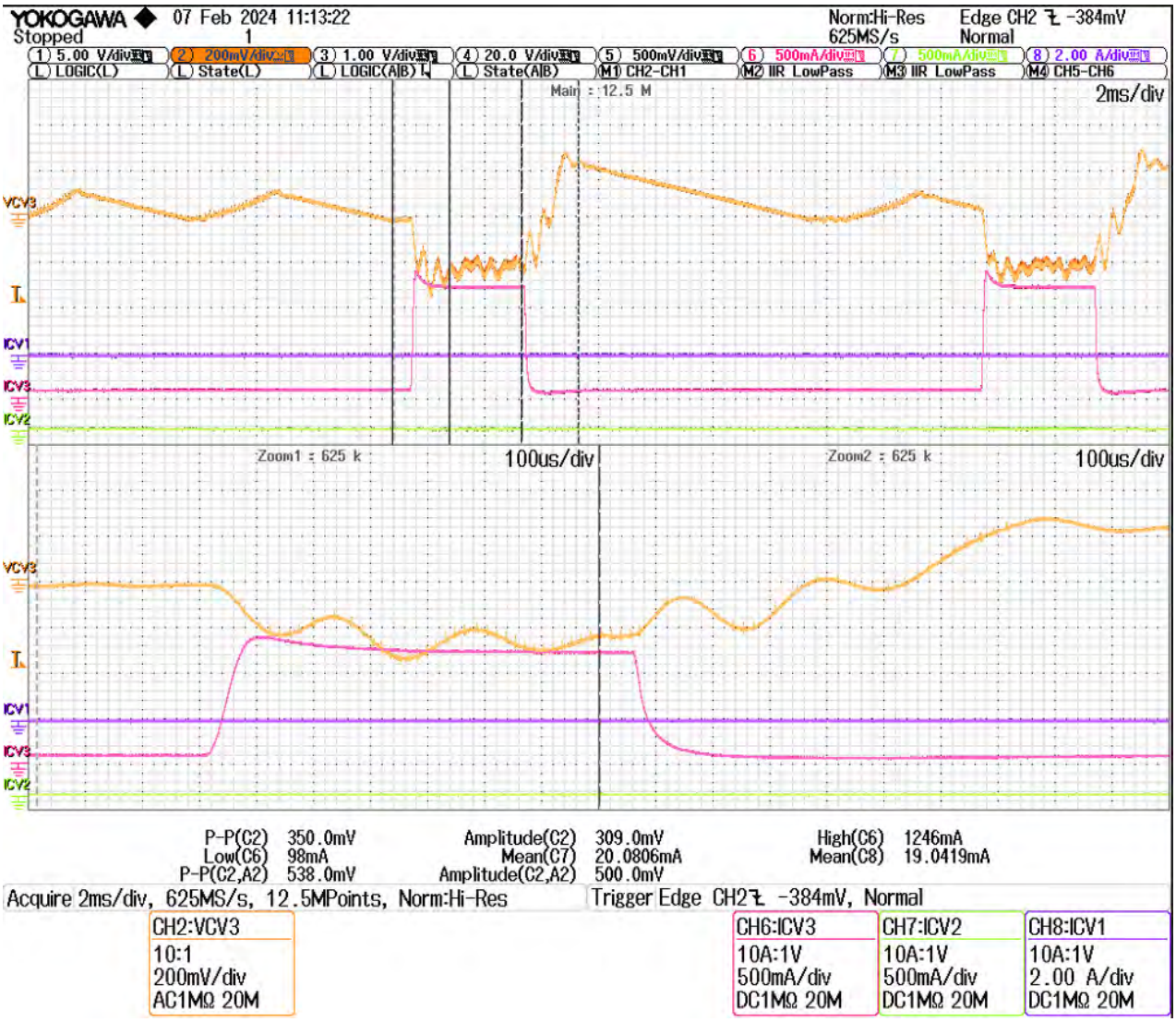



**Figure 33 –** CV3 (24 V) Output - Load Transient Under No-Load on CV1 and CV2 at 265 VAC.
$I_{CV2}$ = 0.1 A - 1.25 A; Undershoot 350 mV, 1.46%; Overshoot = 538 mV, 2.24%
CH2: $V_{CV3}$ Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, CH8: $I_{CV1}$

## *9.7 Switching Waveforms*

### 9.7.1 Primary Switch Maximum Voltage

Voltages on the primary FET have been measured at 265 VAC and 90 VAC under full load condition. Channel bandwidth is 200 MHz.

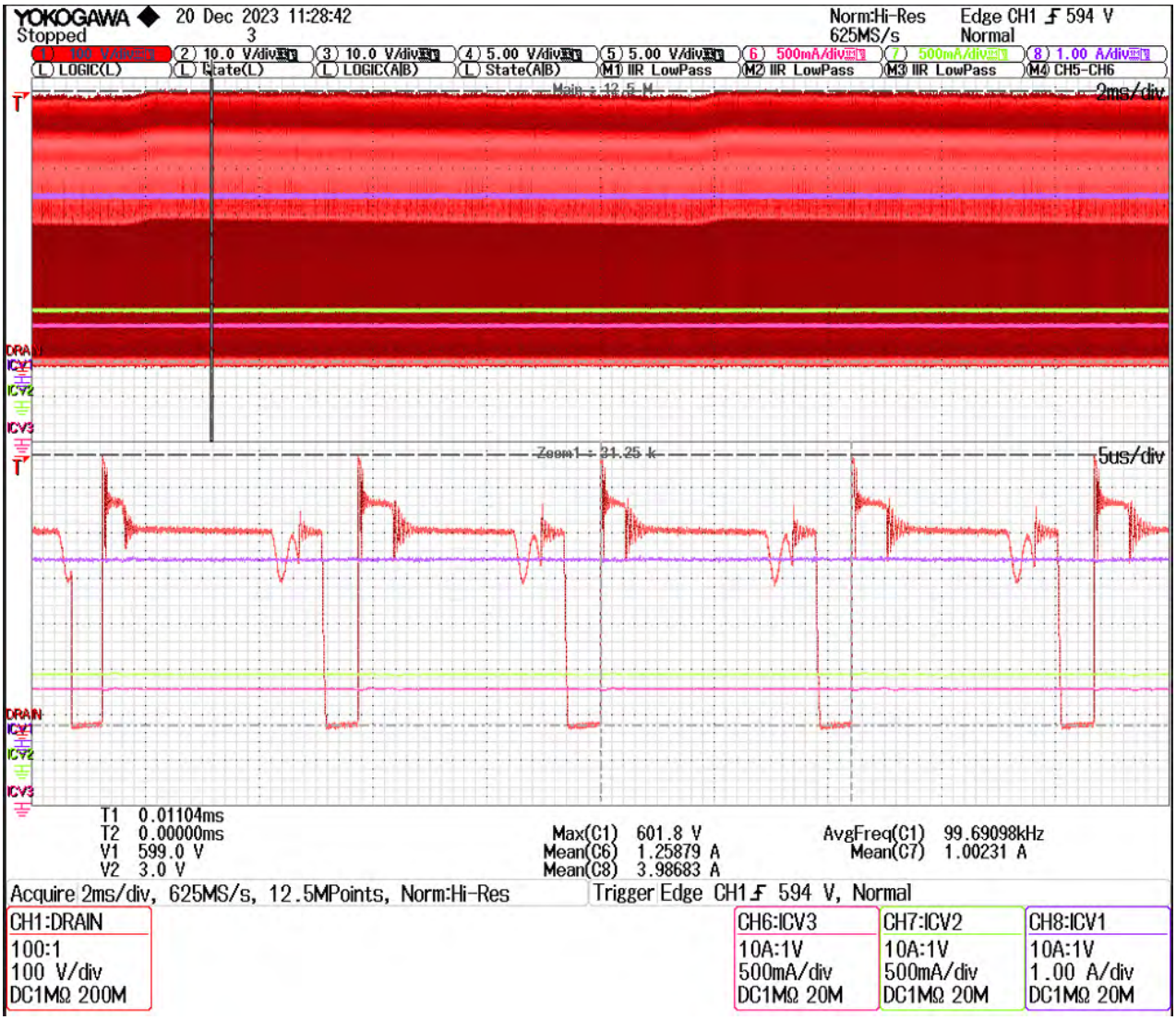



**Figure 34 –** Primary Switch Voltage Under Full Load at 265 VAC.

CH1: $V_{DRAIN}$, CH6: $I_{CV3}$, CH7: $I_{CV2}$, CH8: $I_{CV1}$

Maximum D-S voltage across the primary switch is 602 V.


**Figure 35 –** Primary Switch Voltage Under Full Load at 90 VAC.

CH1: $V_{DRAIN}$, CH6: $I_{CV3}$, CH7: $I_{CV2}$, CH8: $I_{CV1}$

Maximum D-S voltage across the primary switch is 383 V.

### 9.7.2 Primary Switching Frequency

The primary switching frequency of the converter varies depending on line and load conditions. It was measured under full load at minimum line input of 90 VAC. The maximum switching frequency occurs at the minimum DC input (115 kHz).CV1 channel has 4 A, CV2 has 1 A, CV3 has 1.25 A load currents.

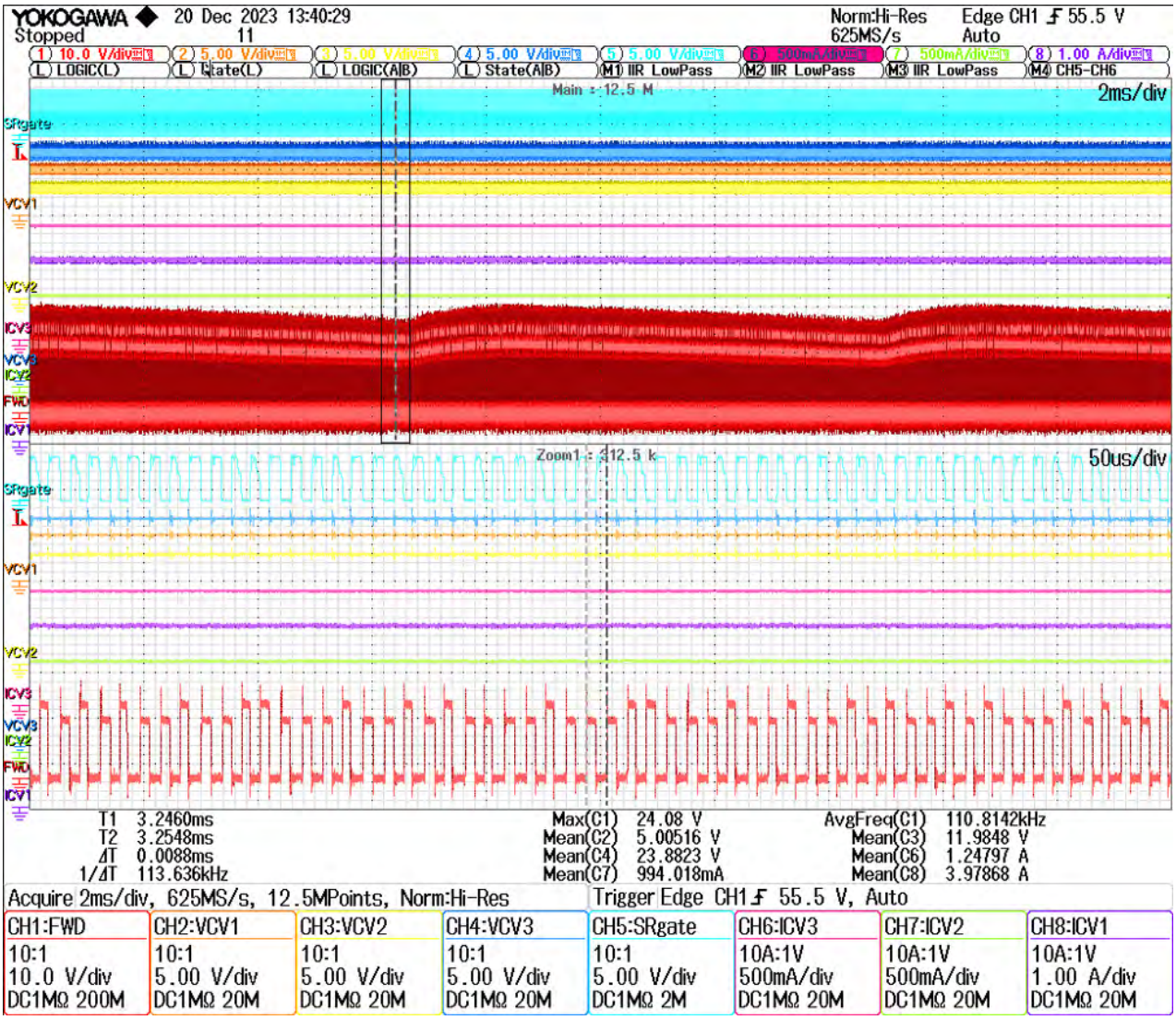



**Figure 36 –** Maximum Primary Switching Frequency (115 kHz).

### 9.7.3 Transformer Current Waveforms

| | |
|---|---|
| CH4 | ICV1_TX |
| CH5 | ICV2_TX |
| CH6 | ICV3_TX |
| CH7 | IPR_SW |
| CH8 | ISR |

Scope Channel Allocation (This Section).

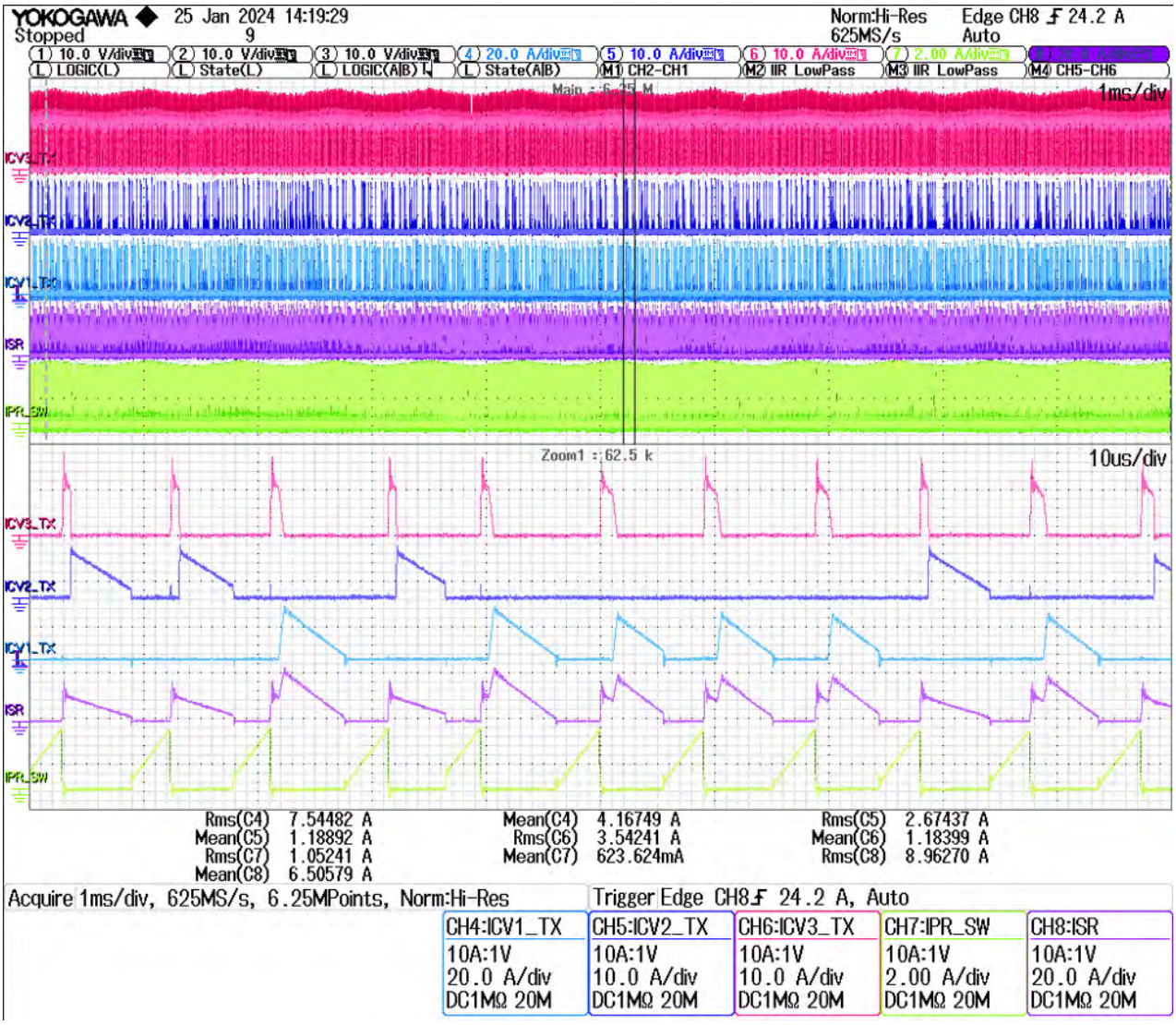



**Figure 37 –** Transformer Winding Currents at Minimum Input Voltage.

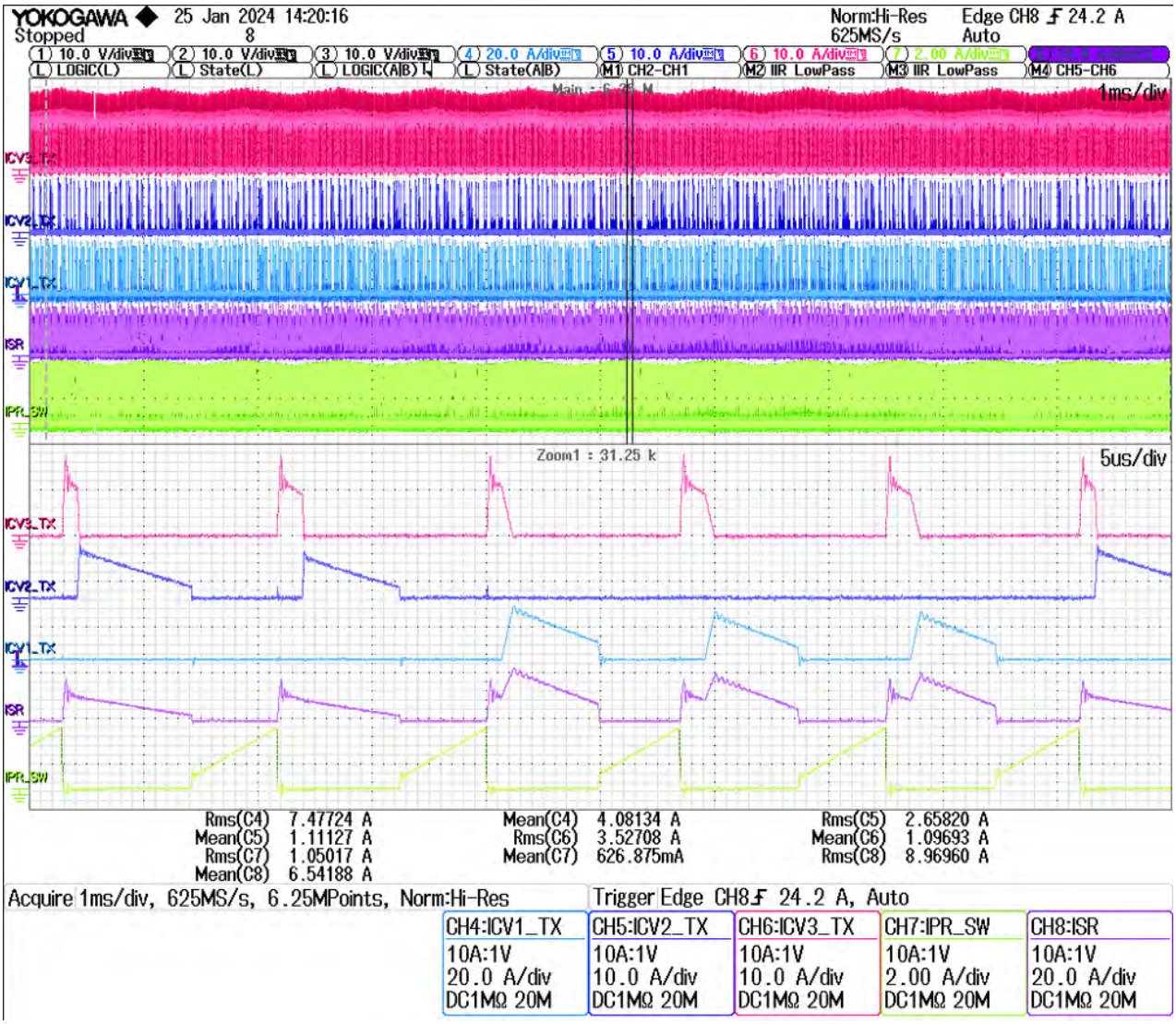



**Figure 38 –** Transformer Currents – Detailed View.

## 9.8 Start-Up

| | |
|---|---|
| CH2 | VCV1 |
| CH3 | VCV2 |
| CH4 | VCV3 |
| CH5 | BPS voltage |
| CH6 | ICV3 |
| CH7 | ICV2 |
| CH8 | ICV1 |

Scope Channel Allocation (This Section).

### 9.8.1 Full Load Start-up

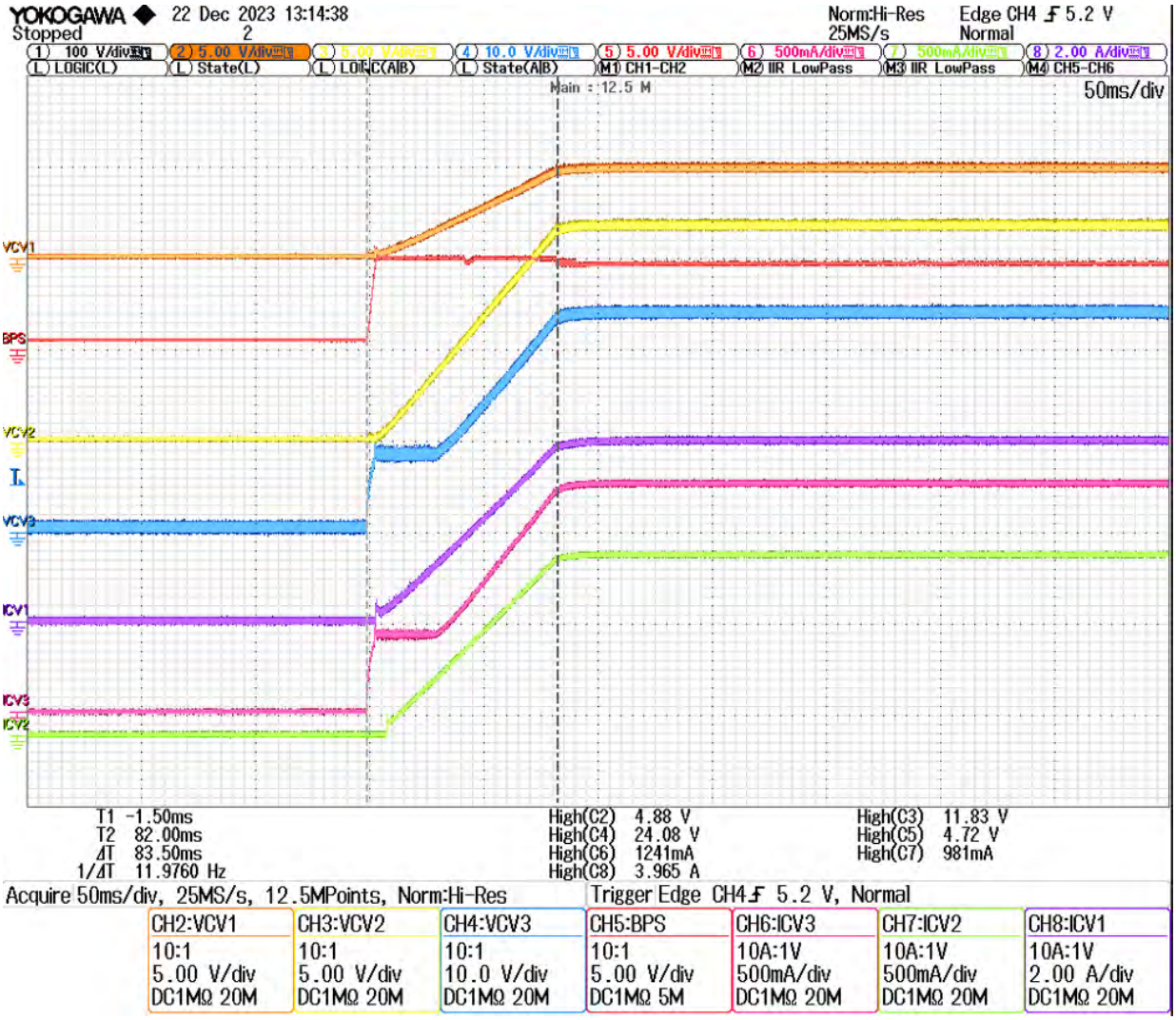



**Figure 39 –** Full Load Start-up. Line Input 90 VAC.

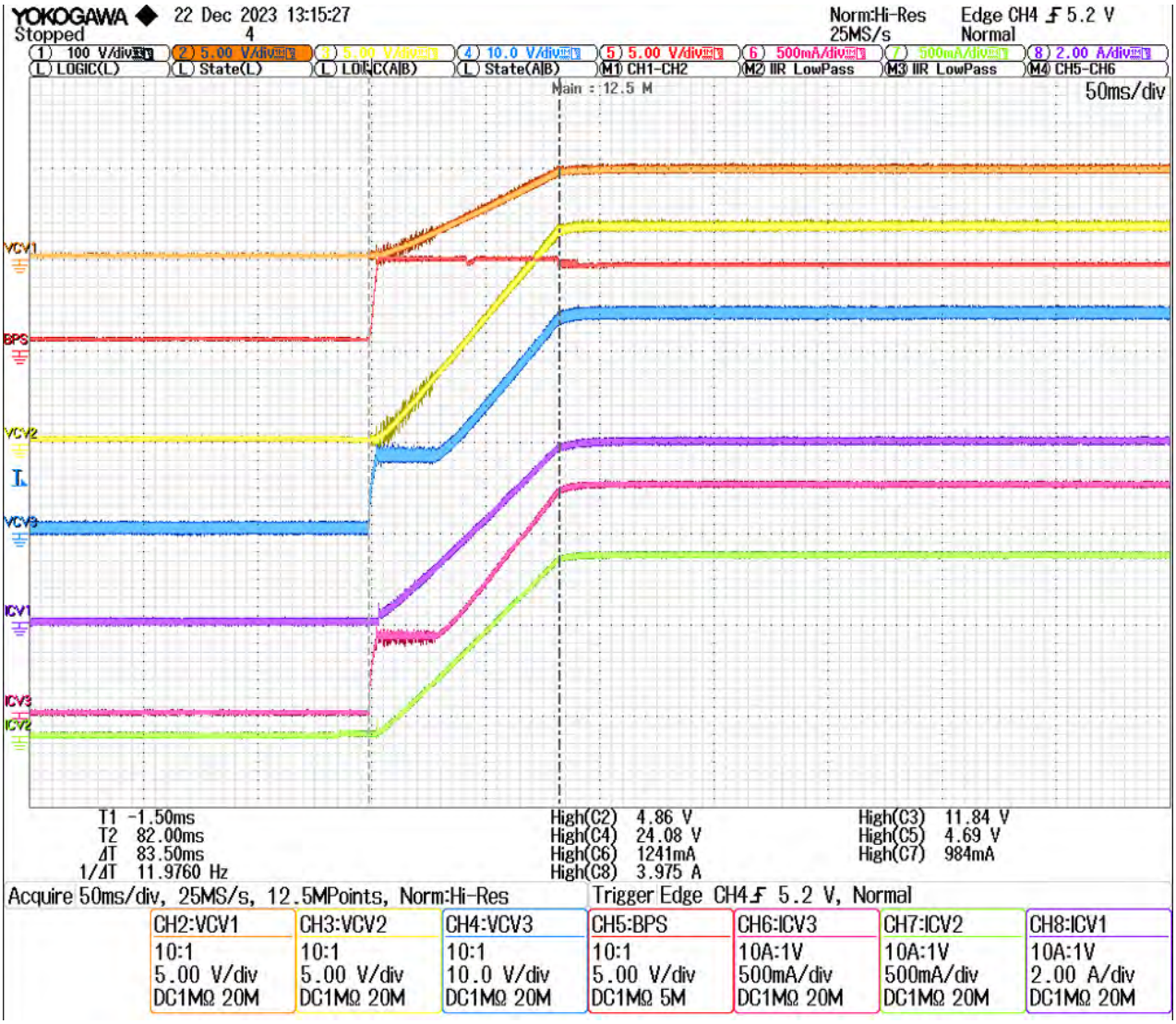



**Figure 40 –** Full Load Start-up. Line Input 265 VAC.

### 9.8.2 No-Load Start-up

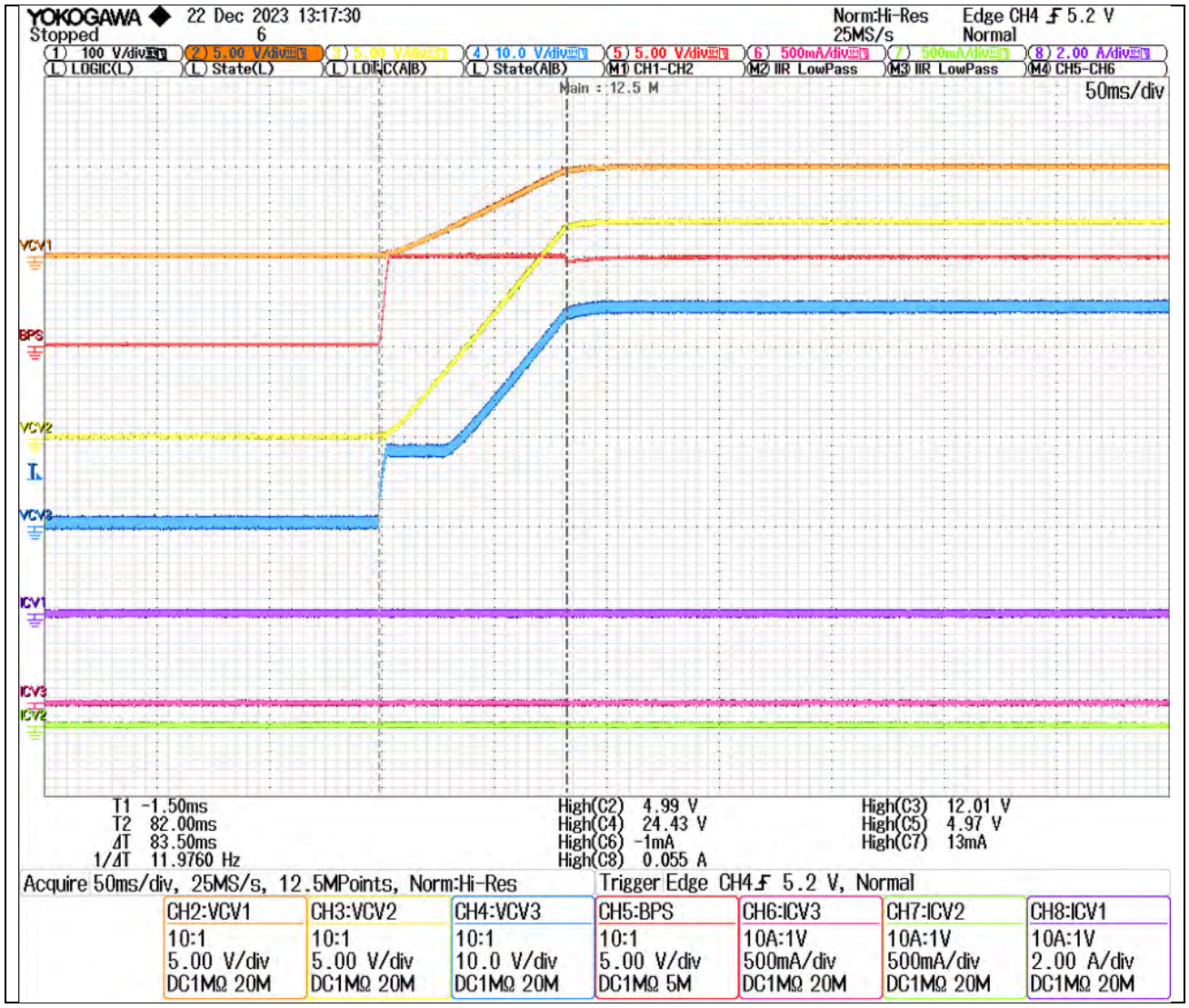



**Figure 41 –** No-load Start-up, Line Input 90 VAC.

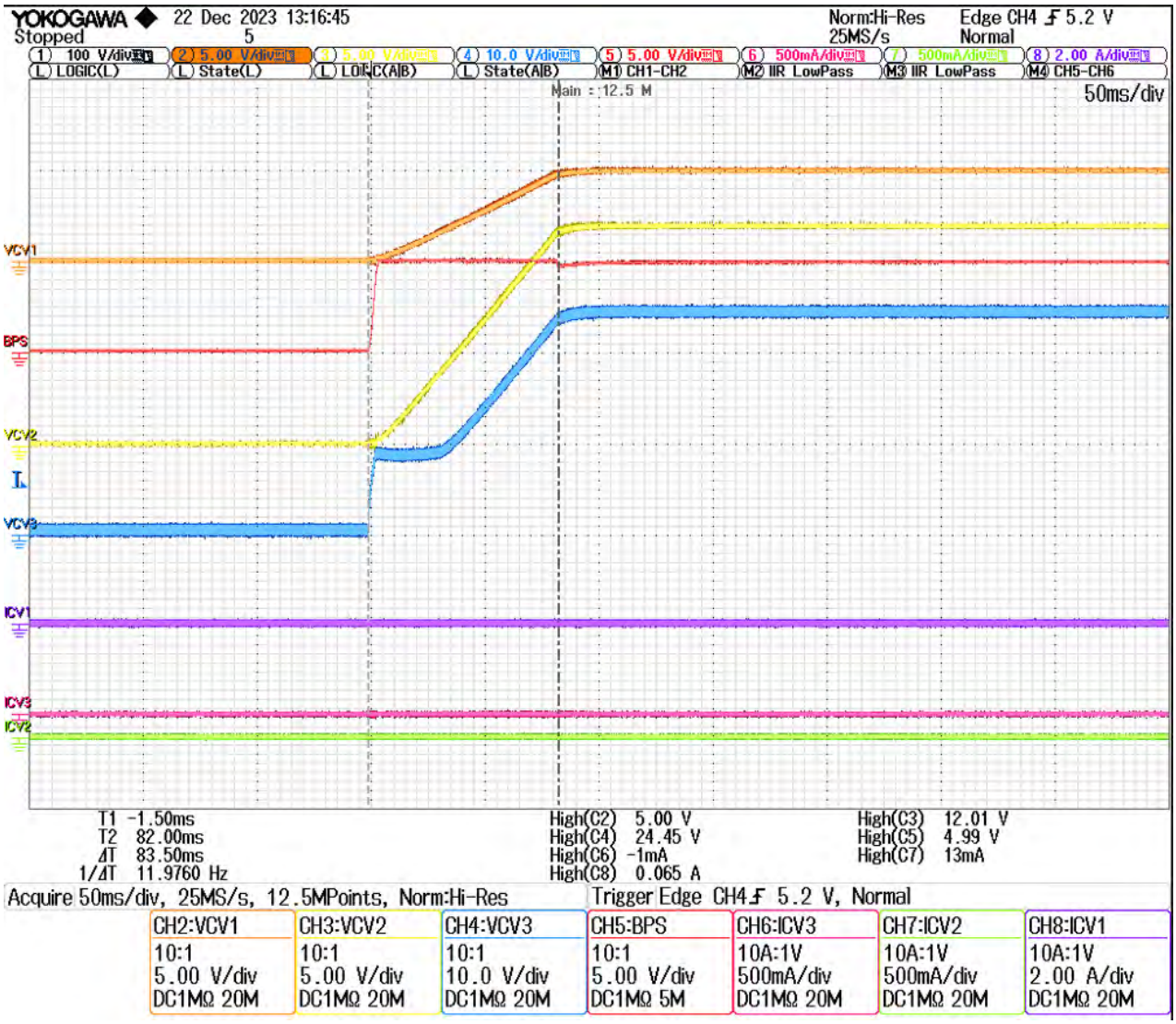



**Figure 42 –** No-load Start-up, Line Input 265 VAC.

### 9.8.3 Start-up Under CV Fault Conditions

| | |
|---|---|
| CH1 | FWD |
| CH2 | VCV1 |
| CH3 | VCV2 |
| CH4 | CDR3 |
| CH5 | CDR1 |
| CH6 | ICV3 |
| CH7 | ICV2 |
| CH8 | ICV1 |

Scope Channel Allocation (This Section).

The converter was tested for start-up under two types of single fault conditions, namely:

- Short-circuit to GND at CV1 output
- Short-circuit to GND at CV2 output
- Short-circuit to GND at CV3 output
- Open circuit of feedbacks

In all cases, the converter protection prevented any permanent damage to its components. The line fuse F1 remained intact. The converter went into auto restart for the duration of the fault condition. It resumed normal operation after the fault condition was removed.

Details of the start-up behavior under those fault conditions are shown in Figure 43 to Figure 66

### 9.8.4 Protection Under Fault Conditions

| CV's Full Load | Faults Before Start-up | | | | | |
|---|---|---|---|---|---|---|
| | CV1 Short to GND | | CV2 Short to GND | | CV3 Short to GND | |
| | 90 V | 265 V | 90 V | 265 V | 90 V | 265 V |
| Protection Definition | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled |

| CV's No-Load | Faults Before Start-up | | | | | |
|---|---|---|---|---|---|---|
| | CV1 Short to GND | | CV2 Short to GND | | CV3 Short to GND | |
| | 90 V | 265 V | 90 V | 265 V | 90 V | 265 V |
| Protection Definition | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled |

| CV's Full Load | Faults Before Start-up | | | | | |
|---|---|---|---|---|---|---|
| | CV1 FB Open | | CV2 FB Open | | CV3 FB Open | |
| | 90 V | 265 V | 90 V | 265 V | 90 V | 265 V |
| Protection Definition | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled |

| CV's No-Load | Faults Before Start-up | | | | | |
|---|---|---|---|---|---|---|
| | CV1 FB Open | | CV2 FB Open | | CV3 FB Open | |
| | 90 V | 265 V | 90 V | 265 V | 90 V | 265 V |
| Protection Definition | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled | Protection Enabled |

### 9.8.4.1 Start-up Under CV Fault Conditions

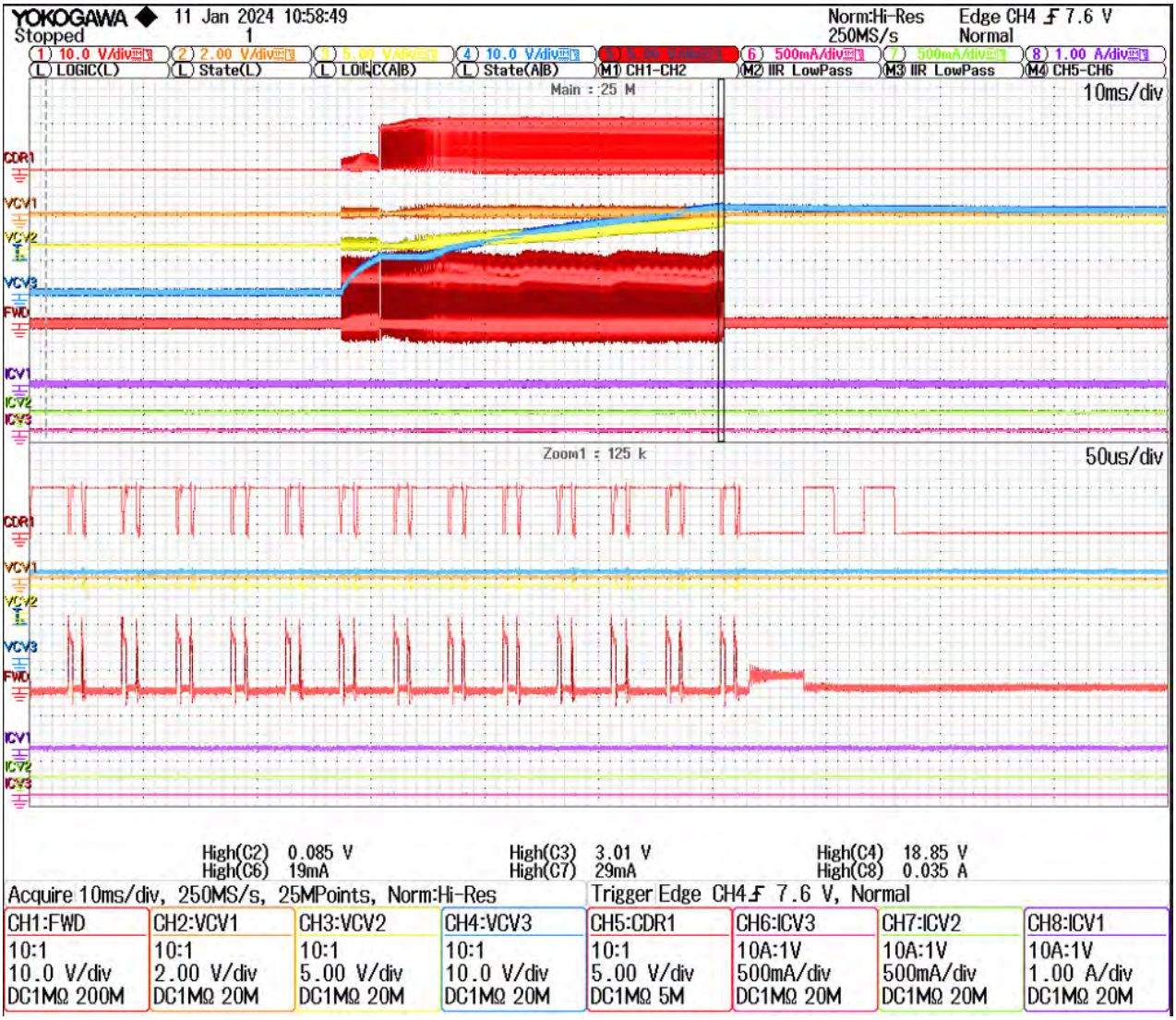



**Figure 43 –** Start-up With CV1 Shorted to GND. Line Input 90 V, No-Load.

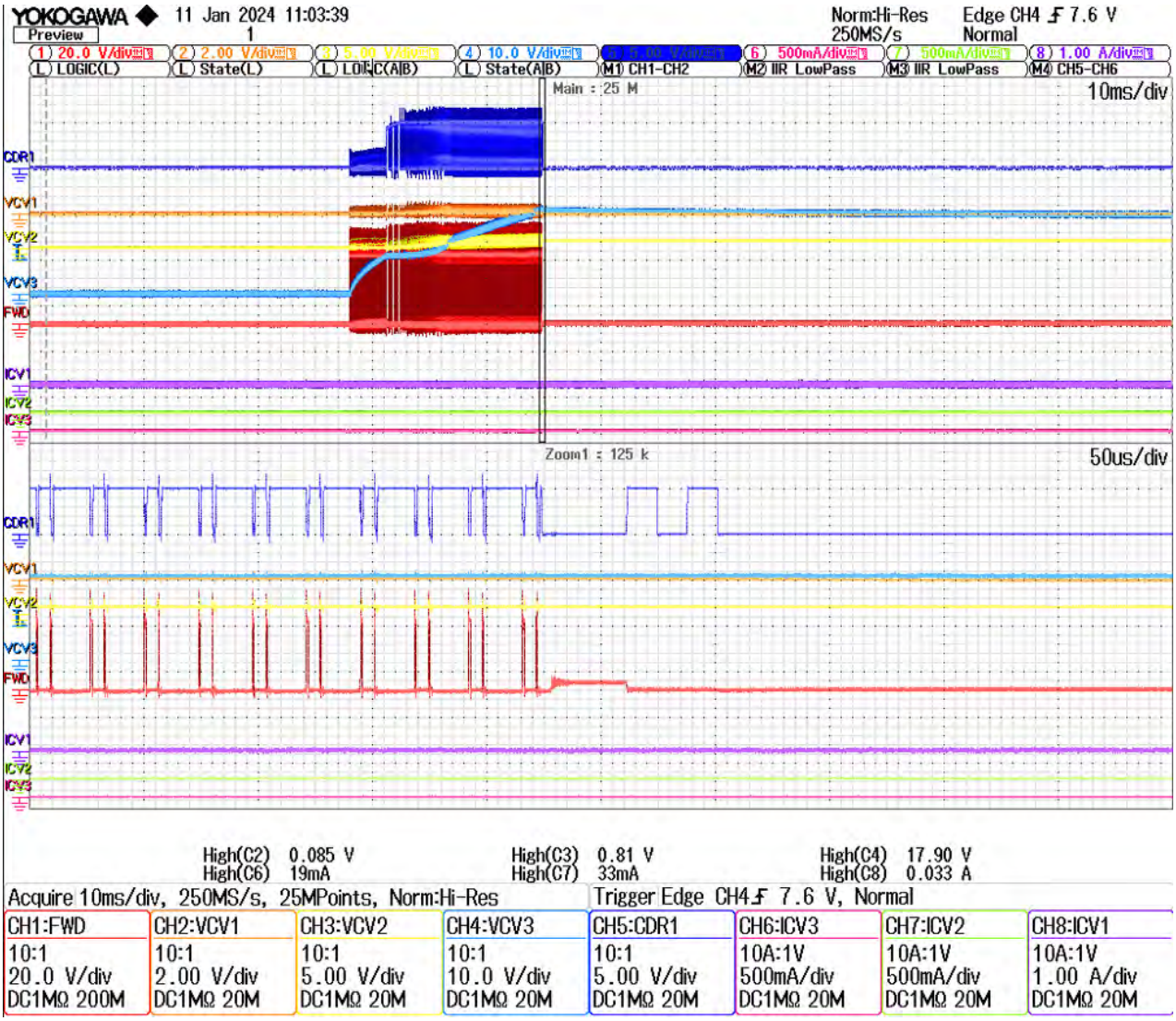



**Figure 44 –** Start-up With CV1 Shorted to GND. Line Input 265 V, No-Load.

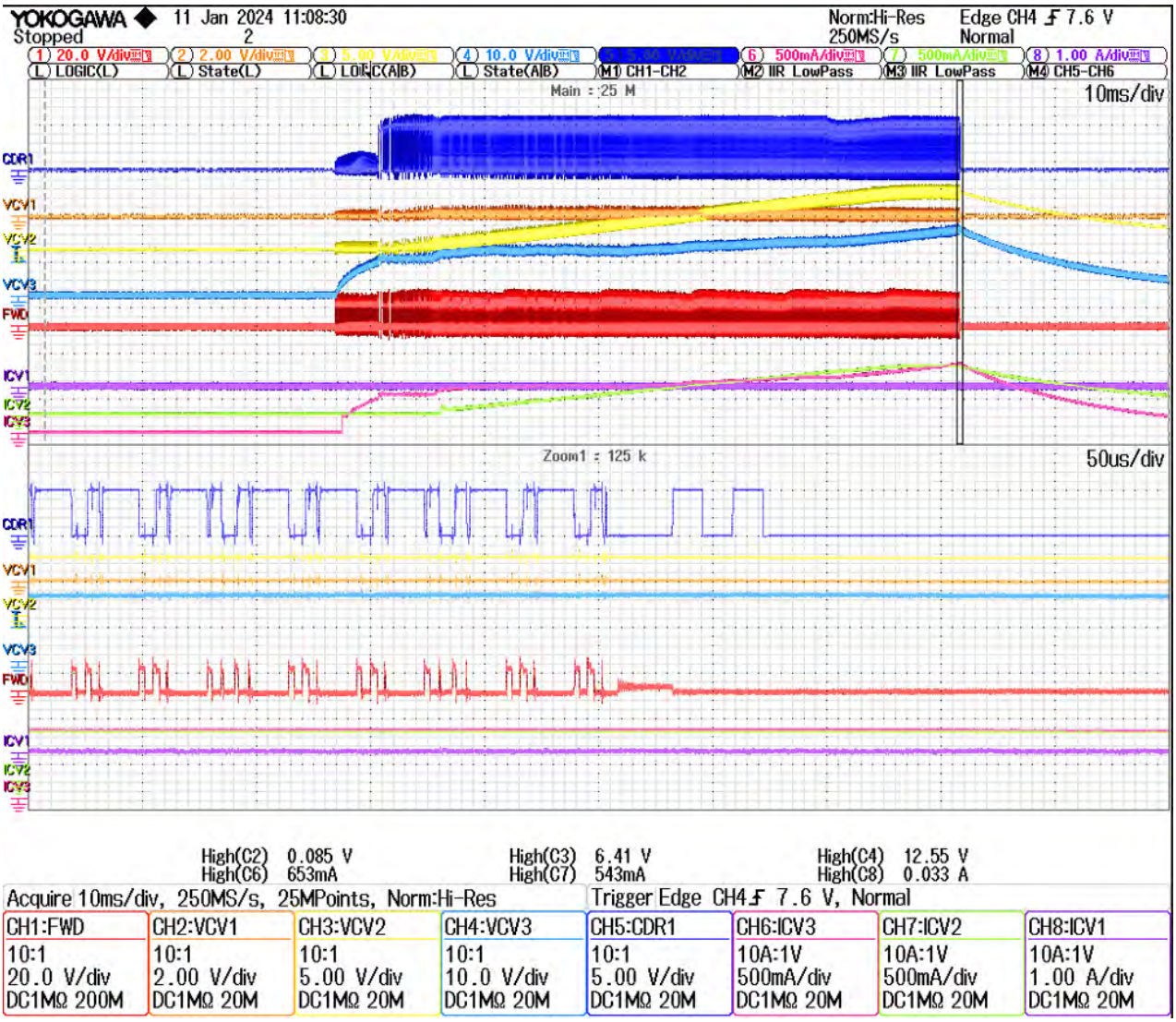



**Figure 45 –** Start-up With CV1 Shorted to GND. Line Input 90 V, Full Load.

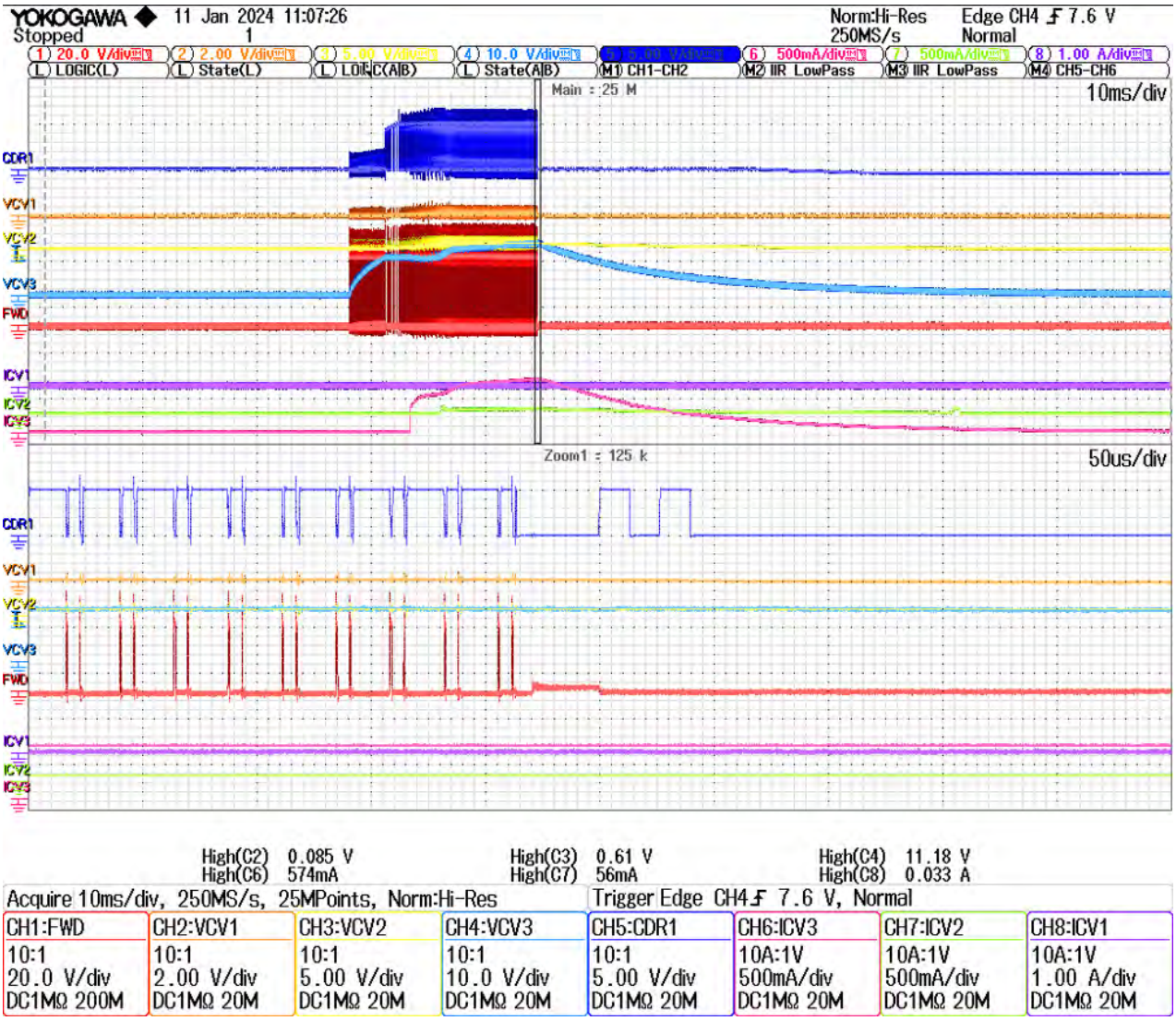



**Figure 46 –** Start-up With CV1 Shorted to GND. Line Input 265 V, Full Load.

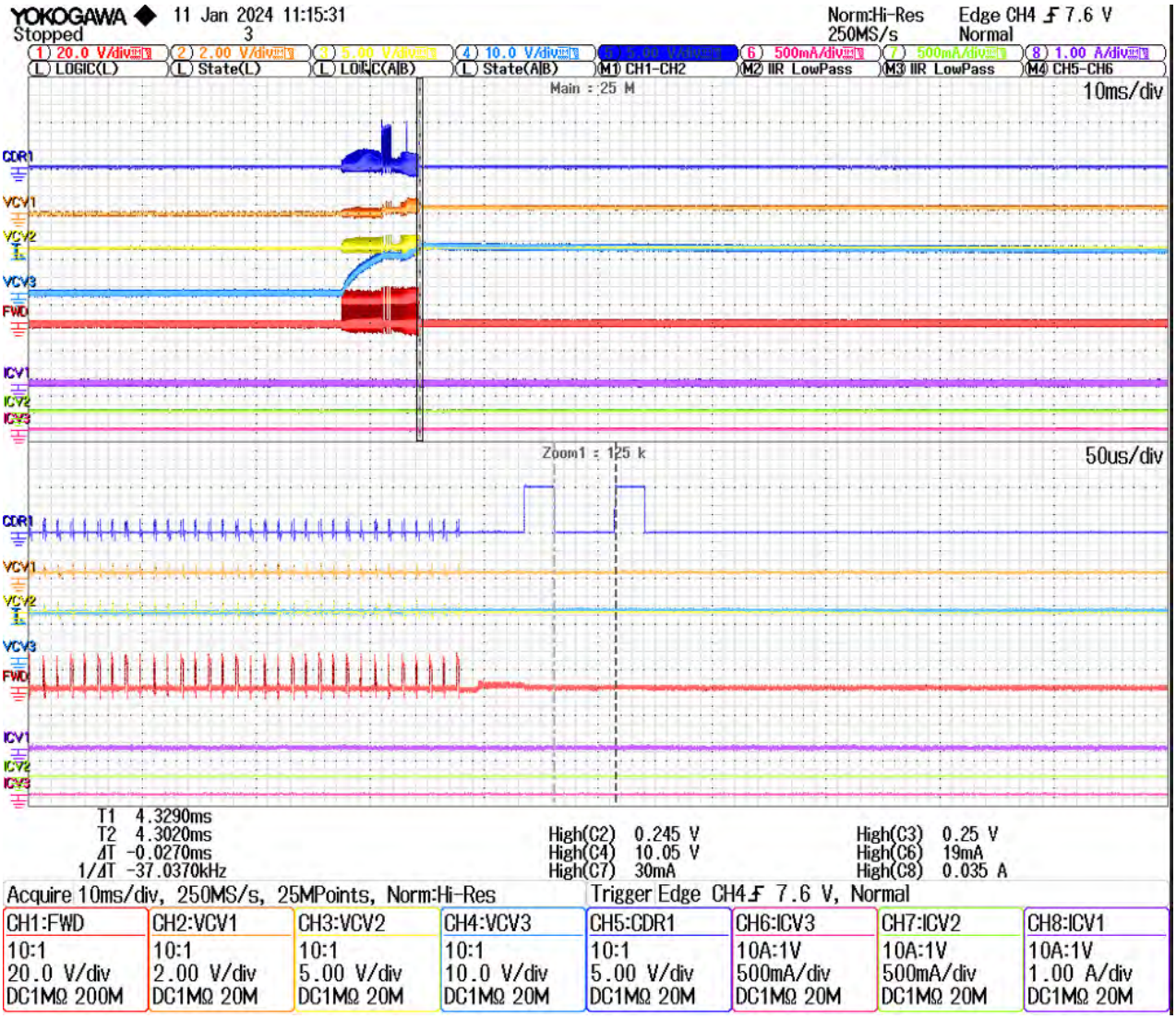



**Figure 47 –** Start-up With CV2 Shorted to GND. Line Input 90 V, No-Load.

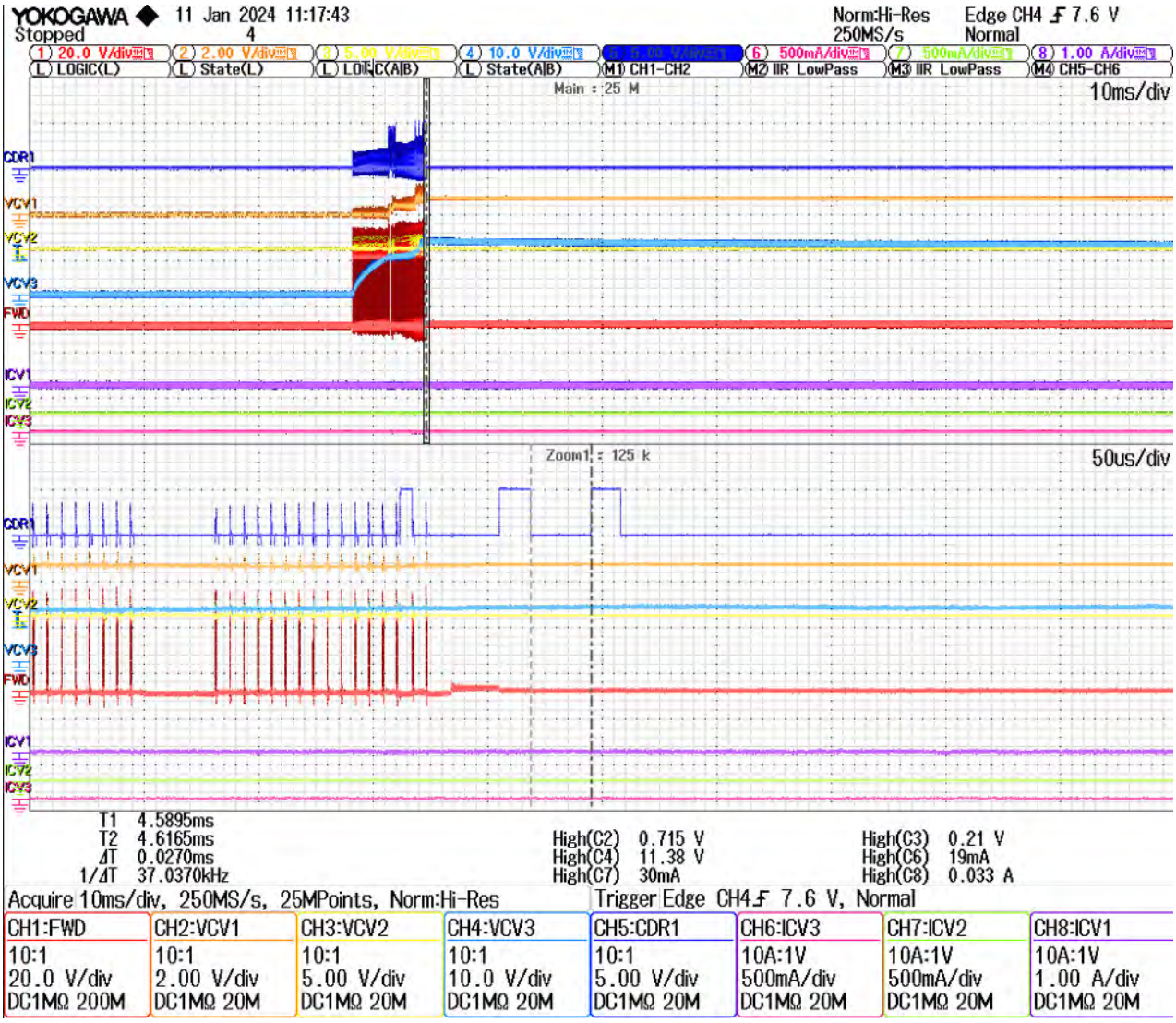



**Figure 48 –** Start-up With CV2 Shorted to GND. Line Input 265 V, No-Load.

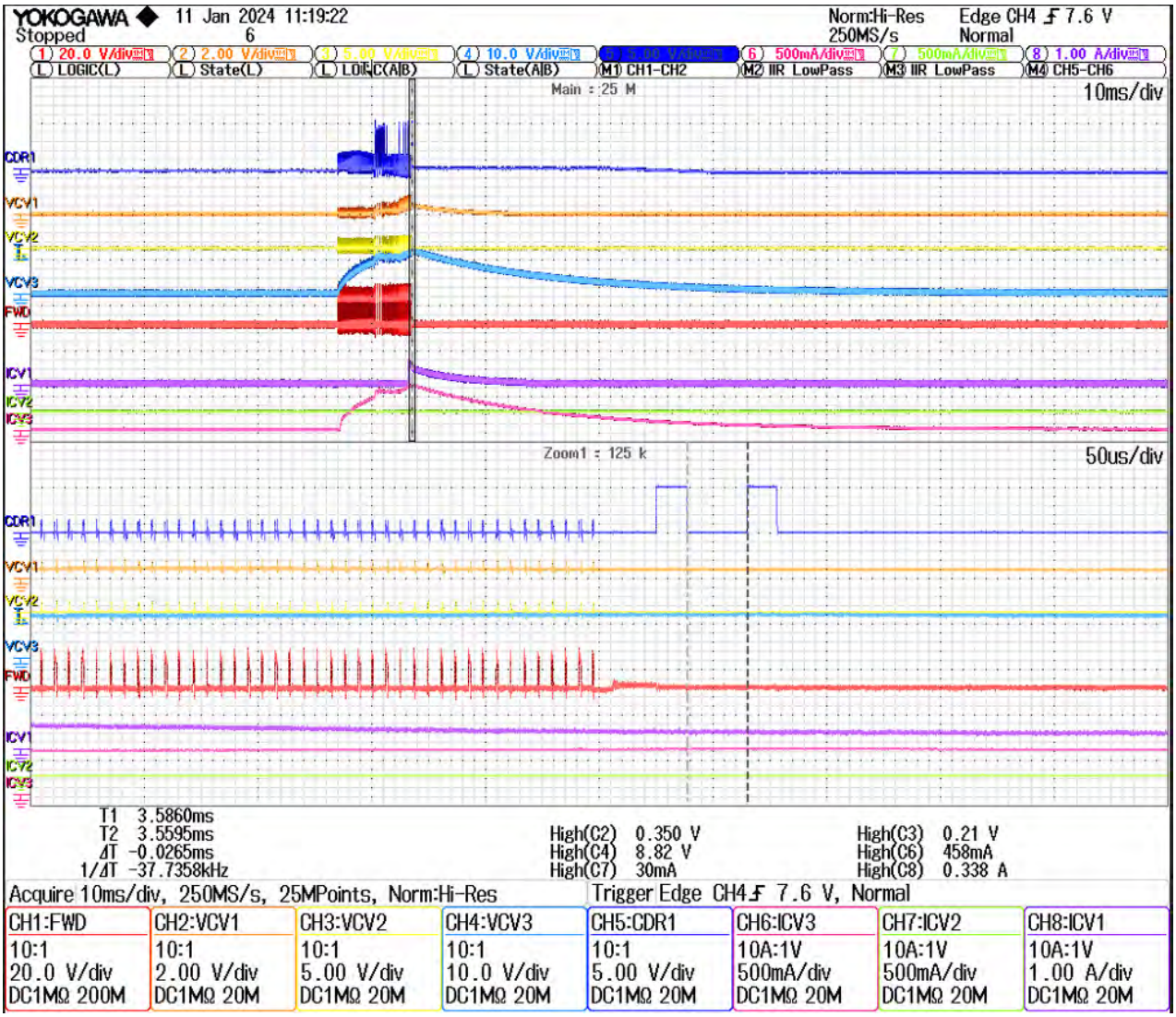



**Figure 49 –** Start-up With CV2 Shorted to GND. Line Input 90 V, Full Load.

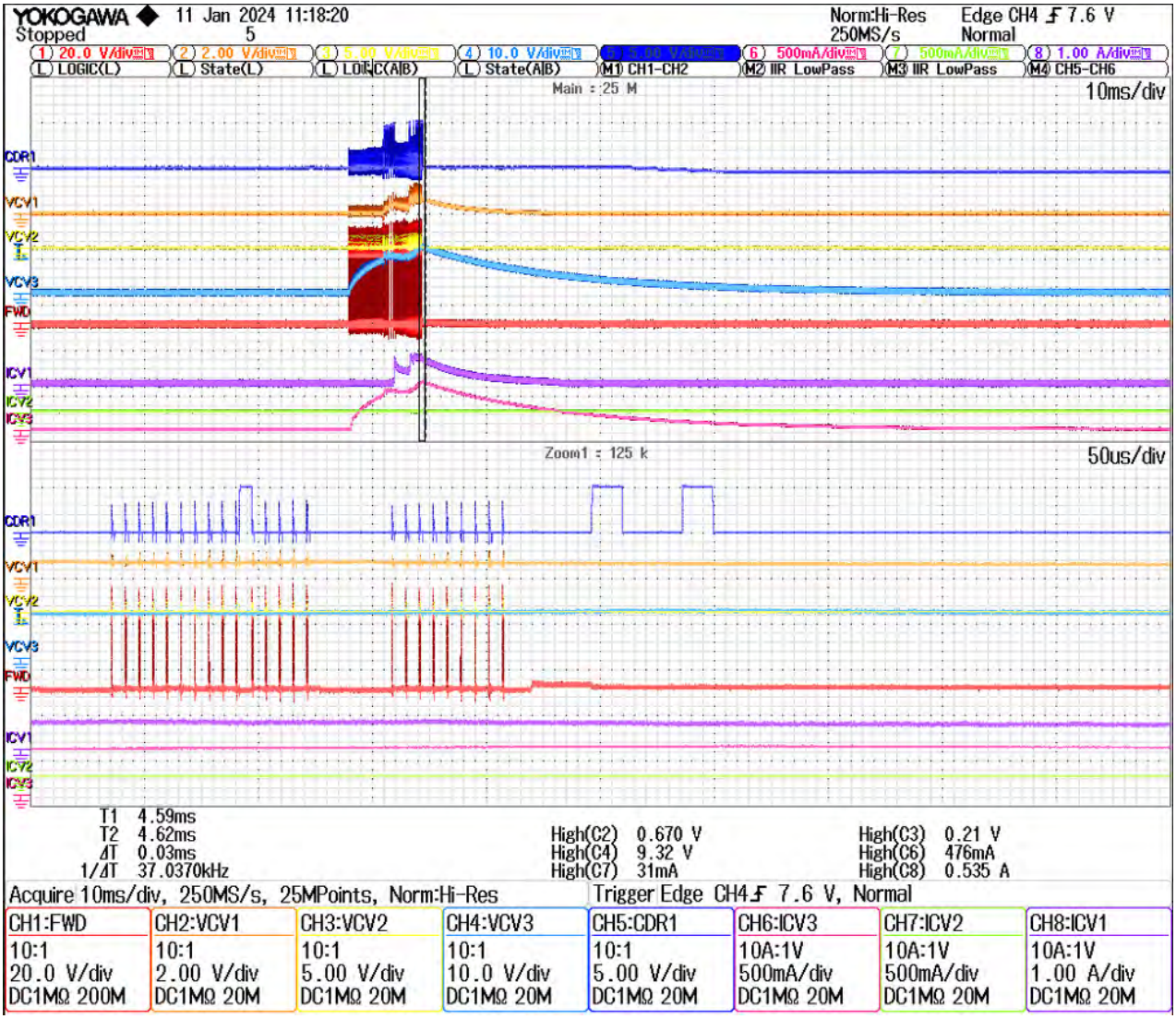



**Figure 50 –** Start-up With CV2 Shorted to GND. Line Input 265 V, Full Load.

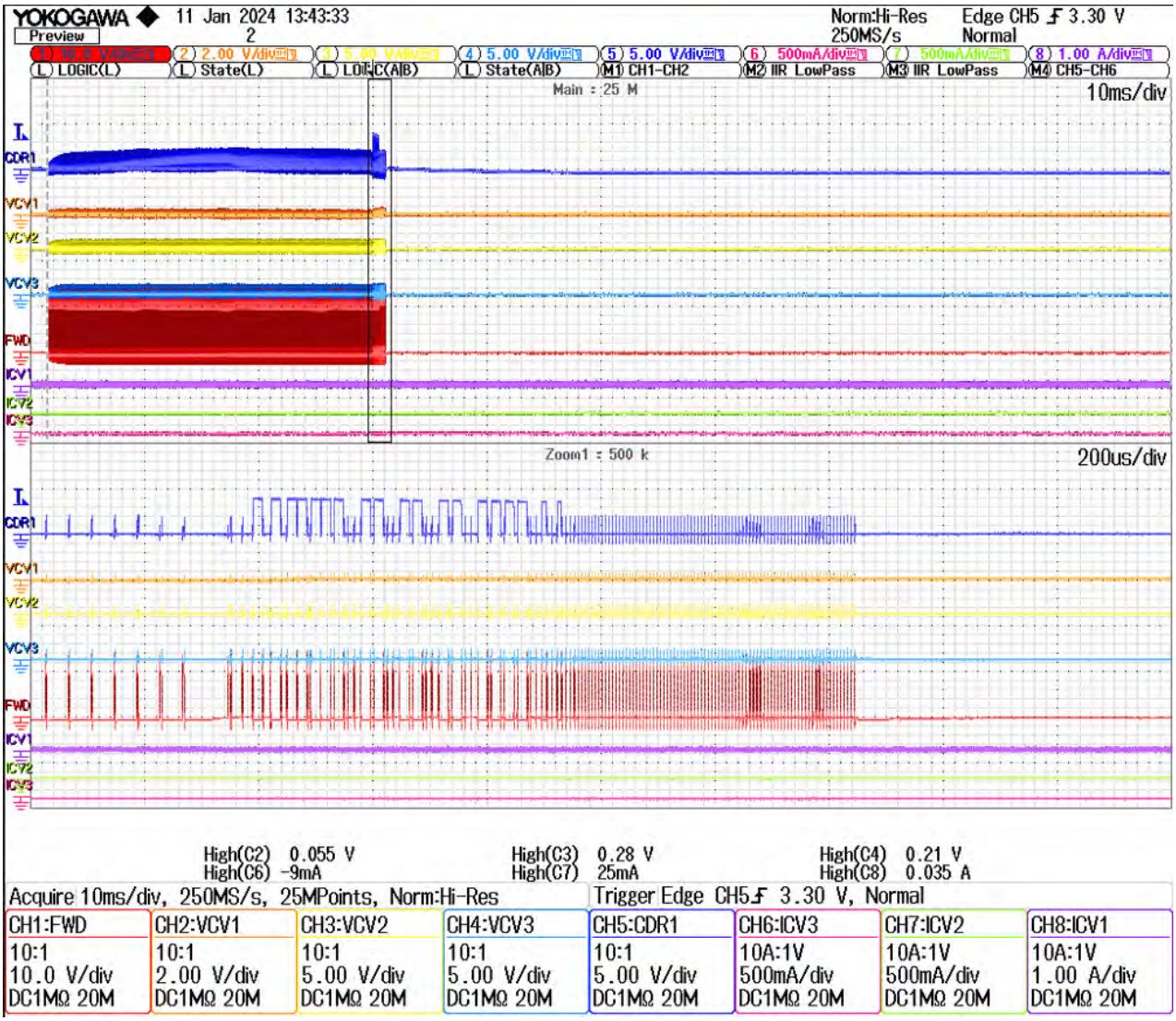



**Figure 51 –** Start-up With CV3 Shorted to GND. Line Input 90 V, No-Load.

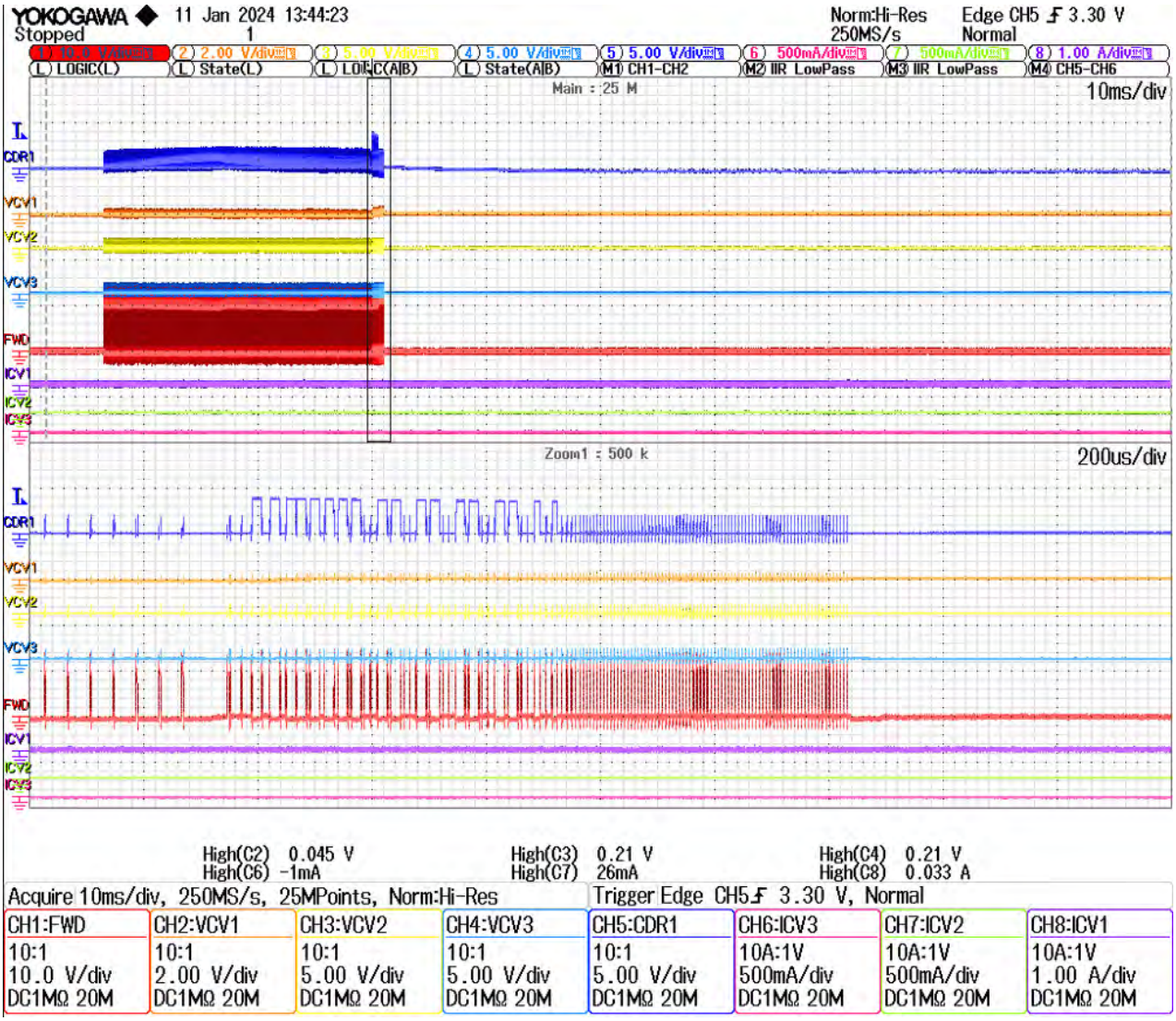



**Figure 52 –** Start-up with CV3 Shorted to GND. Line Input 90 V, Full Load.

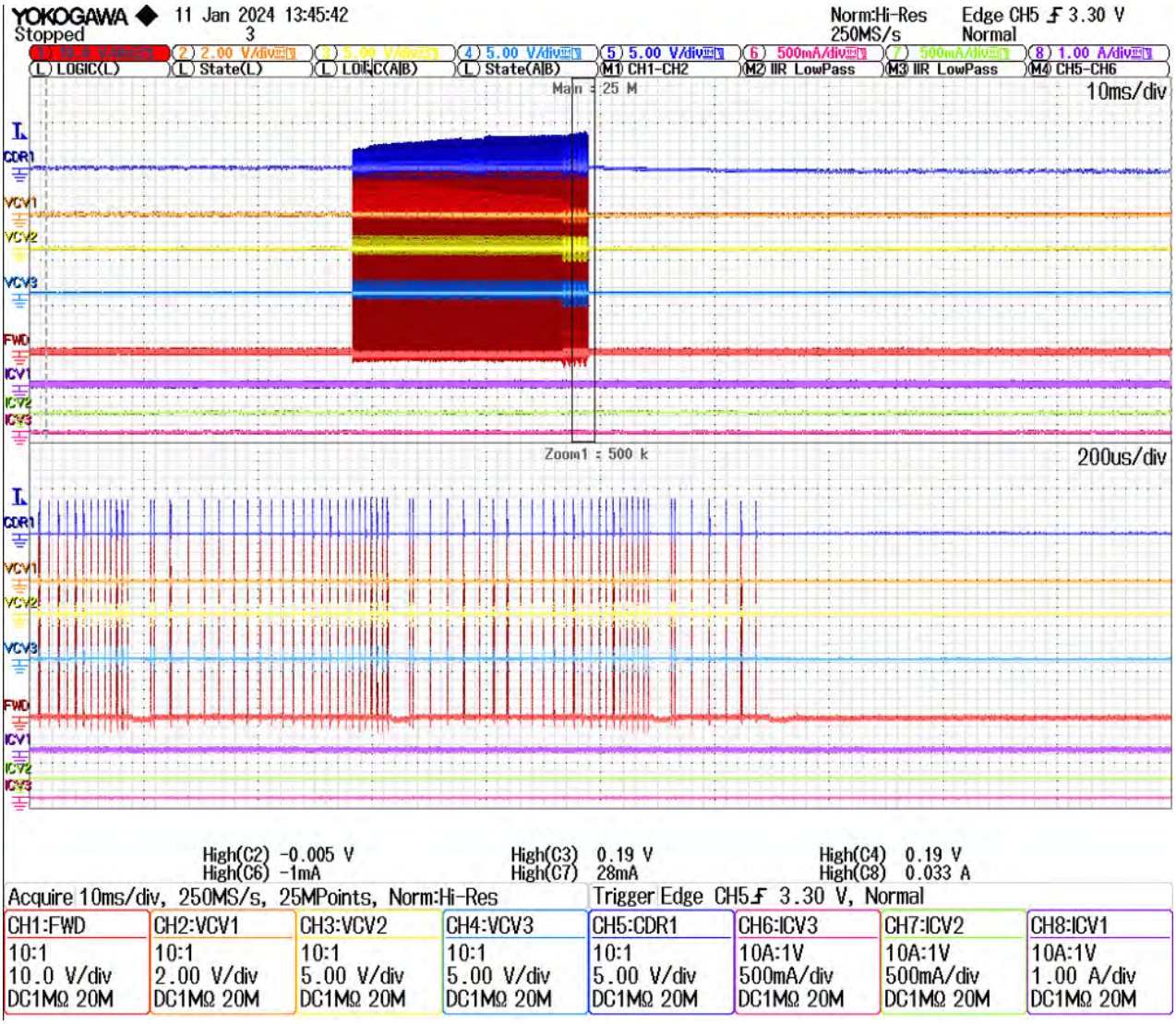



**Figure 53 –** Start-up with CV3 Shorted to GND. Line Input 265 V, No-Load.

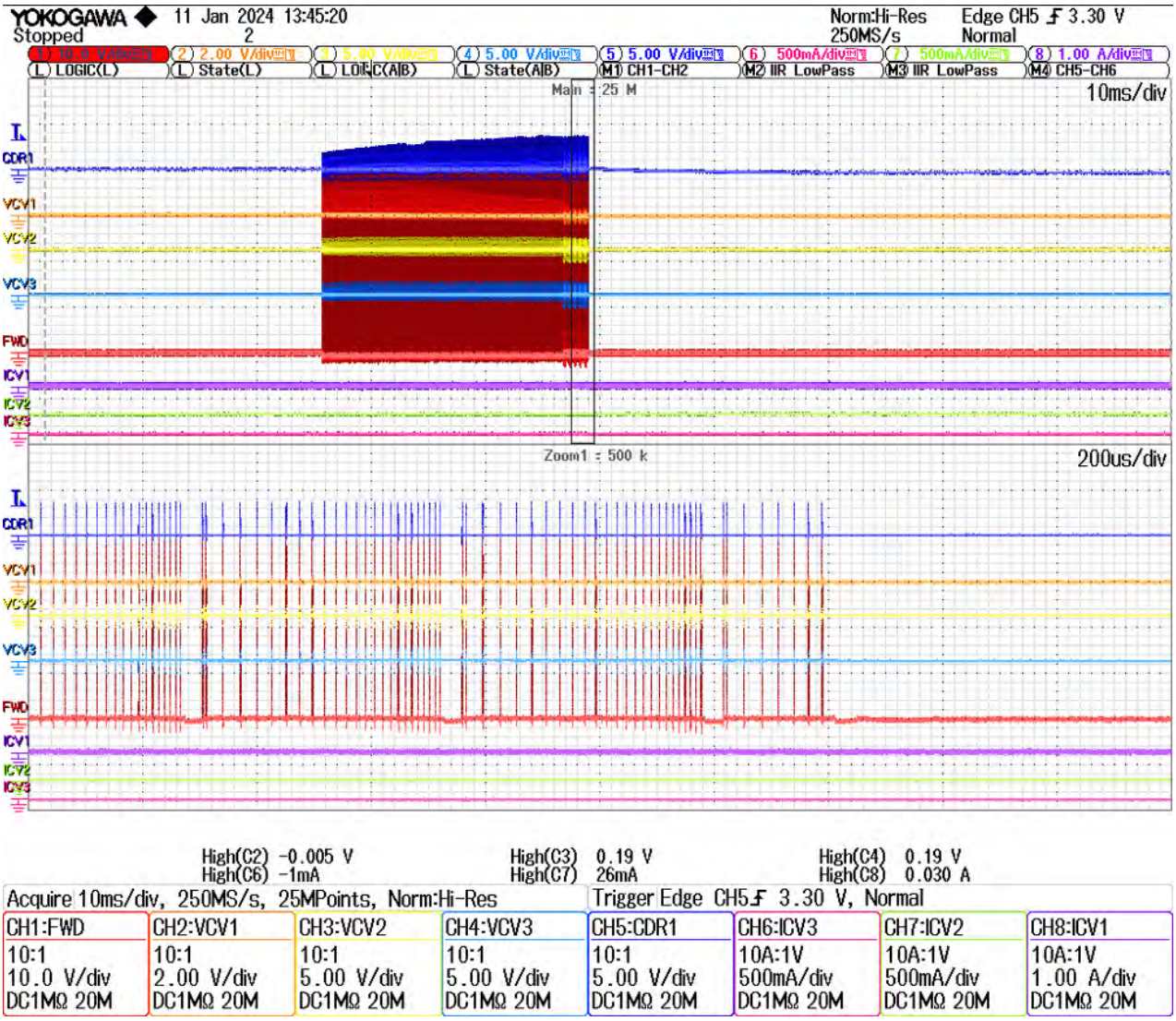



**Figure 54 –** Start-up With CV3 Shorted to GND. Line Input 265 V, Full Load.

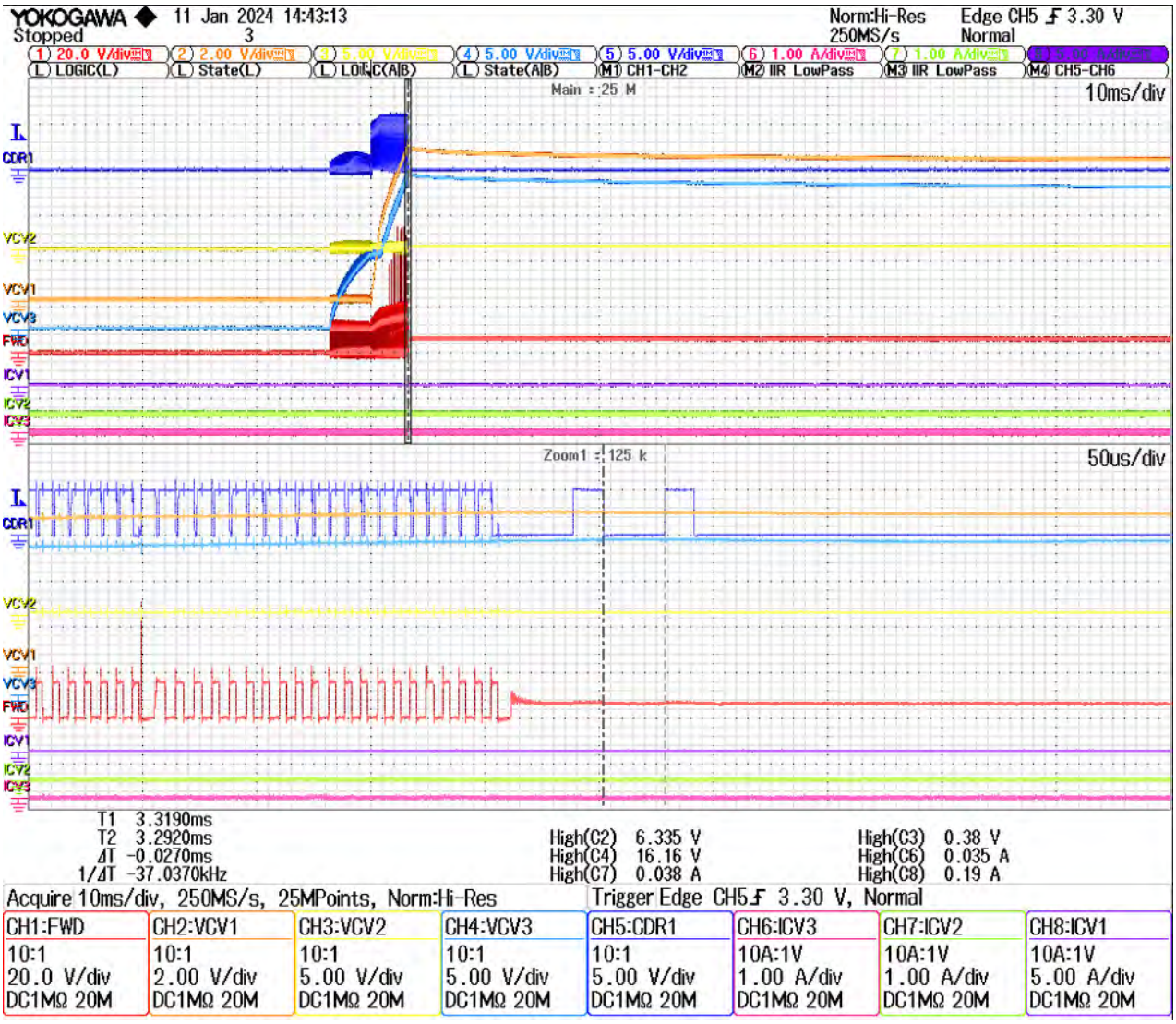



**Figure 55 –** Start-up With FB1 Open. Line Input 90 V, No-Load.

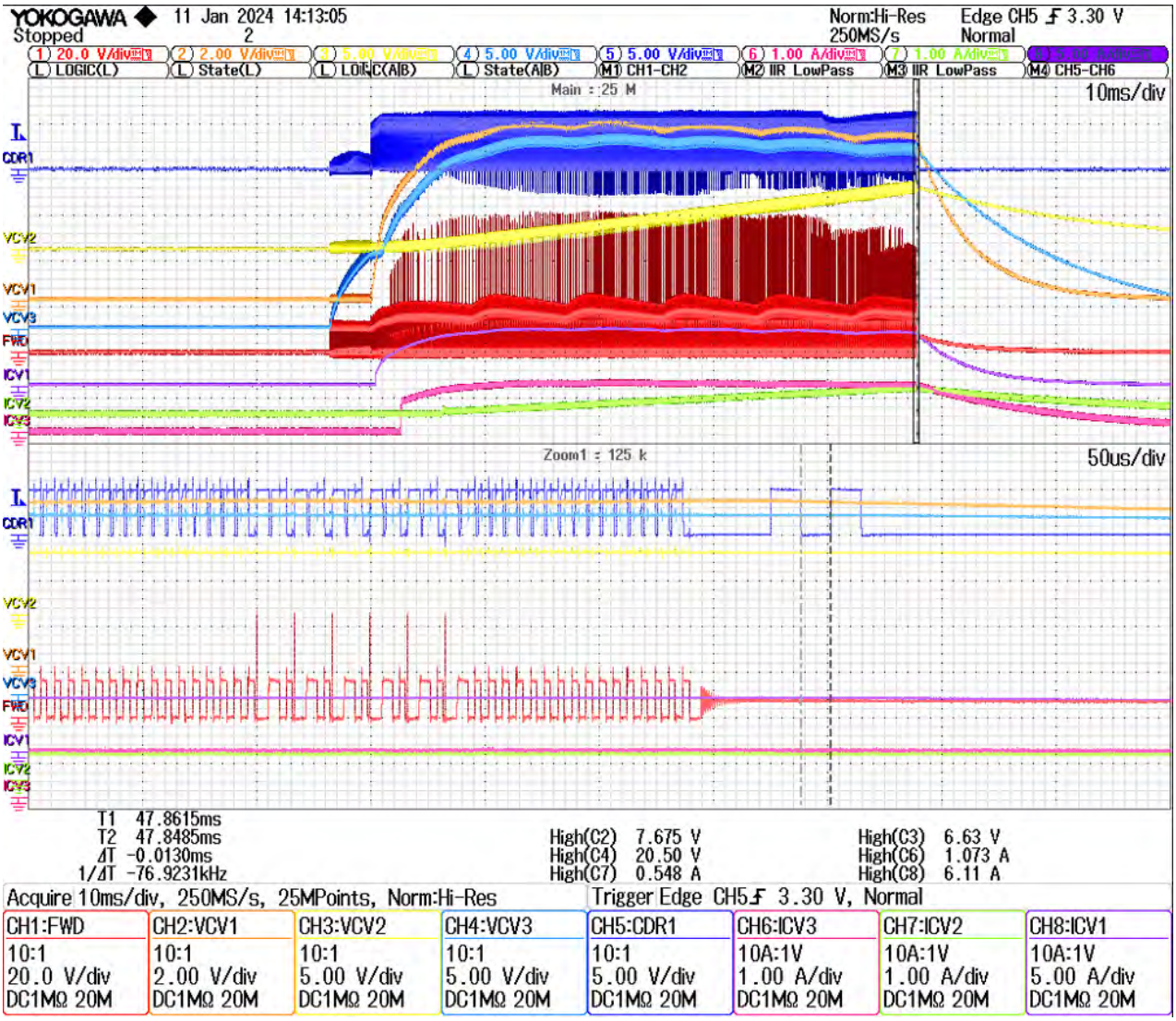



**Figure 56 –** Start-up With FB1 Open. Line Input 90 V, Full Load.

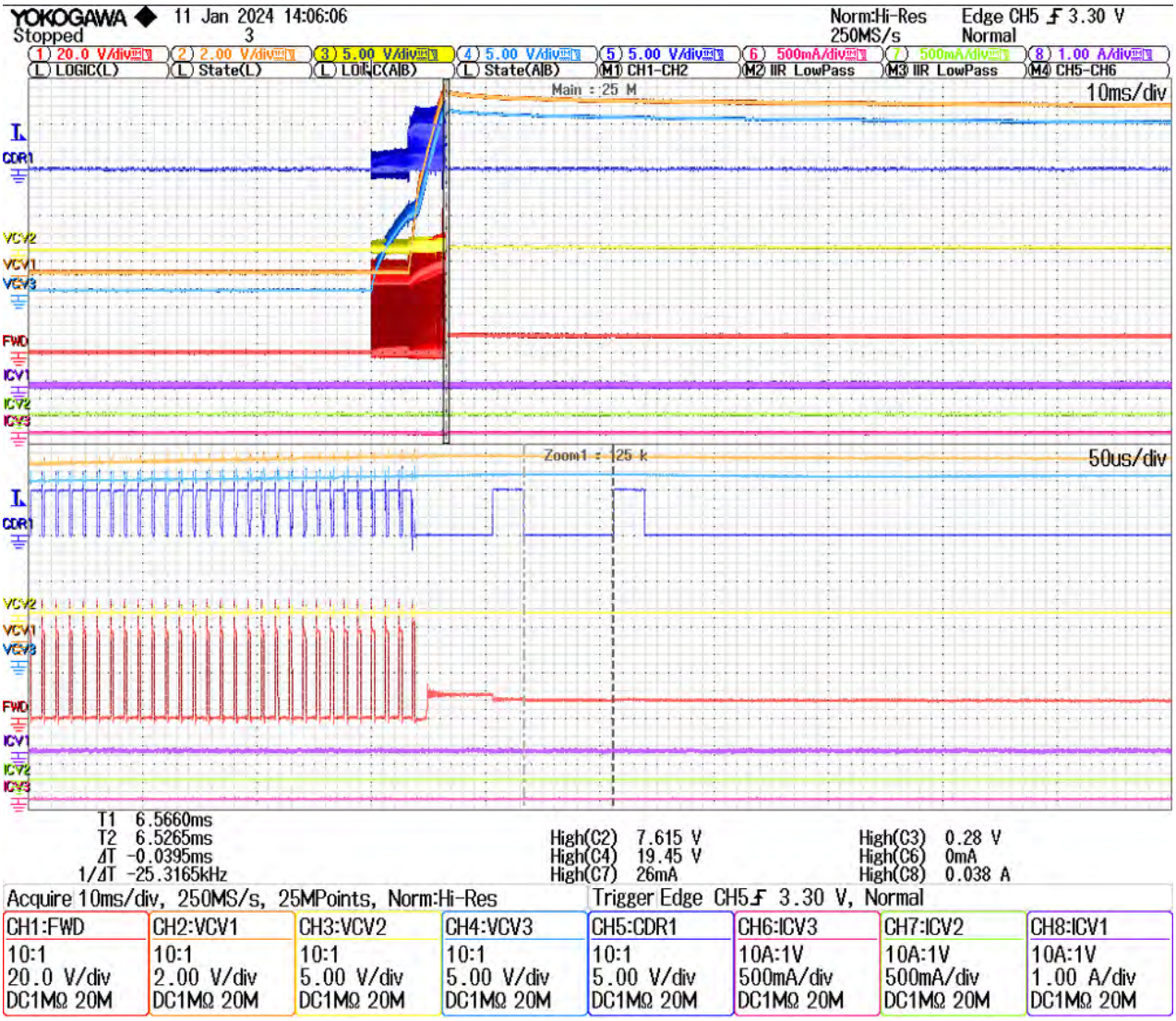



**Figure 57 –** Start-up With FB1 Open. Line Input 265 V, No-Load.

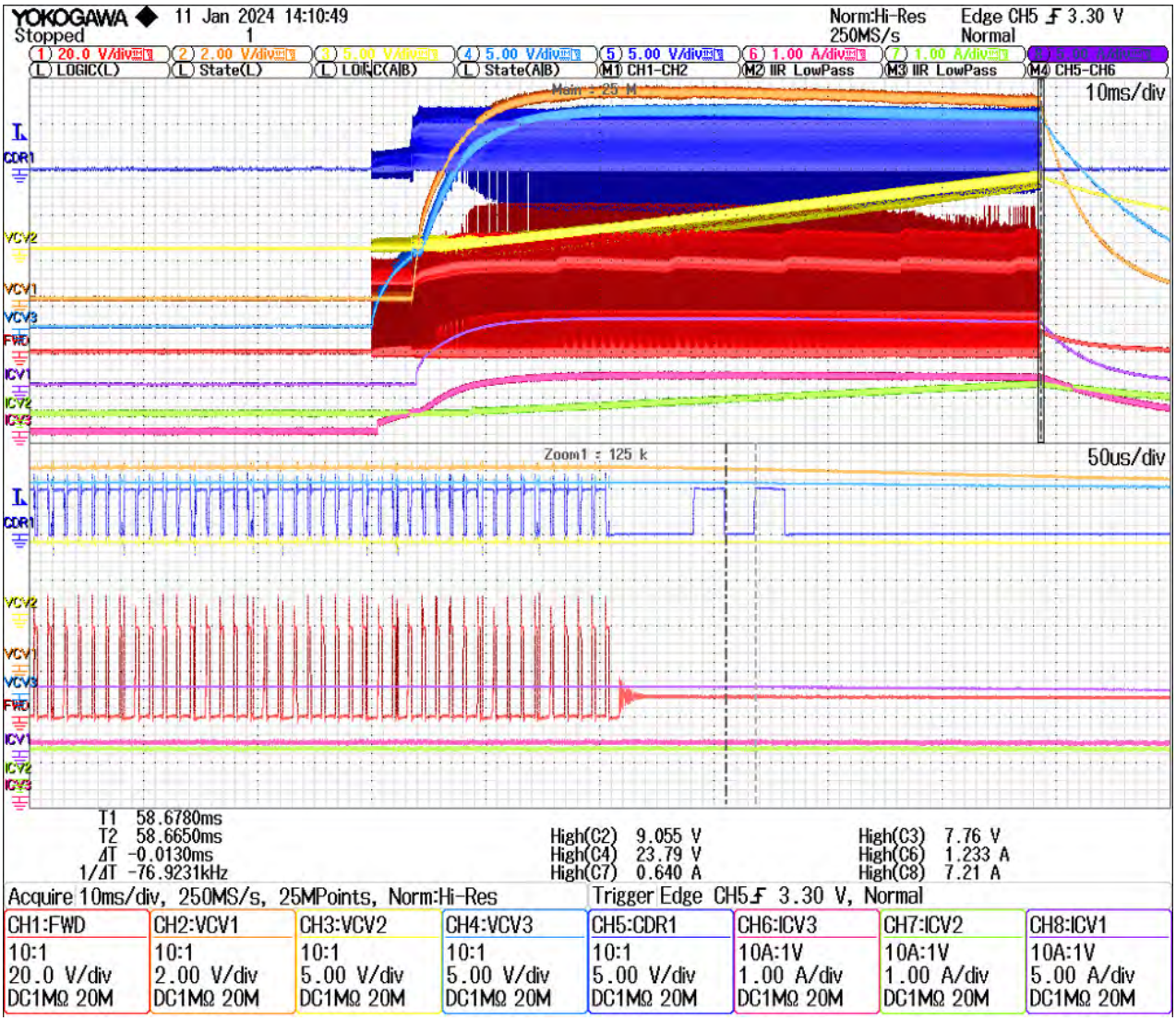



**Figure 58 –** Start-up With FB1 Open. Line Input 265 V, Full Load.

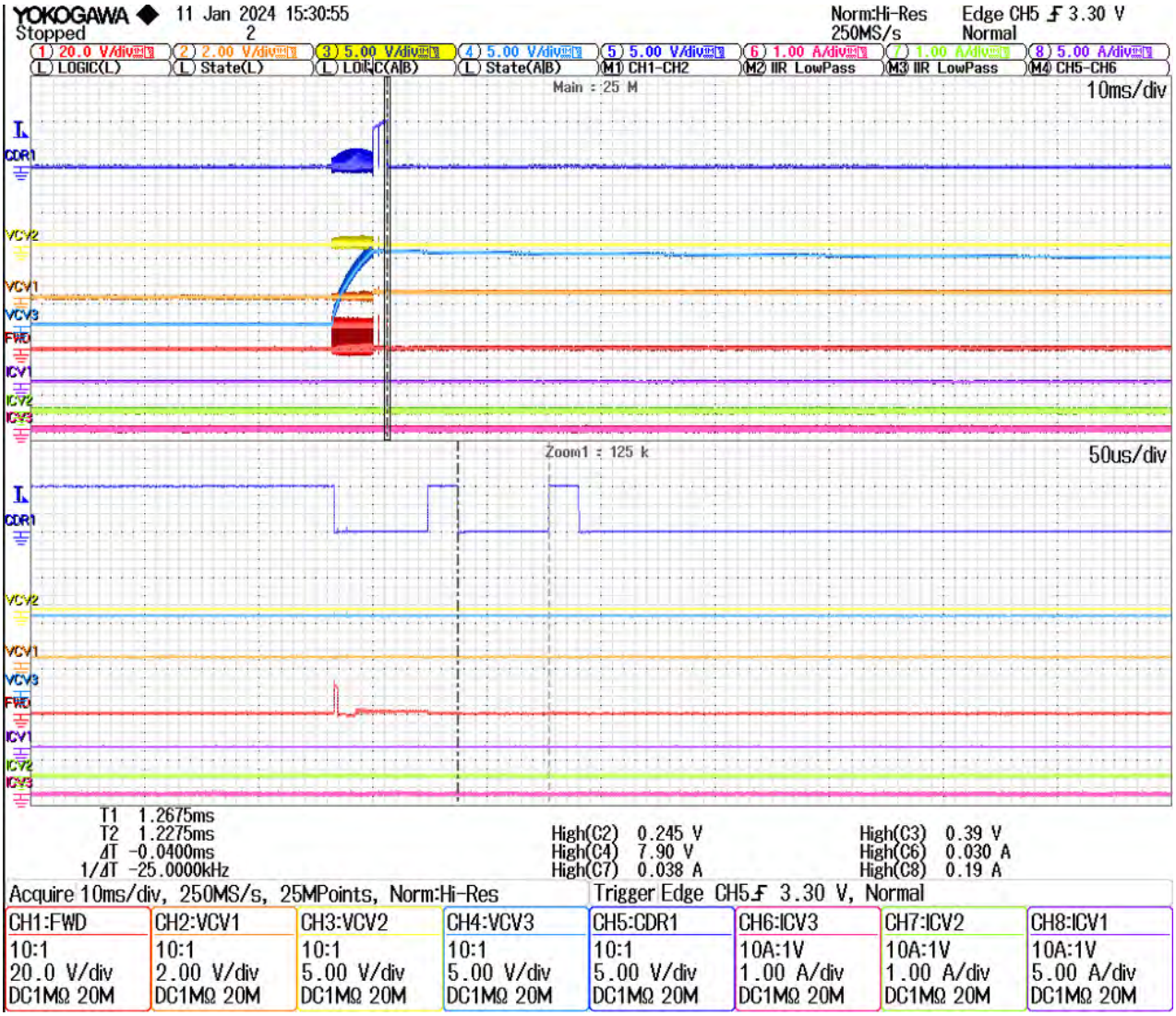



**Figure 59 –** Start-up With FB2 Open. Line Input 90 V, No-Load.

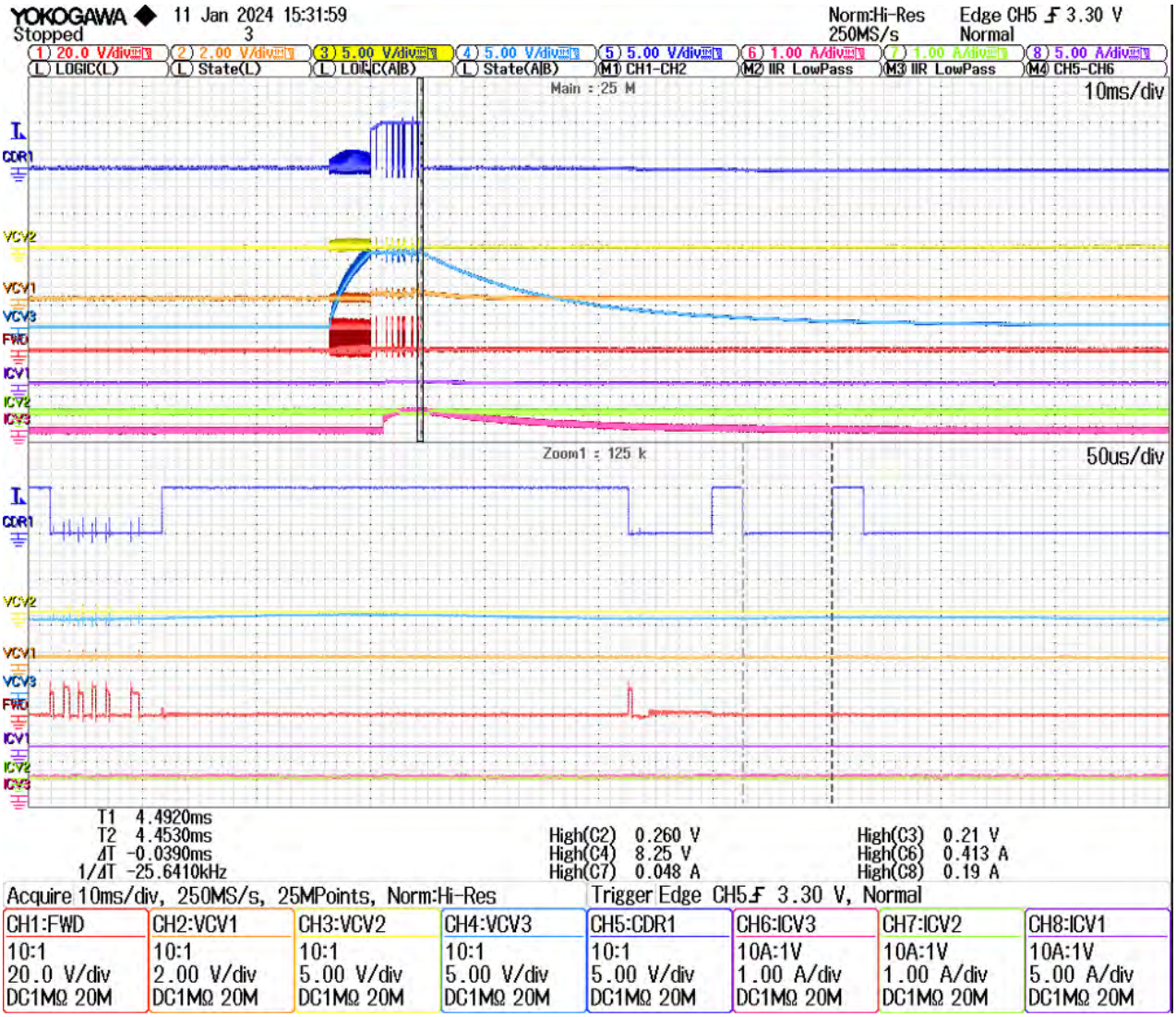



**Figure 60 –** Start-up With FB2 Open. Line Input 90 V, Full Load.

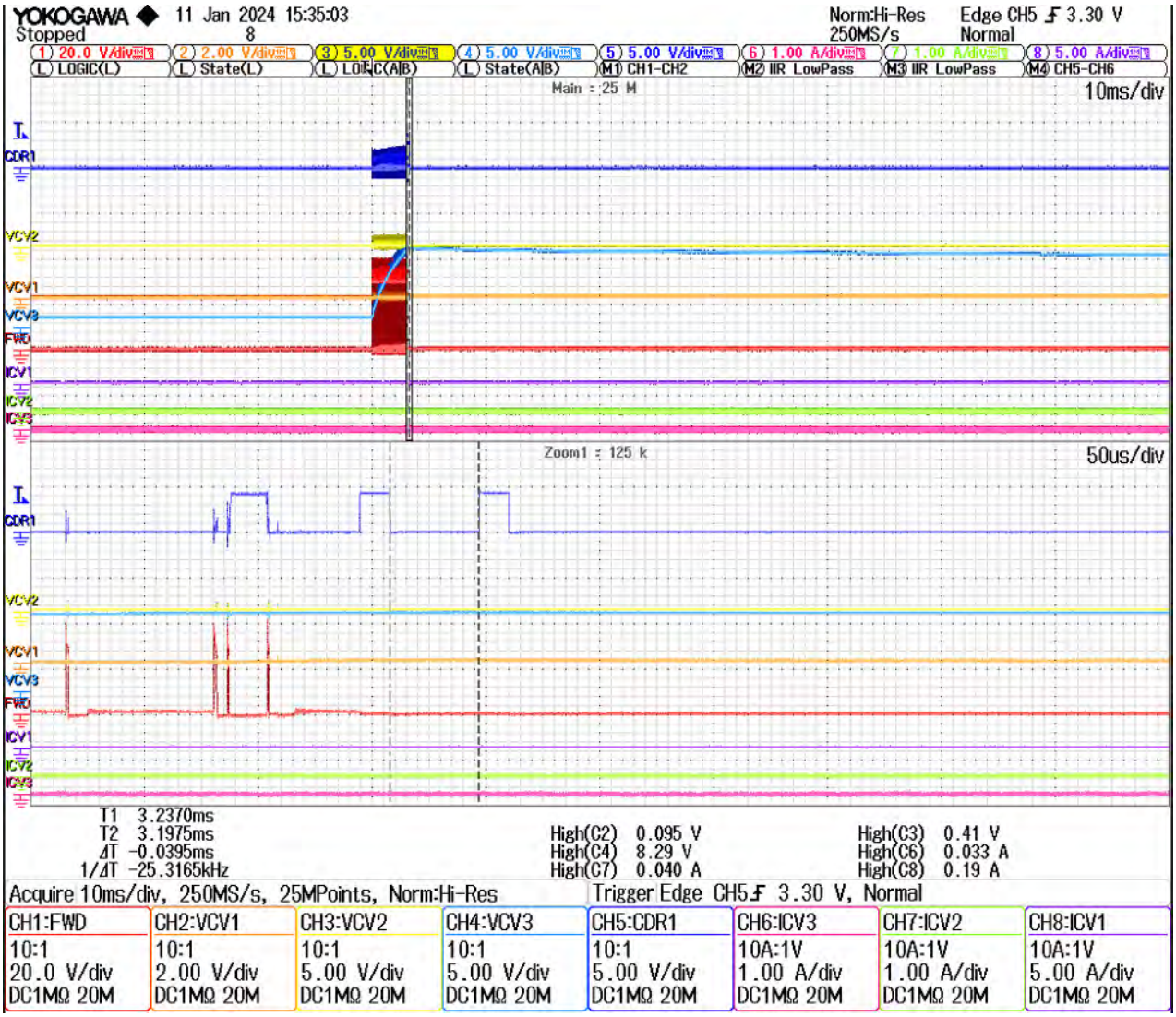



**Figure 61 –** Start-up With FB2 Open. Line Input 265 V, No-Load.

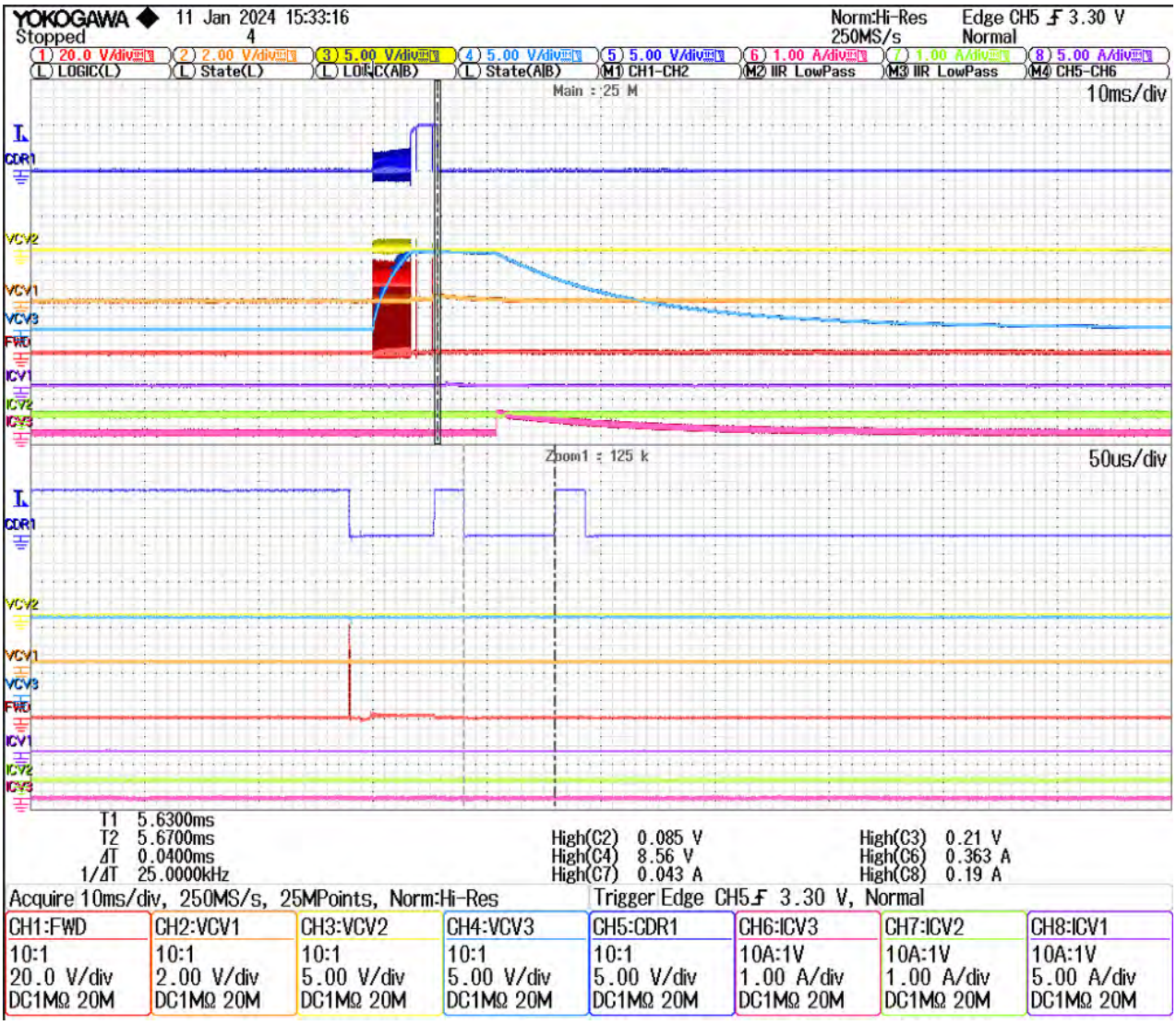



**Figure 62 –** Start-up With FB2 Open. Line Input 265 V, Full Load.

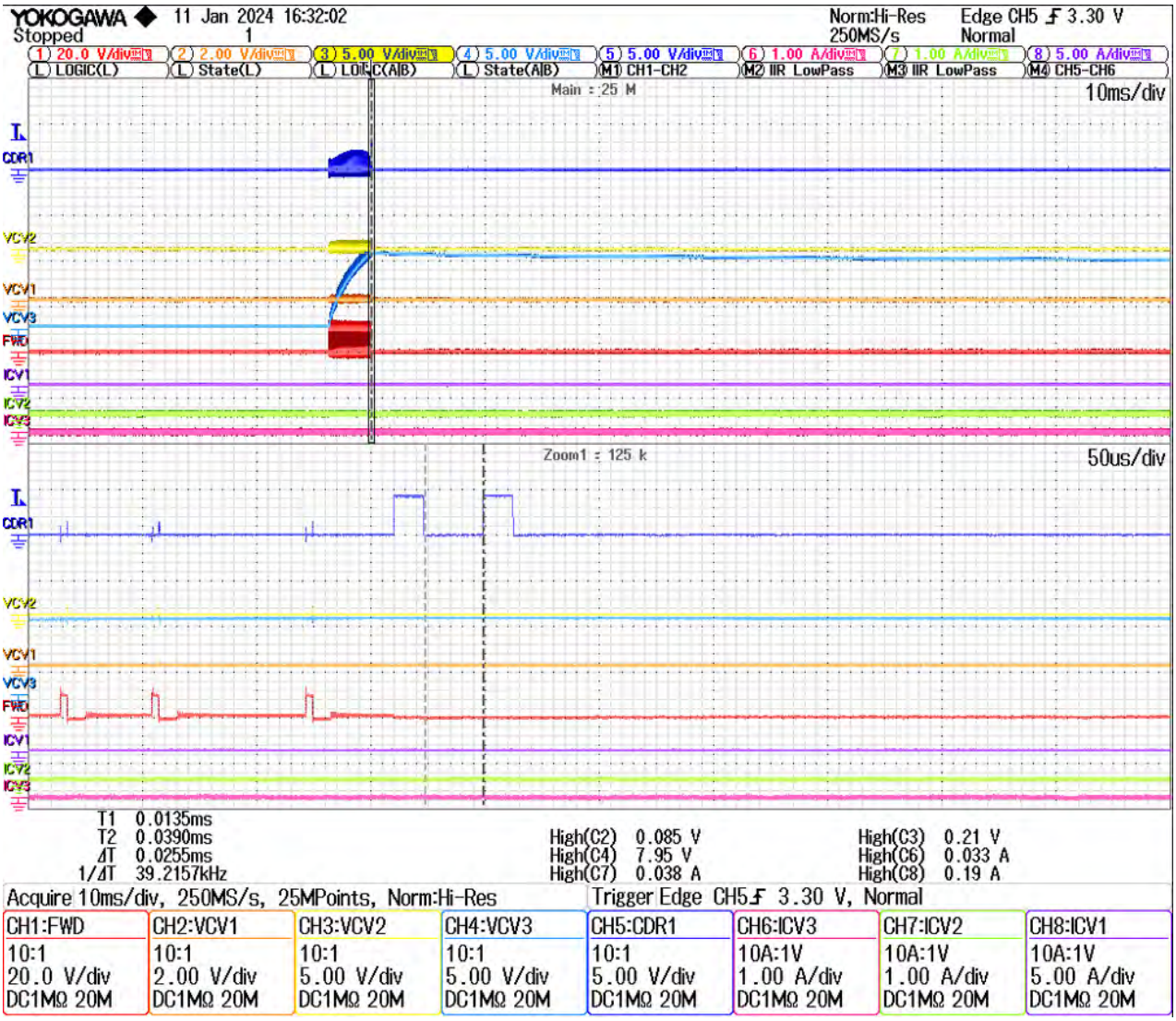



**Figure 63 –** Start-up With FB3 Open. Line Input 90 V, No-Load.

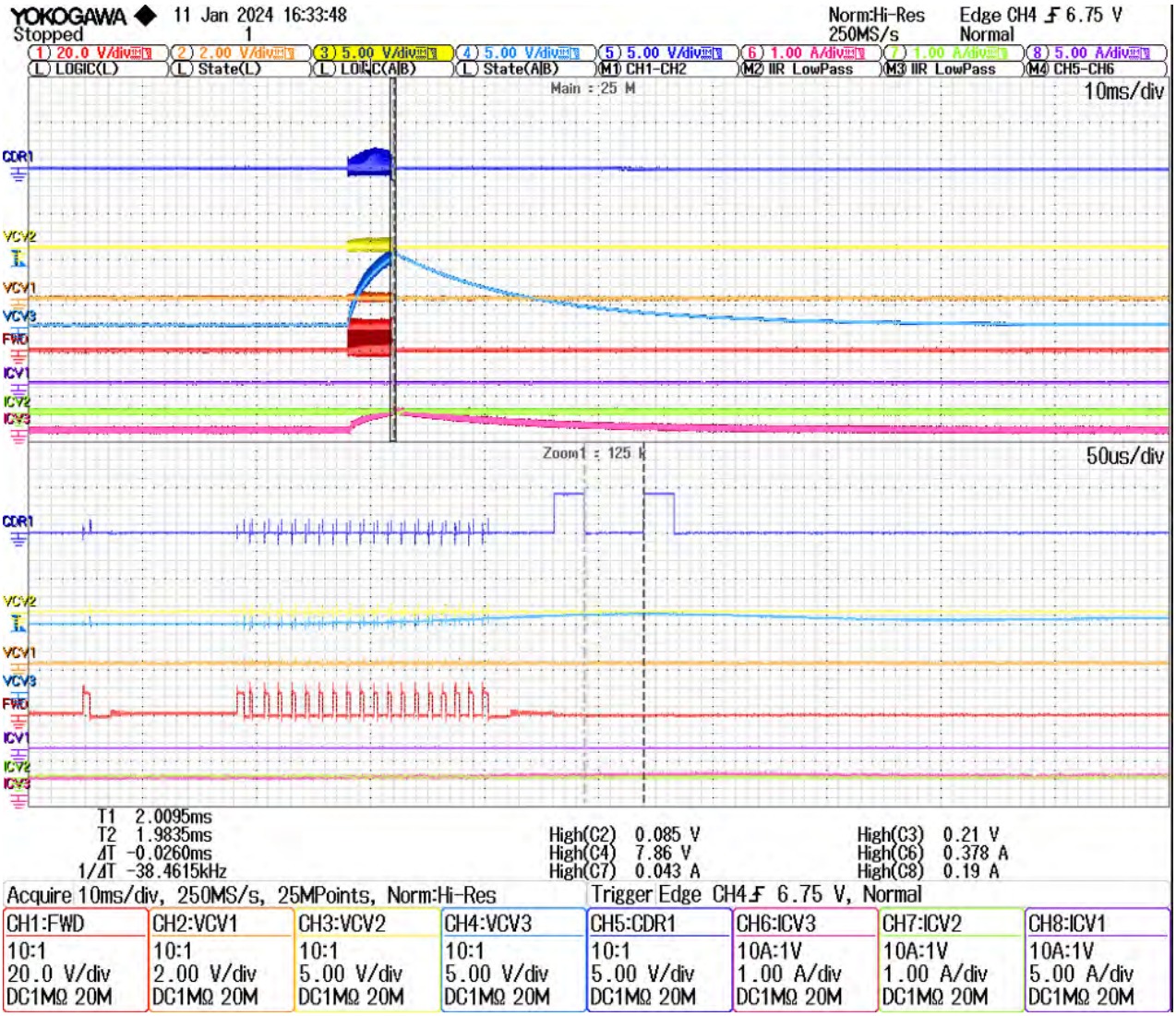



**Figure 64 –** Start-up With FB3 Open. Line Input 90 V, Full Load.

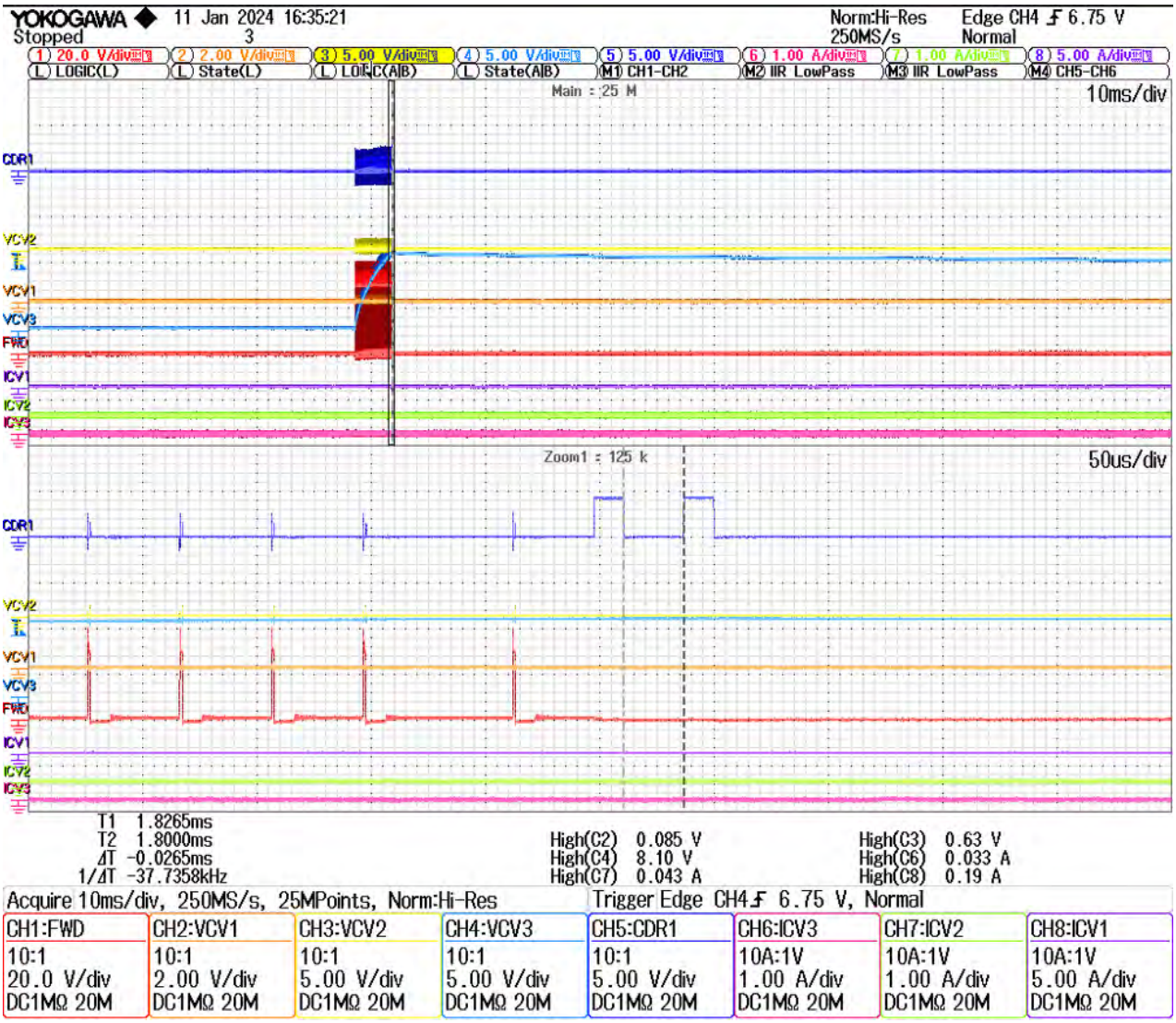



**Figure 65 –** Start-up With FB3 Open. Line Input 265 V, No-Load.

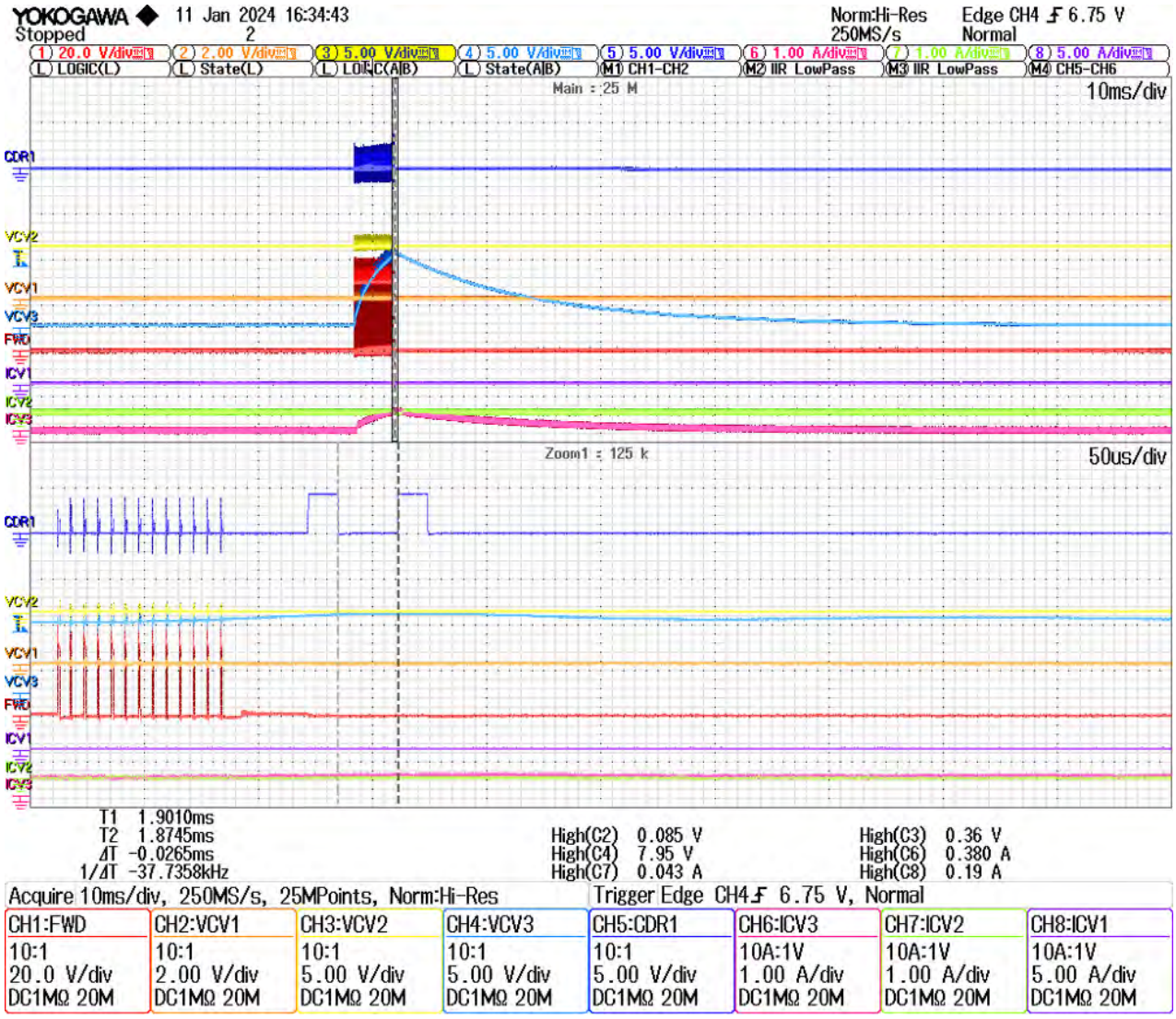



**Figure 66 –** Start-up With FB3 Open. Line Input 265 V, Full Load.

## *9.9 Component Peak Voltages*

### 9.9.1 SR FET Drain-Source Voltage


**Figure 67 –** SR FET(Q1) $V_{DS}$ Voltage Under Full Load at 265 VAC.

Ch1: $V_{SR}$, Ch5: $SR_{GATE}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum D-S voltage across the SR FET is 53 V.


**Figure 68 –** SR FET(Q1) $V_{DS}$ Voltage Under at Start-up at 265 VAC.

Ch1: $V_{SR}$, Ch5: $SR_{GATE}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum D-S voltage across the SR FET is 48 V.


**Figure 69 –** SR FET(Q1) $V_{DS}$ Voltage Under Full Load at 90 VAC.

Ch1: $V_{SR}$, Ch5: $SR_{GATE}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum D-S voltage across the SR FET is 23 V.


**Figure 70 –** SR FET(Q1) $V_{DS}$ Voltage at Start-up at 90 VAC.

Ch1: $V_{SR}$, Ch5: $SR_{GATE}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum D-S voltage across the SR FET 17.6 V.

### 9.9.2 CV1 Selection FET Drain-Source Voltage


**Figure 71 –** CV1 Selection FET (Q2) D-S Voltage Under Full Load at 265 VAC.

Ch1: $V_{CV1DRAIN}$, Ch2: $V_{CV1}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, $Ch_M1$: $V_{DS\_CV1}$

The maximum D-S voltage across the selection FET of CV1 is 17.7 V.

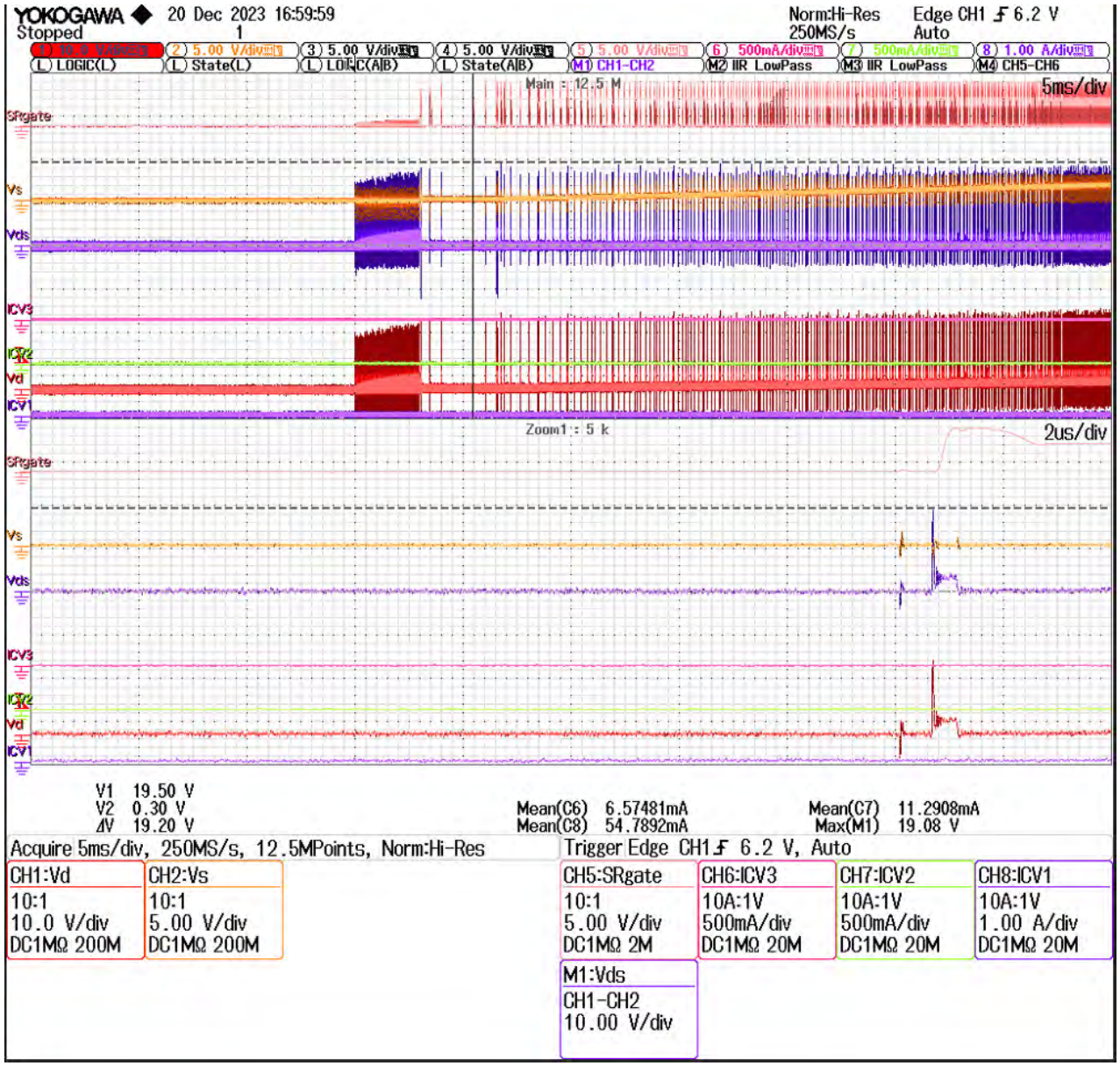



**Figure 72 –** CV1 Selection FET (Q2) D-S Voltage at Start-up at 265 VAC.

Ch1: $V_{CV1DRAIAN}$, Ch2: $V_{CV1}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV1}$

The maximum D-S voltage across the selection FET of CV1 is 19.5 V.


**Figure 73 –** CV1 Selection FET (Q2) D-S Voltage Under Full Load at 90 VAC.

Ch1: $V_{CV1DRAIN}$, Ch2: $V_{CV1}$, Ch5: $SR_{GATE}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV1}$

The maximum D-S voltage across the selection FET of CV1 is 10.7 V.

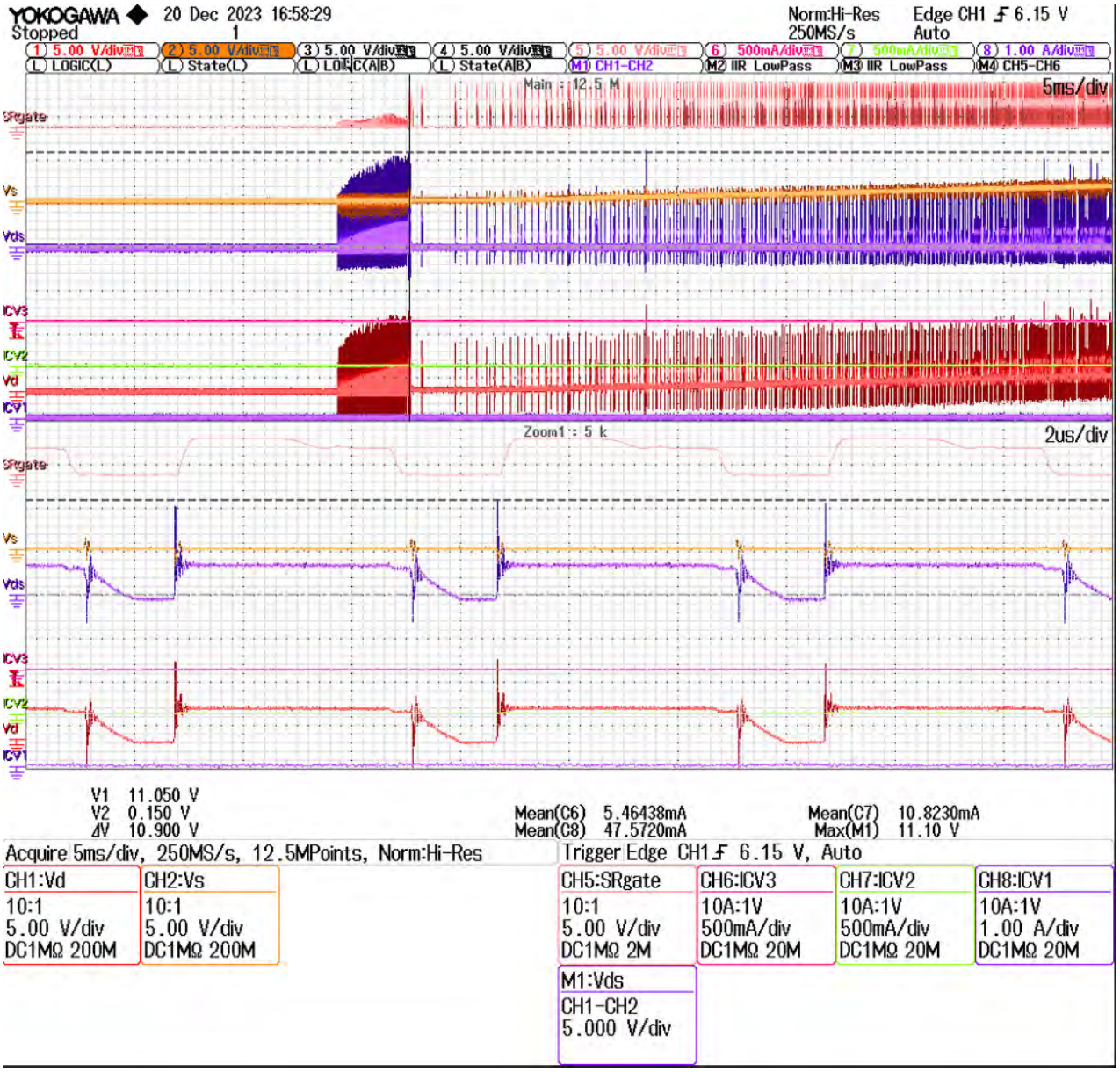



**Figure 74 –** CV1 Selection FET (Q2) D-S Voltage at Start-up at 90 VAC.

Ch1: $V_{CV1DRAIN}$, Ch2: $V_{CV1}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV1}$

The maximum D-S voltage across the selection FET of CV1 is 11 V.

### 9.9.3 CV2 Selection FET Drain-Source Voltage

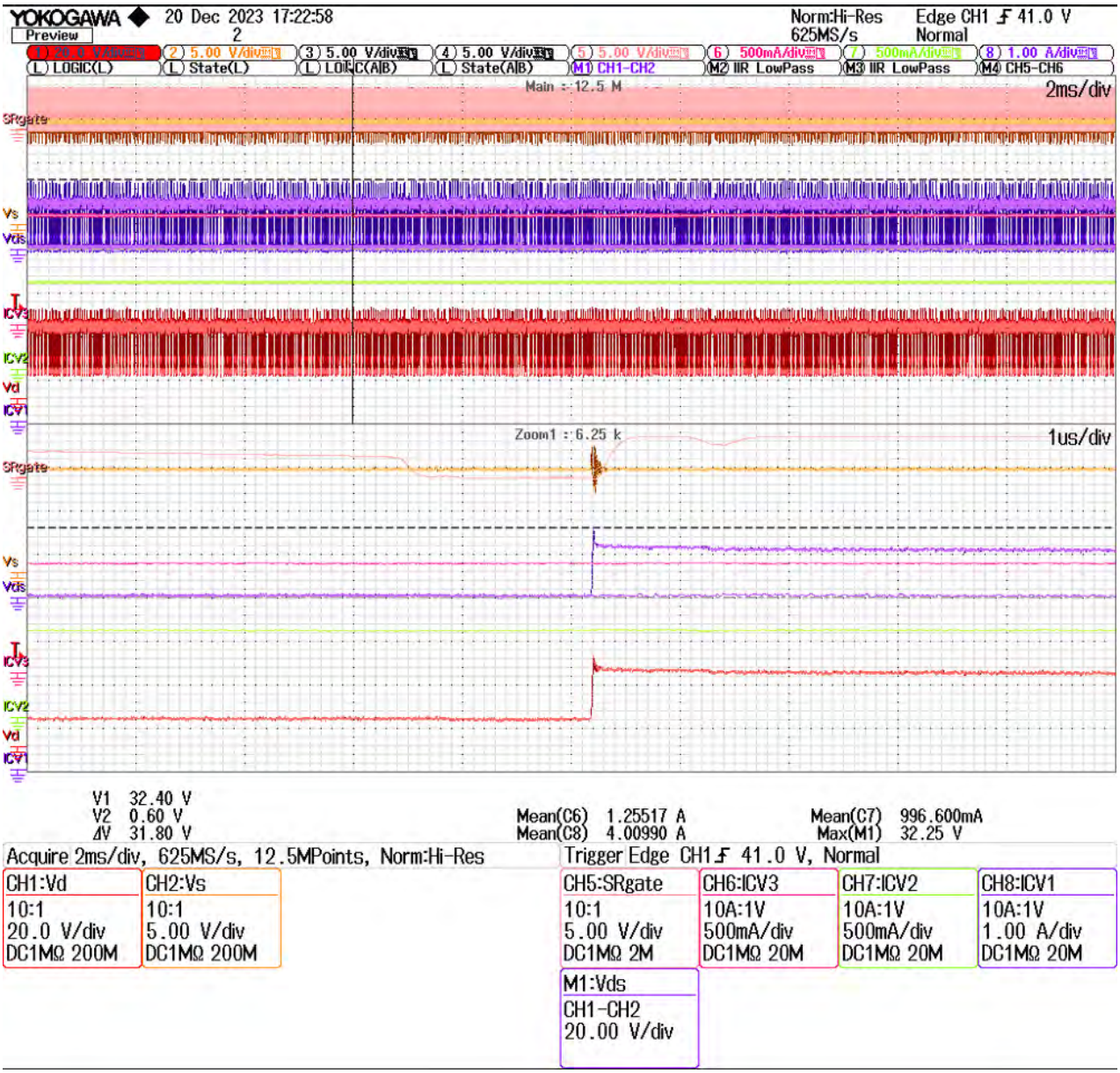



**Figure 75 –** CV2 Selection FET (Q4) D-S Voltage Under Full Load at 265 VAC.

Ch1: $V_{CV2DRAIN}$, Ch2: $V_{CV2}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV2}$

The maximum D-S voltage across the selection FET of CV2 is 32.2 V.

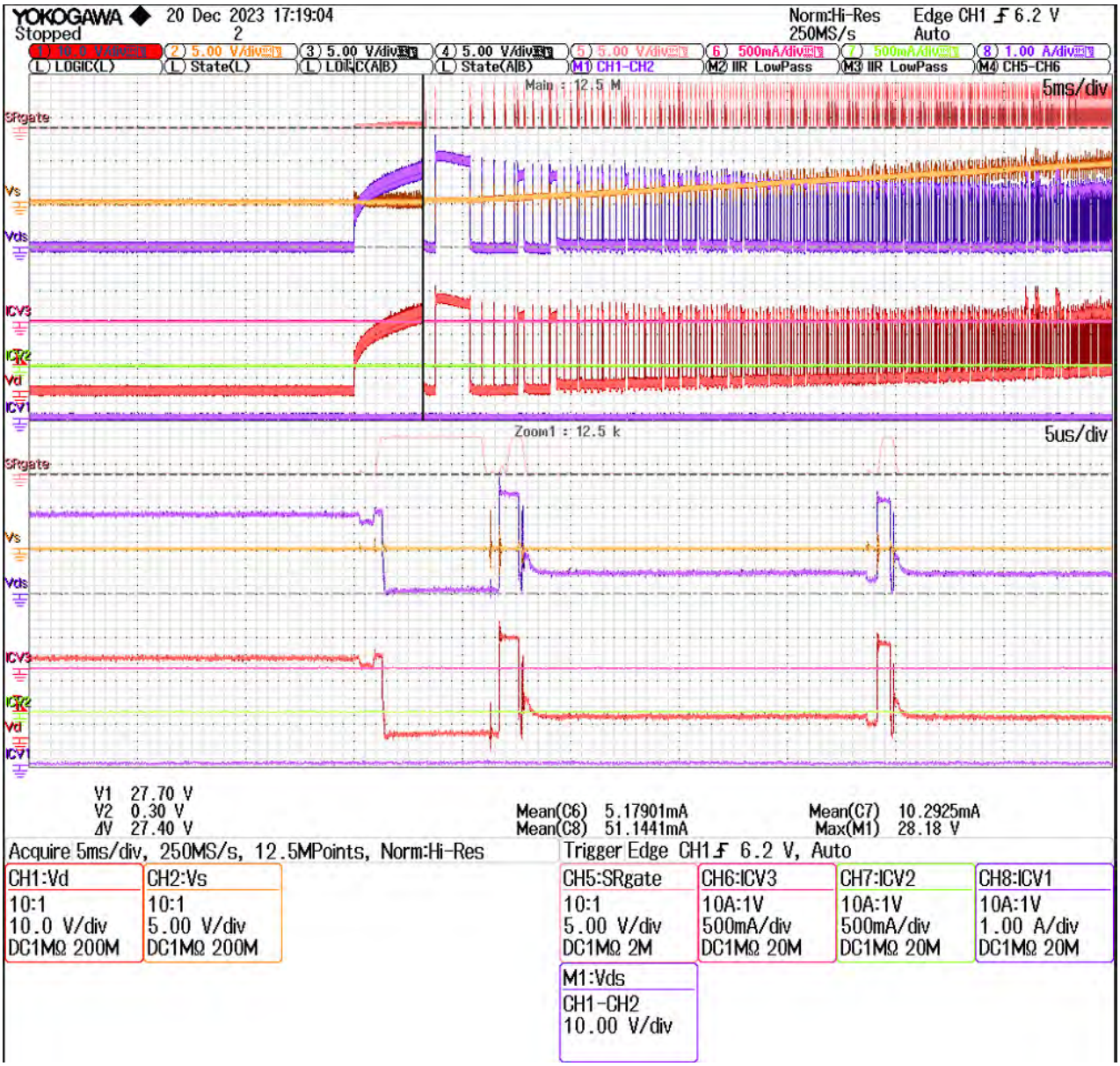



**Figure 76 –** CV2 Selection FET (Q4) D-S Voltage at Start-up at 265 VAC.

Ch1: $V_{CV2drain}$, Ch2: $V_{CV2}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV2}$

The maximum D-S voltage across the selection FET of CV2 is 28.2 V.

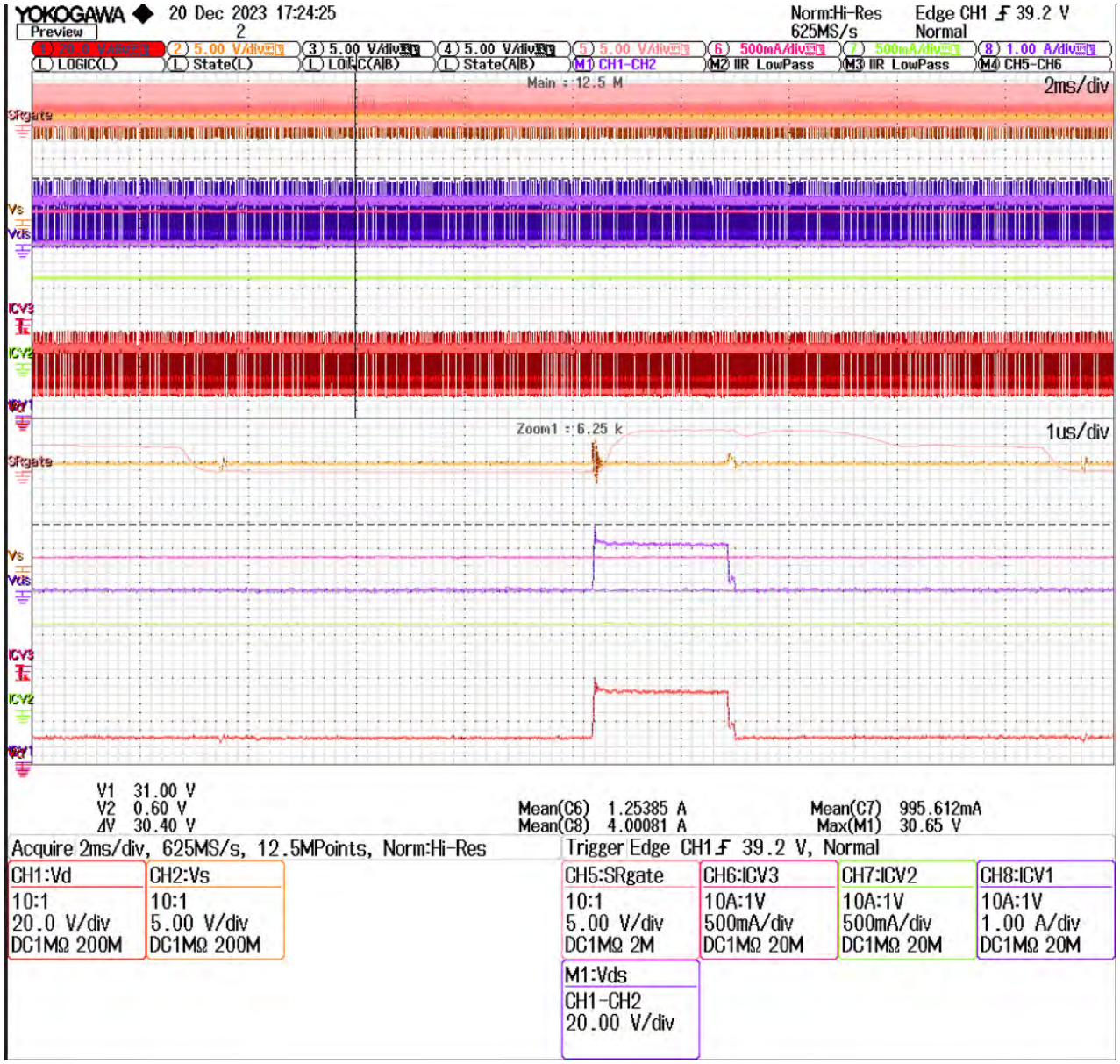



**Figure 77 –** CV2 Selection FET (Q4) D-S Voltage Under Full Load at 90 VAC.

Ch1: $V_{CV2DRAIN}$, Ch2: $V_{CV2}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV2}$

The maximum D-S voltage across the selection FET of CV2 is 30.7 V.

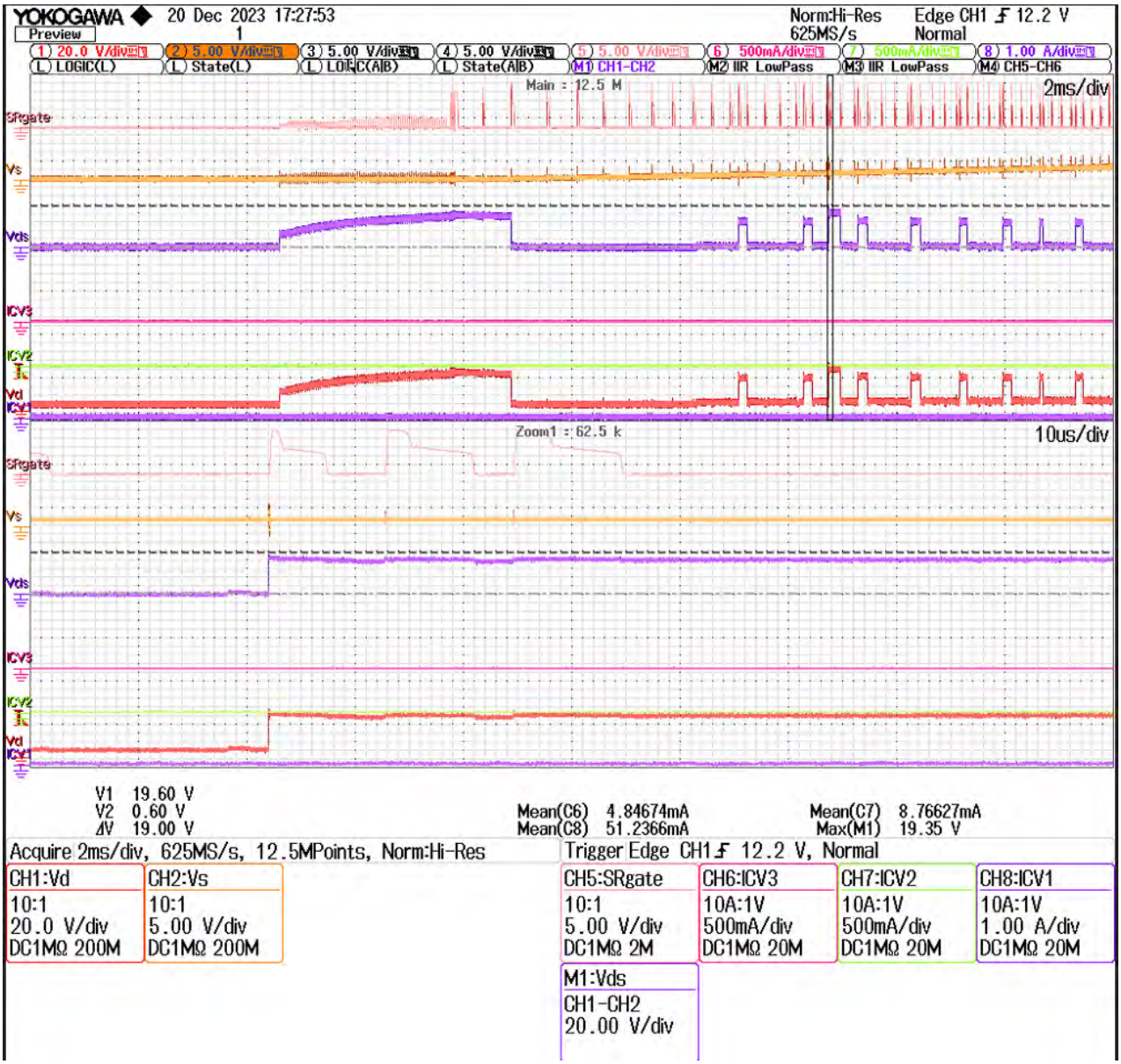



**Figure 78 –** CV2 Selection FET (Q4) D-S Voltage at Start-up at 90 VAC.

Ch1: $V_{CV2DRAIN}$, Ch2: $V_{CV2}$, Ch5: $SR_{GATE}$,
Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, ChM1: $V_{DS\_CV2}$

The maximum D-S voltage across the selection FET of CV2 is 19.3 V.

### 9.9.4 CV2 Rectifier Diode Reverse Voltage

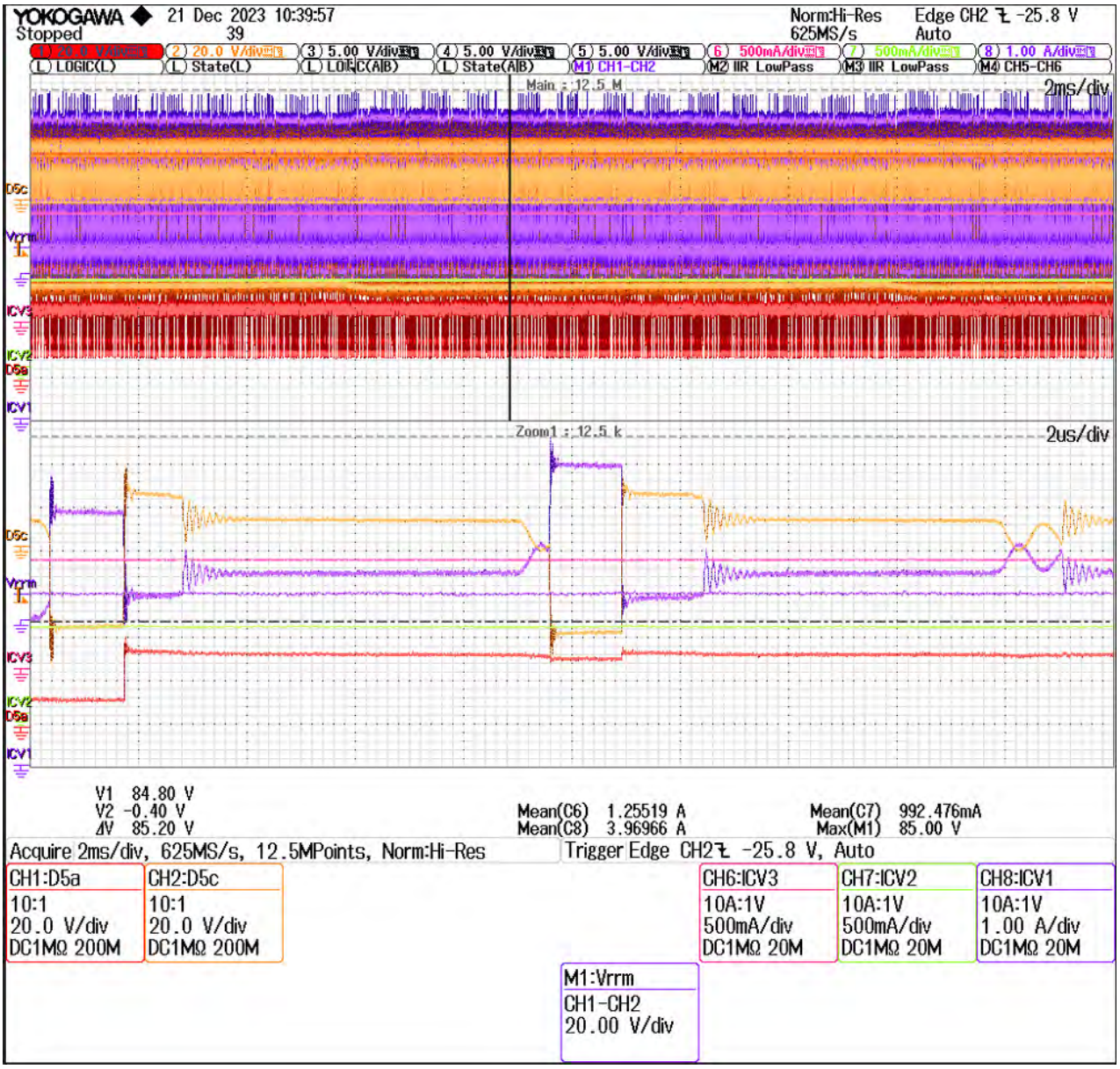



**Figure 79 –** CV2 Rectifier Diode Reverse Voltage Under Full Load at 265 VAC.

Ch1: $D5_A$, Ch2: $D5_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 85 V.

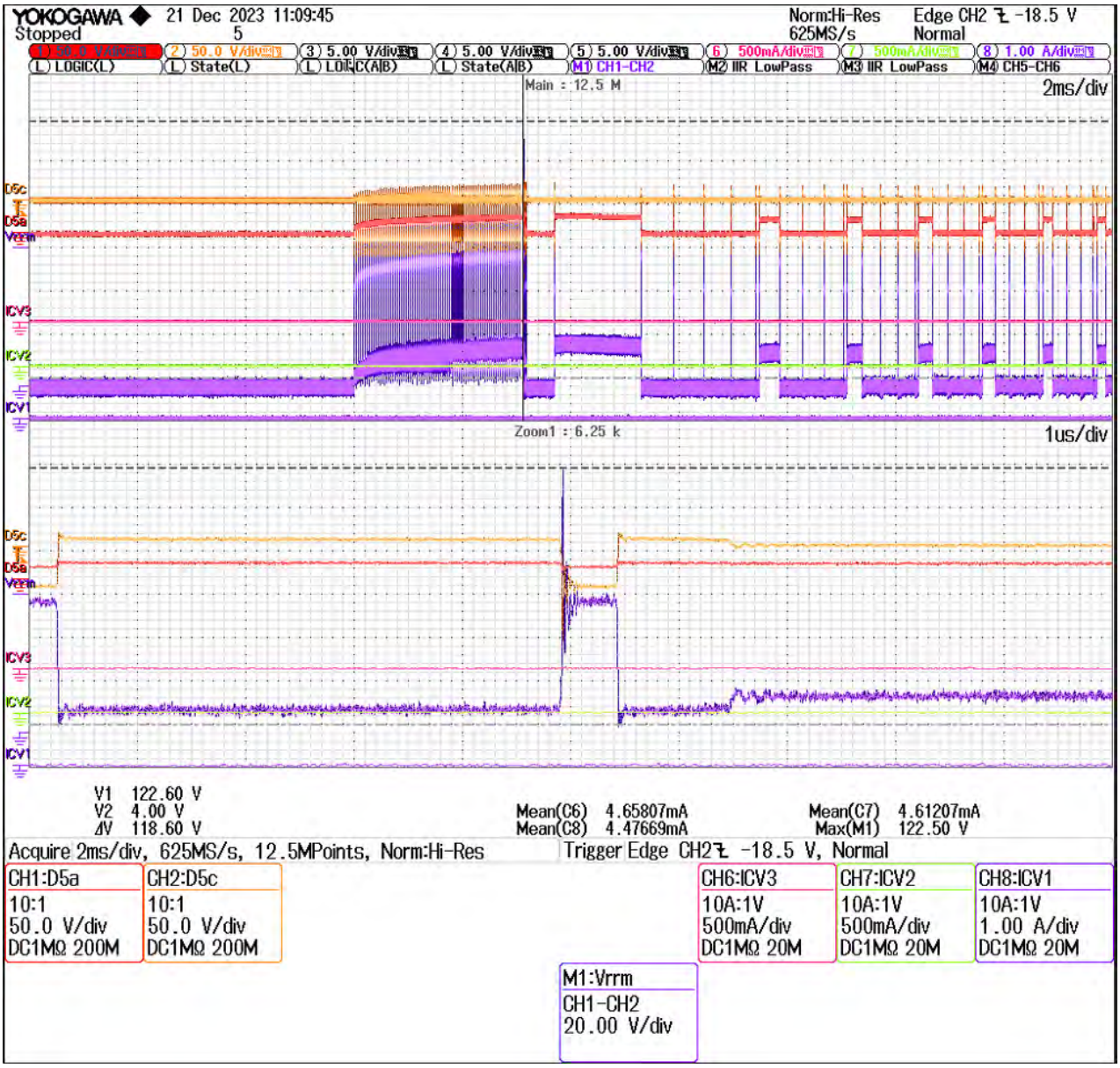



**Figure 80 –** CV2 Rectifier Diode Reverse Voltage at Start-up at 265 VAC.

Ch1: $D5_A$, Ch2: $D5_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 123 V.


**Figure 81 –** CV2 Rectifier Diode Reverse Voltage Under Full Load at 90 VAC.

Ch1: $D5_A$, Ch2: $D5_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 52 V.


**Figure 82 –** CV2 Rectifier Diode Reverse Voltage at Start-up at 90 VAC.

Ch1: $D5_A$, Ch2: $D5_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 51 V.

### 9.9.5 CV3 Rectifier Diode Reverse Voltage

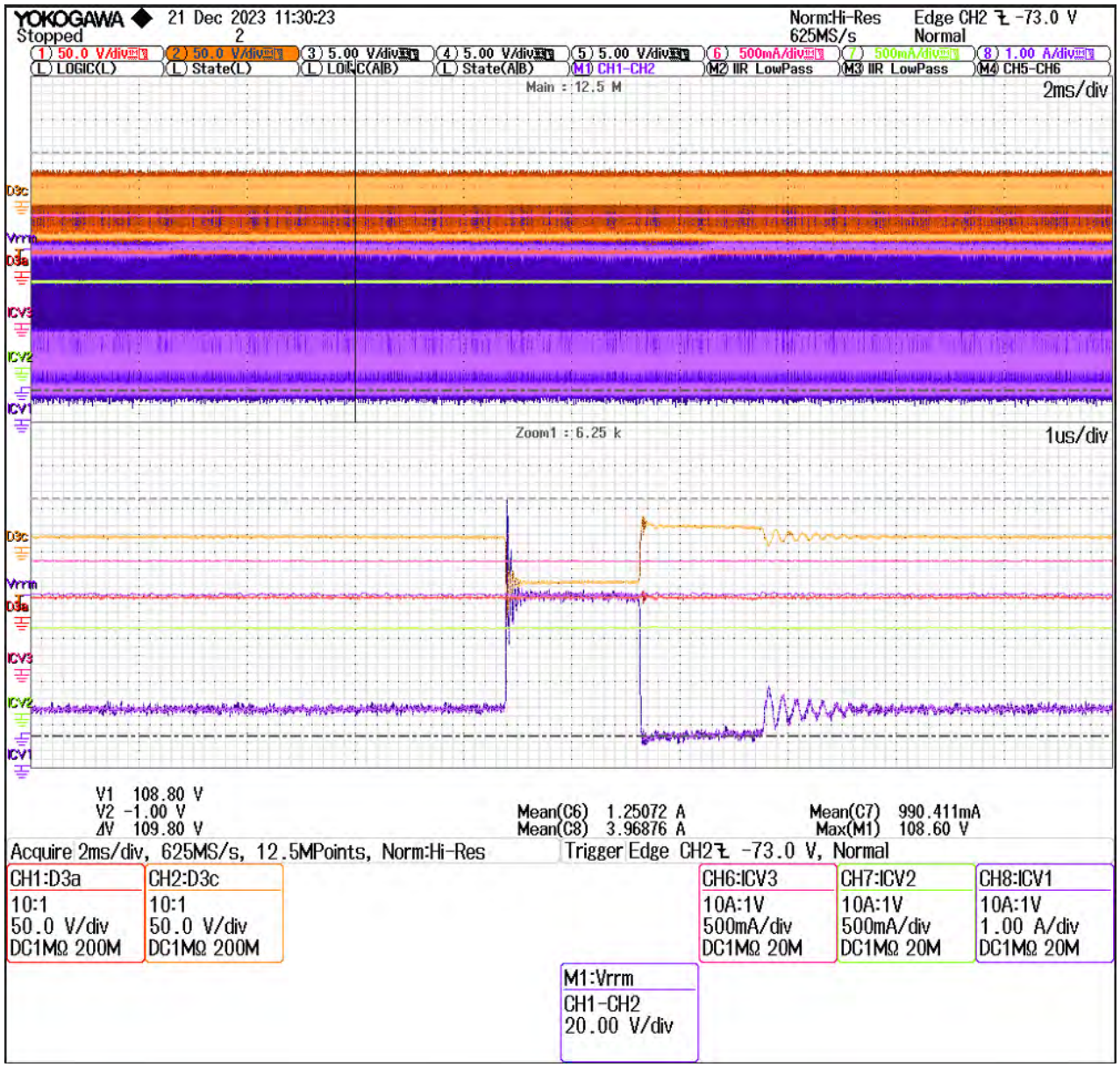



**Figure 83 –** CV3 Rectifier Diode Reverse Voltage Under Full Load at 265 VAC.
Ch1: $D3_A$, Ch2: $D3_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 109 V.

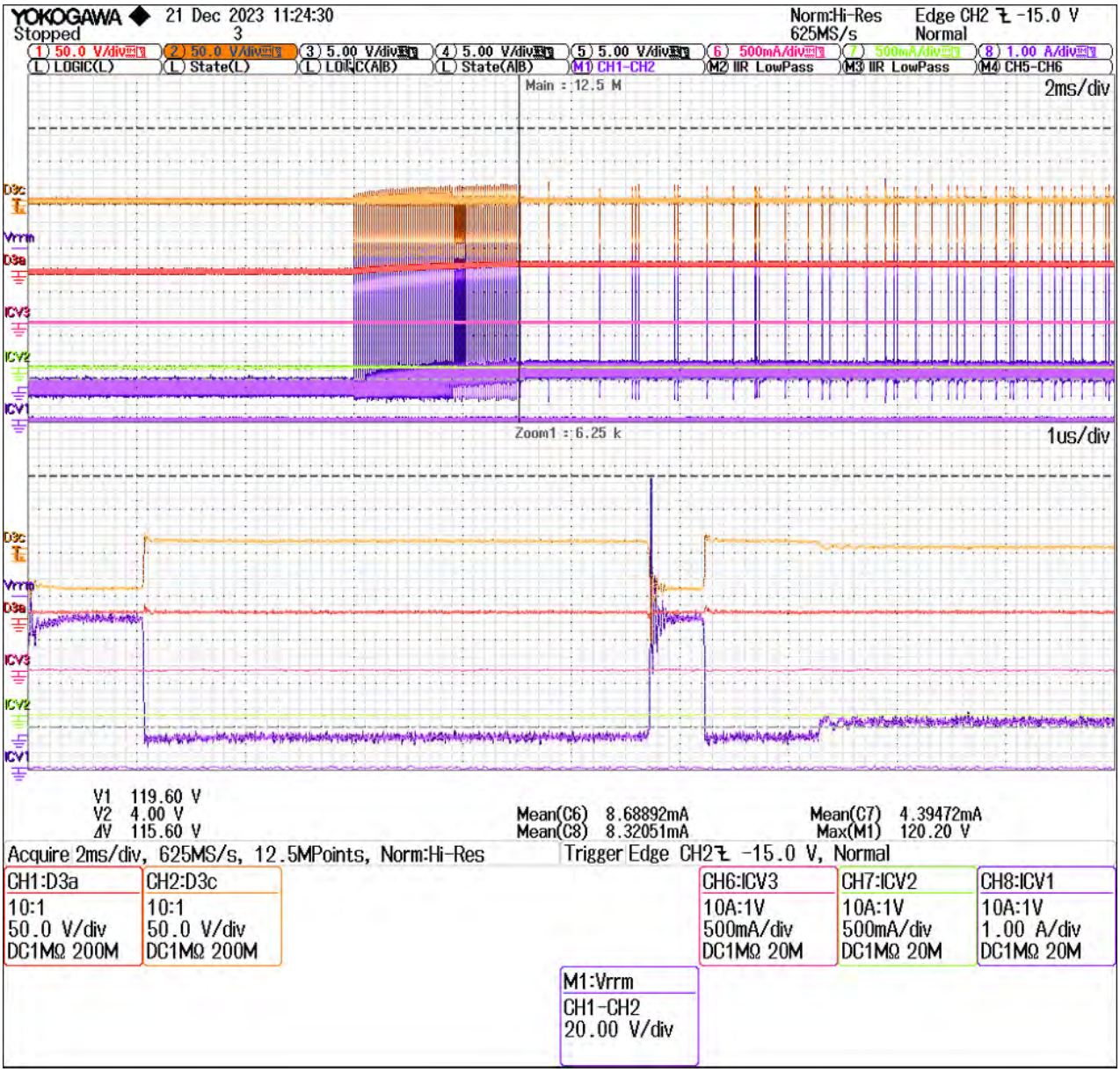



**Figure 84 –** CV3 Rectifier Diode Reverse Voltage at Start-up at 265 VAC.

Ch1: $D3_A$, Ch2: $D3_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 120 V.

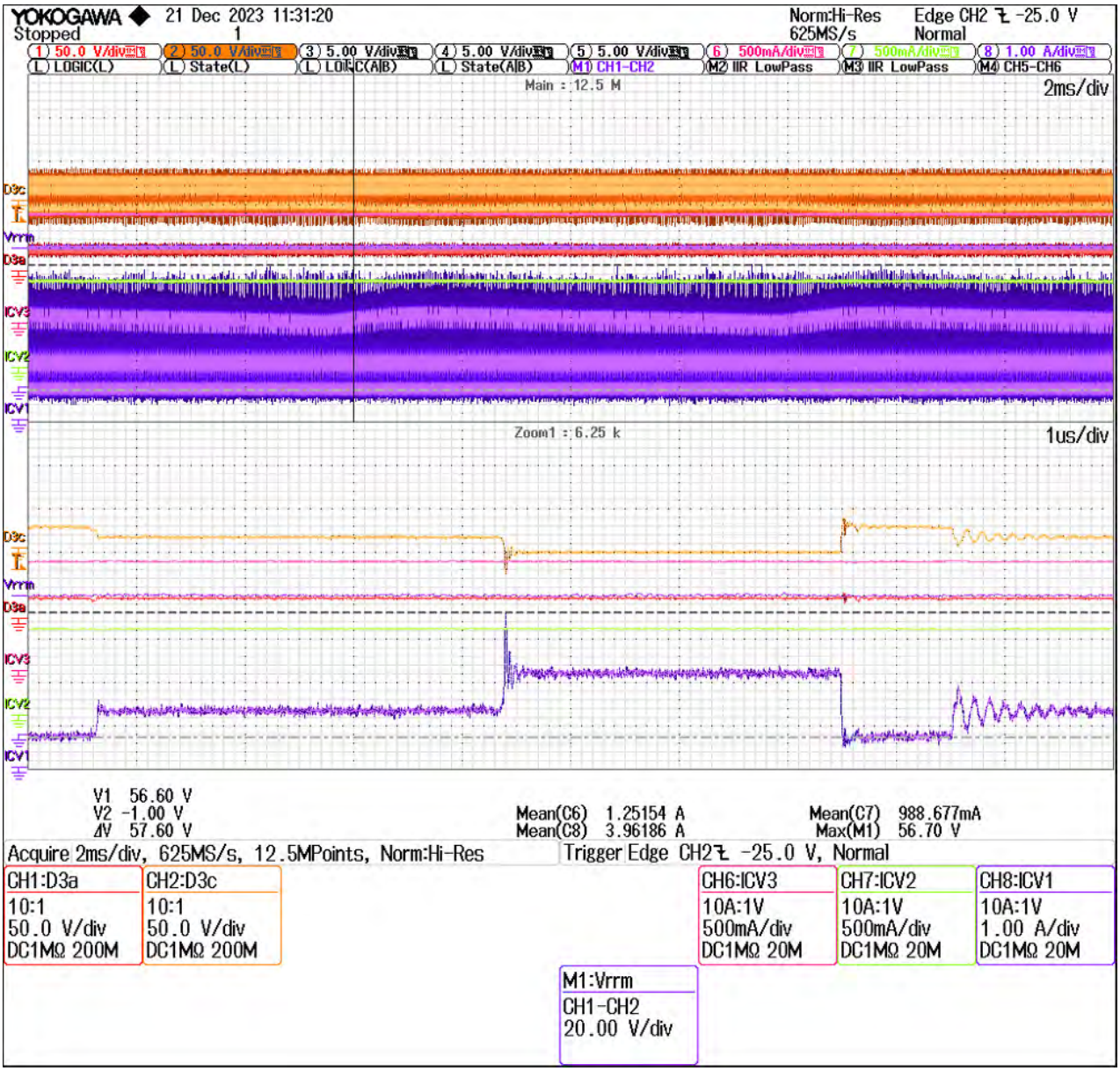



**Figure 85 –** CV3 Rectifier Diode Reverse Voltage Under Full Load at 90 VAC.

Ch1: $D3_A$, Ch2: $D3_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 57 V.

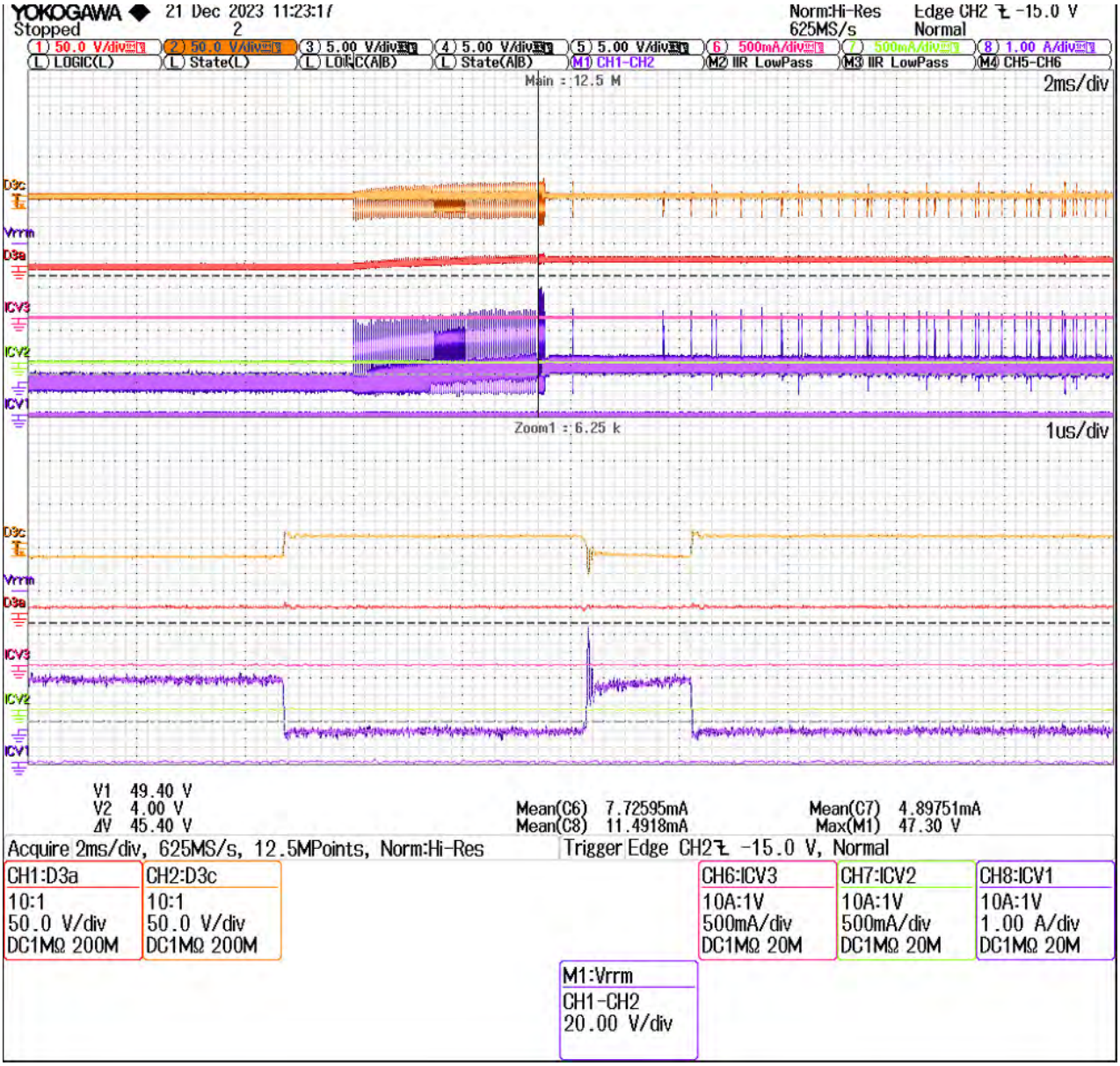



**Figure 86 –** CV3 Rectifier Diode Reverse Voltage at Start-up at 90 VAC.

Ch1: $D3_A$, Ch2: $D3_C$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$, M1: $V_{RRM}$

Maximum reverse voltage across the CV2 rectifier diode is 47 V.

### 9.9.6 Bias Winding Rectifier Diode Reverse Voltage

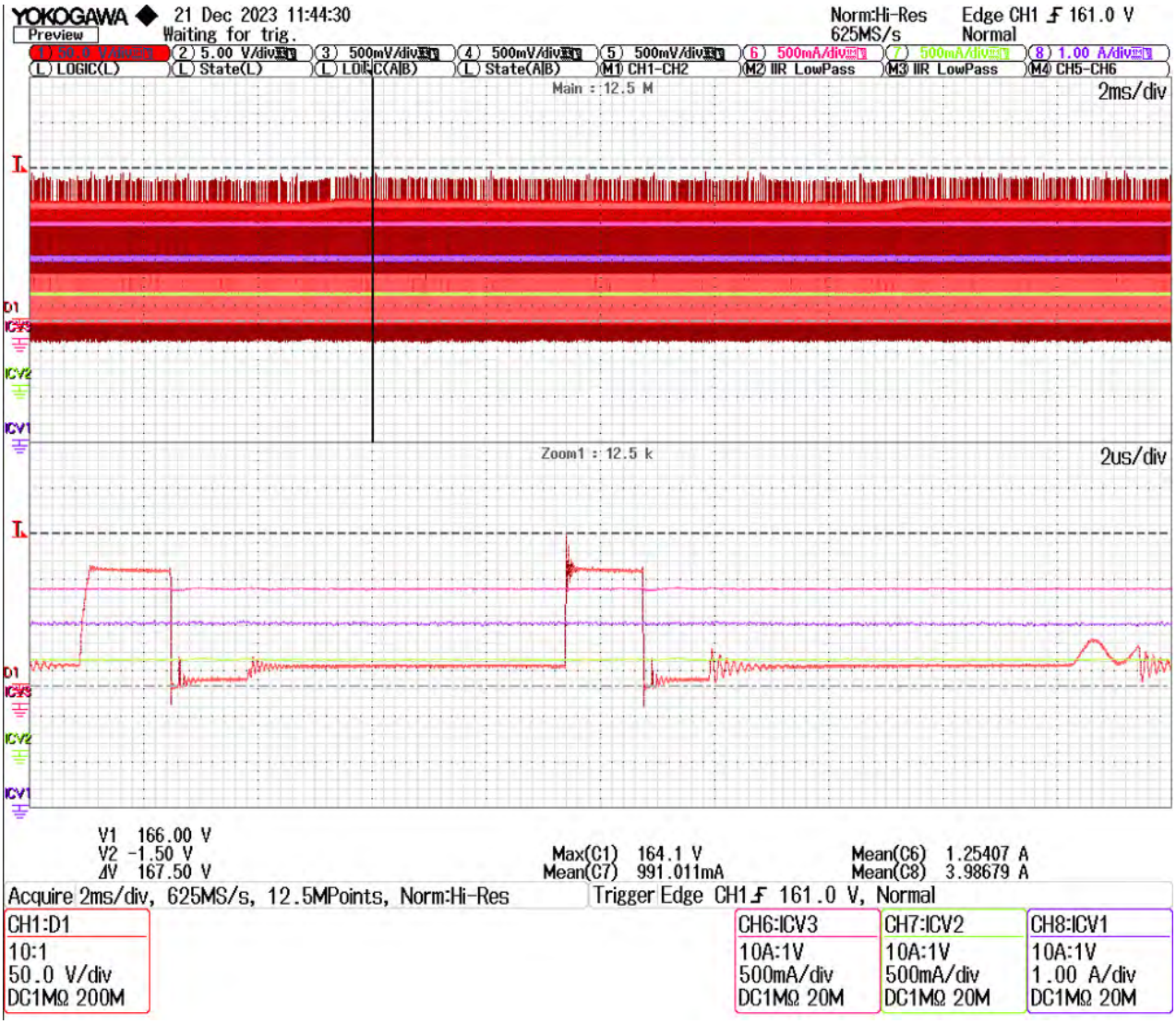



**Figure 87 –** AUX Rectifier Diode Reverse Voltage Under Full Load at 265 VAC.

Ch1: $D1_{RRM}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum reverse voltage across the AUX winding rectifier diode is 166 V.


**Figure 88 –** AUX Rectifier Diode Reverse Voltage at Start-up at 265 VAC.

Ch1: $D1_{RMM}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum reverse voltage across the AUX winding rectifier diode is 154 V.


**Figure 89 –** AUX Rectifier Diode Reverse Voltage Under Full Load at 90 VAC.

Ch1: $D1_{RMM}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum reverse voltage across the AUX winding rectifier diode is 94 V.


**Figure 90 –** AUX Rectifier Diode Reverse Voltage at Start-up at 90 VAC.

Ch1: $D1_{RRM}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

Maximum reverse voltage across the AUX winding rectifier diode is 61 V.

## 9.10 Brown-Out and Brown-In

The brown-in and brown-out results were measured at full load on all outputs. The results are shown in the table below. Screenshots illustrating the tests are shown in Figures 88 and 89.

| Brown-Out Threshold | Brown-In Threshold |
|---|---|
| [$V_{RMS}$] | [$V_{RMS}$] |
| 63 | 73.4 |

Brown-In and Brown-Out Thresholds at Full power.

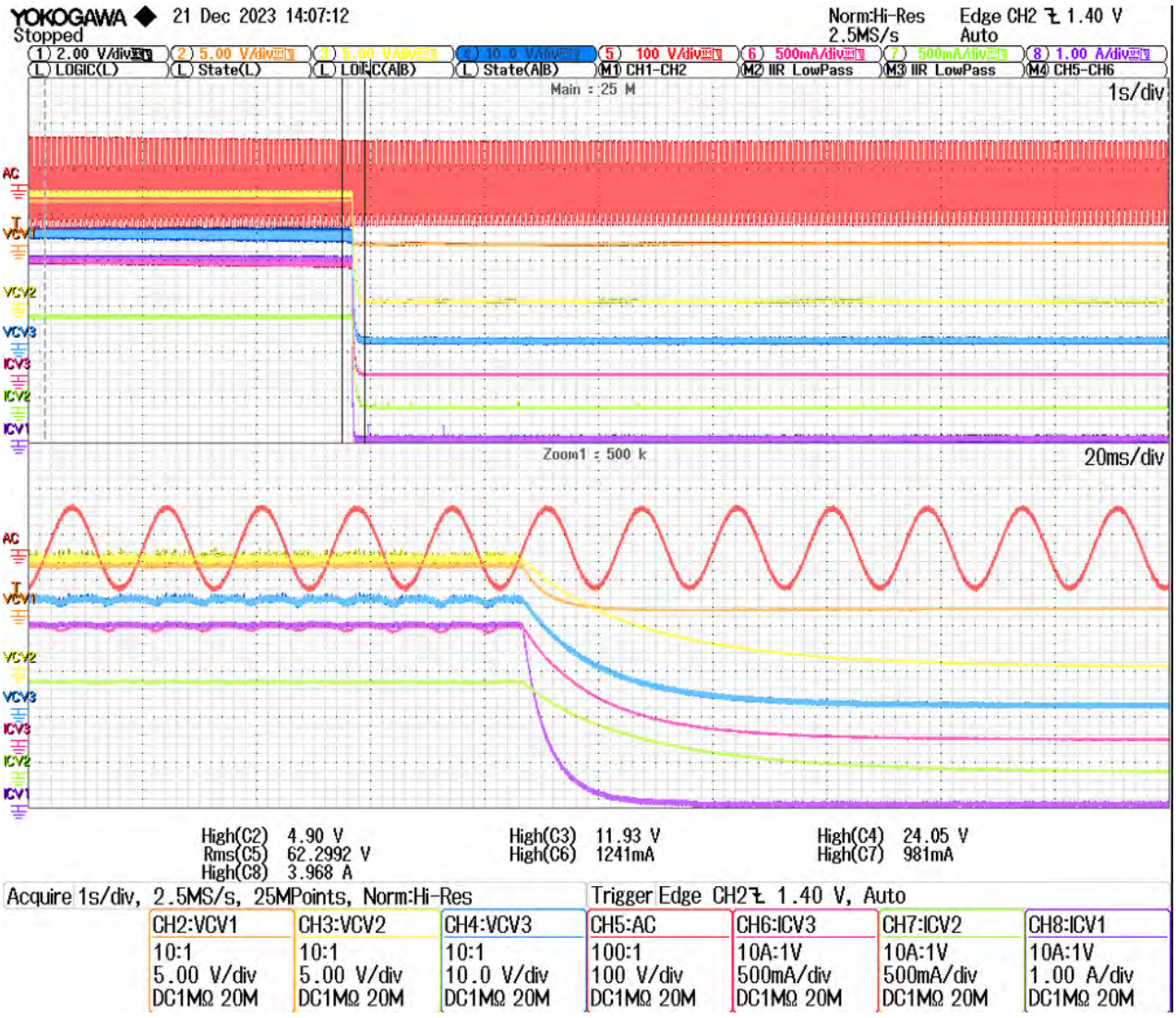



**Figure 91 –** Brown-Out Response at Full Power.

Ch2: $V_{CV1}$, Ch3: $V_{CV2}$, Ch4: $V_{CV3}$, Ch5: $V_{AC}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

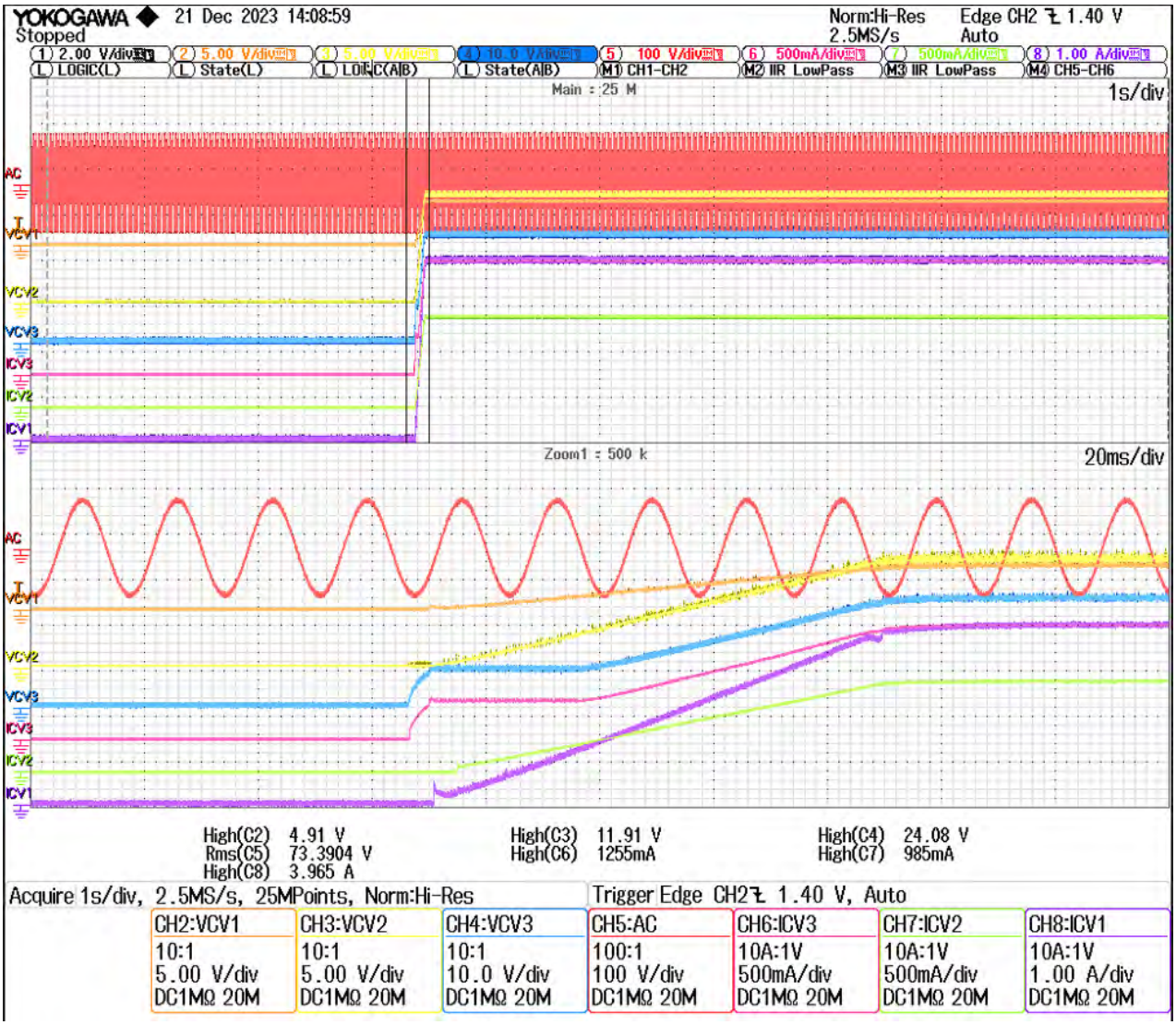



**Figure 92 –** Brown-In Response at Full Power.

Ch2: $V_{CV1}$, Ch3: $V_{CV2}$, Ch4: $V_{CV3}$, Ch5: $V_{AC}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

## *9.11 Output Protections*

### 9.11.1 CV Output Overvoltage Protection

The overvoltage protection threshold of the CV outputs was tested. Additional charge was injected into the output filter capacitor of the output under test until the converter went into a restart. The test was carried out at line voltages 90 V with full and no-load conditions.

In all cases of CV no-load and full-load, OV protection disables the system.

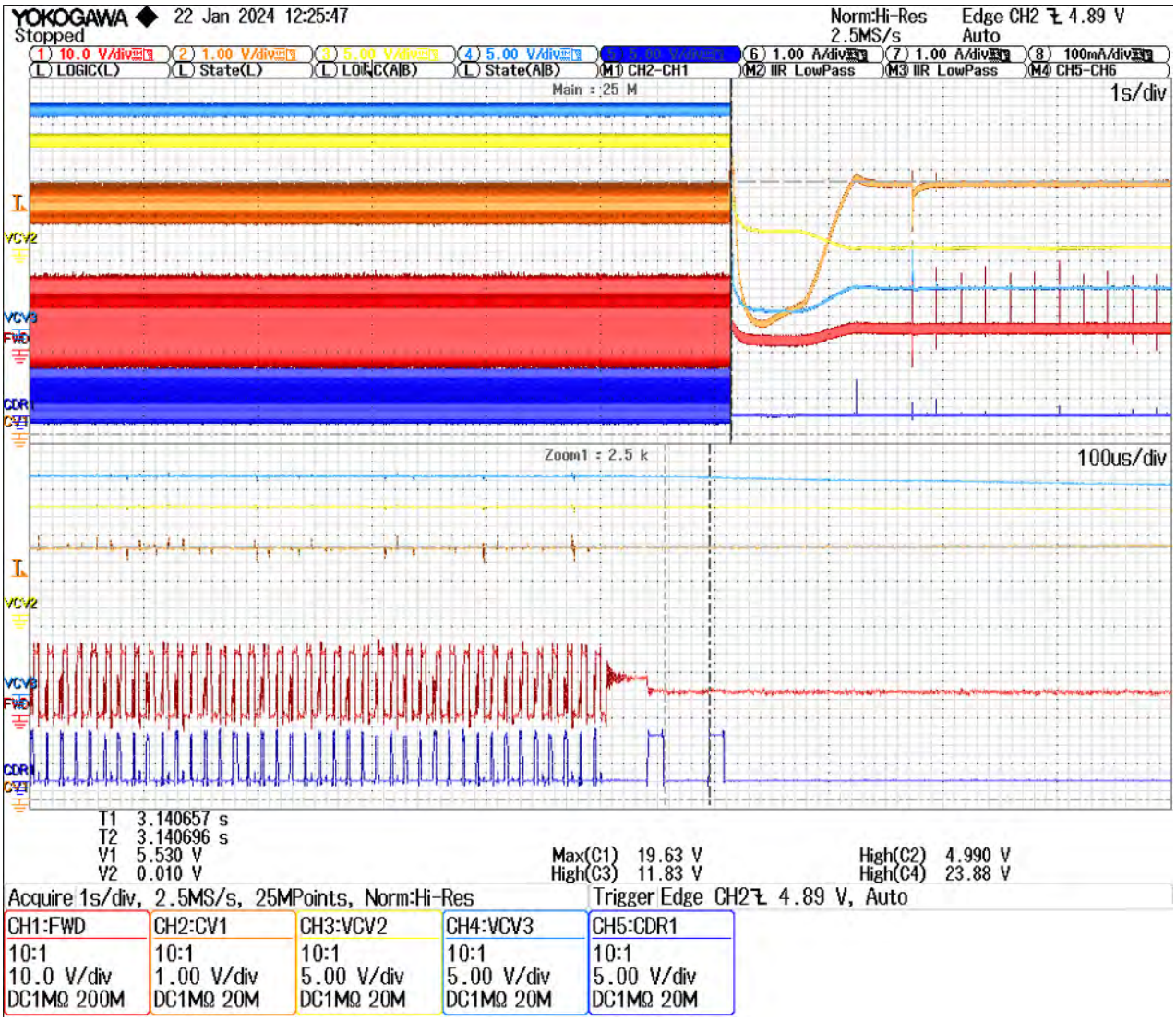



**Figure 93 –** CV1 OVP at Full CV2 and CV3 Load.

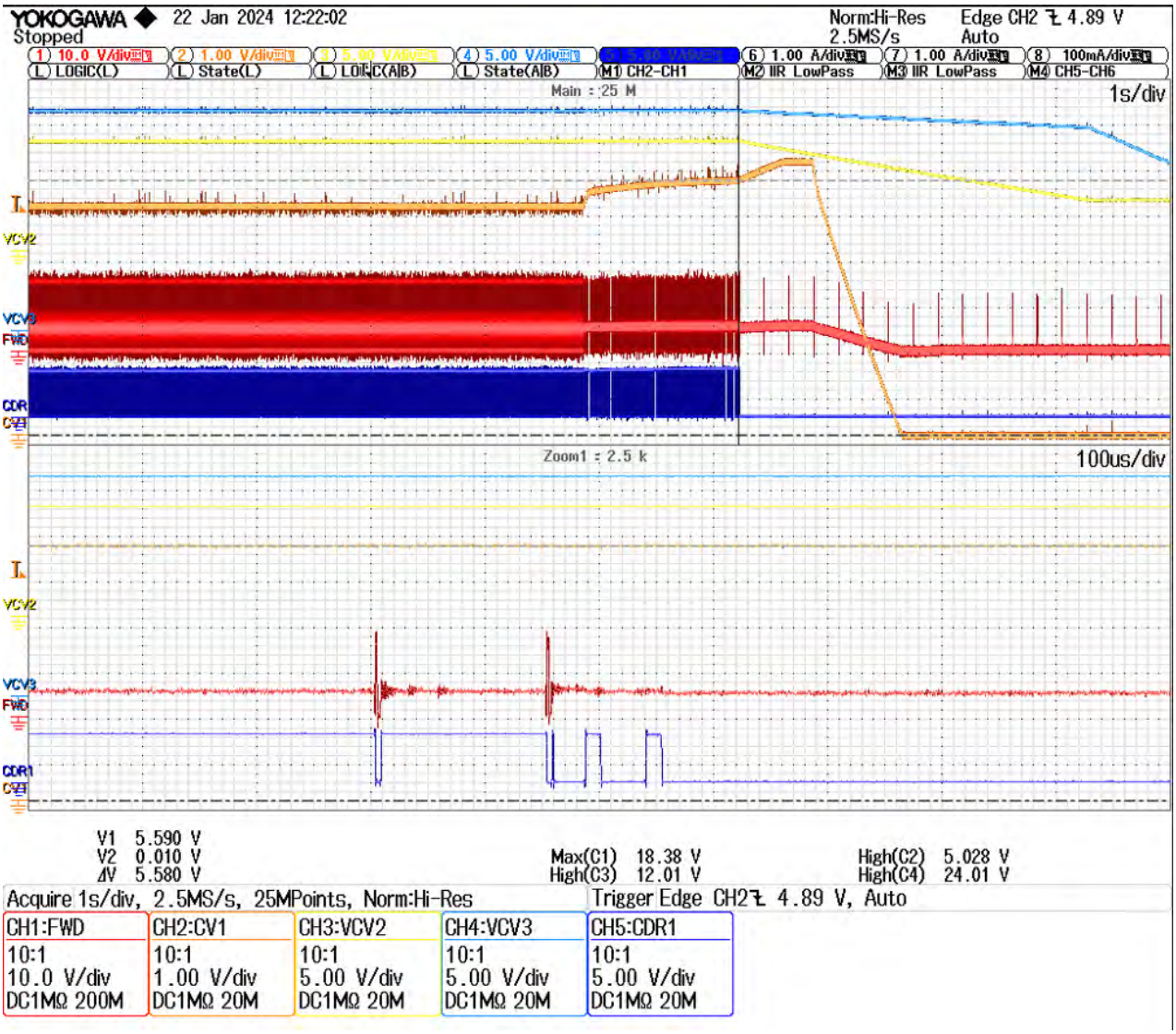



**Figure 94 –** CV1 OVP at No CV2 and CV3 Load.

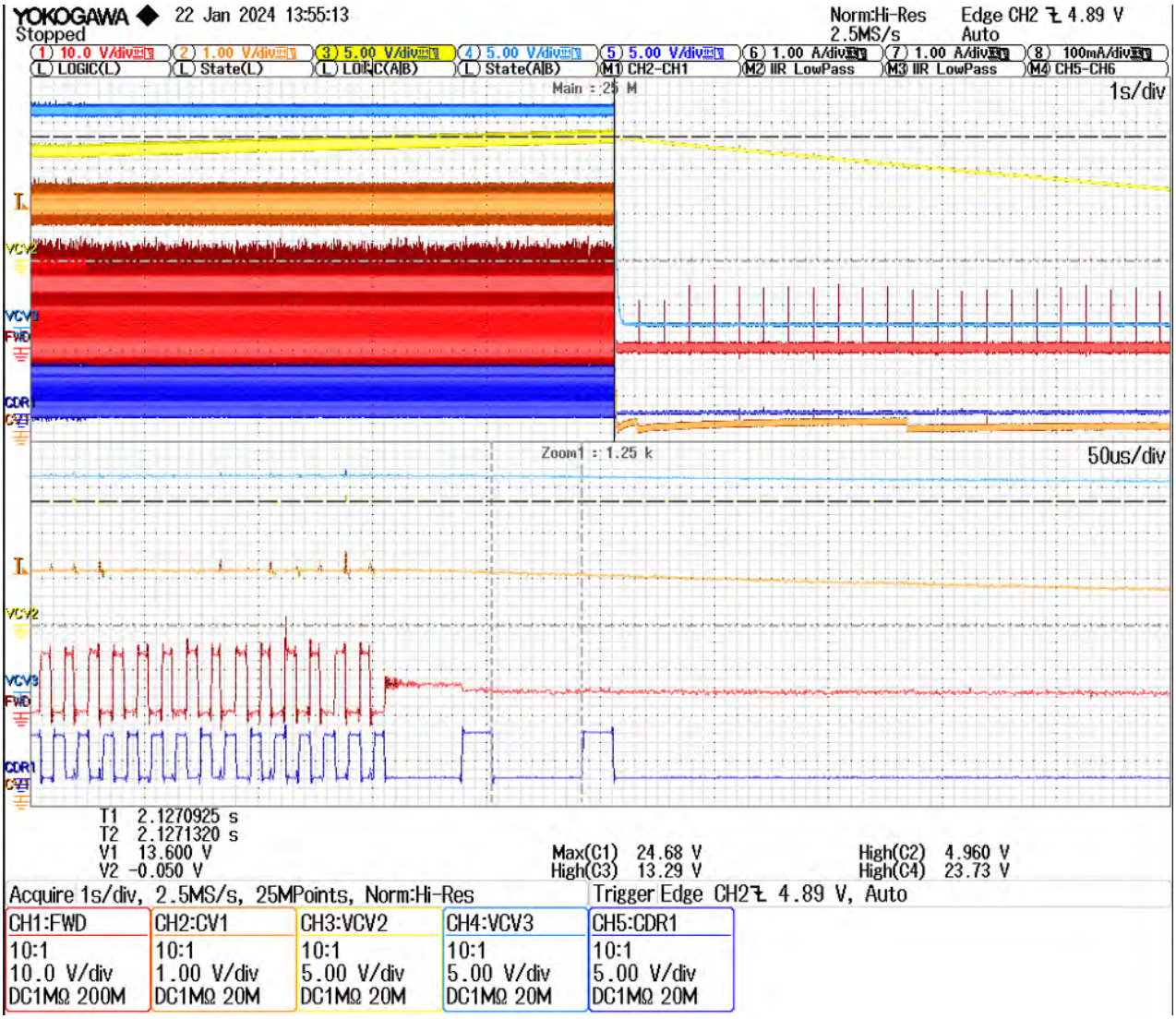



**Figure 95 –** CV2 OVP at Full CV1 and CV3 Load.

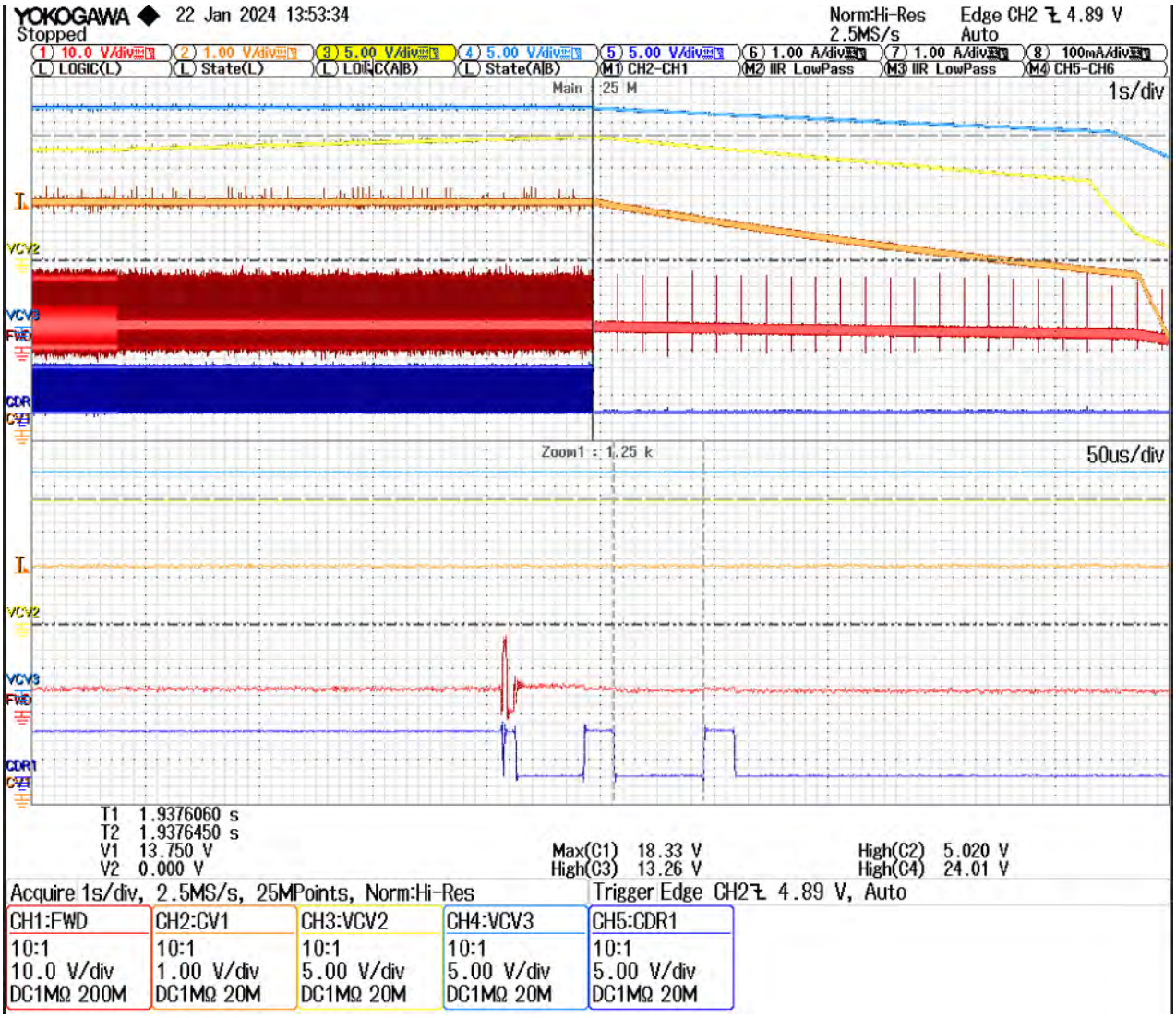



**Figure 96 –** CV2 OVP at No CV1 and CV3 Load.

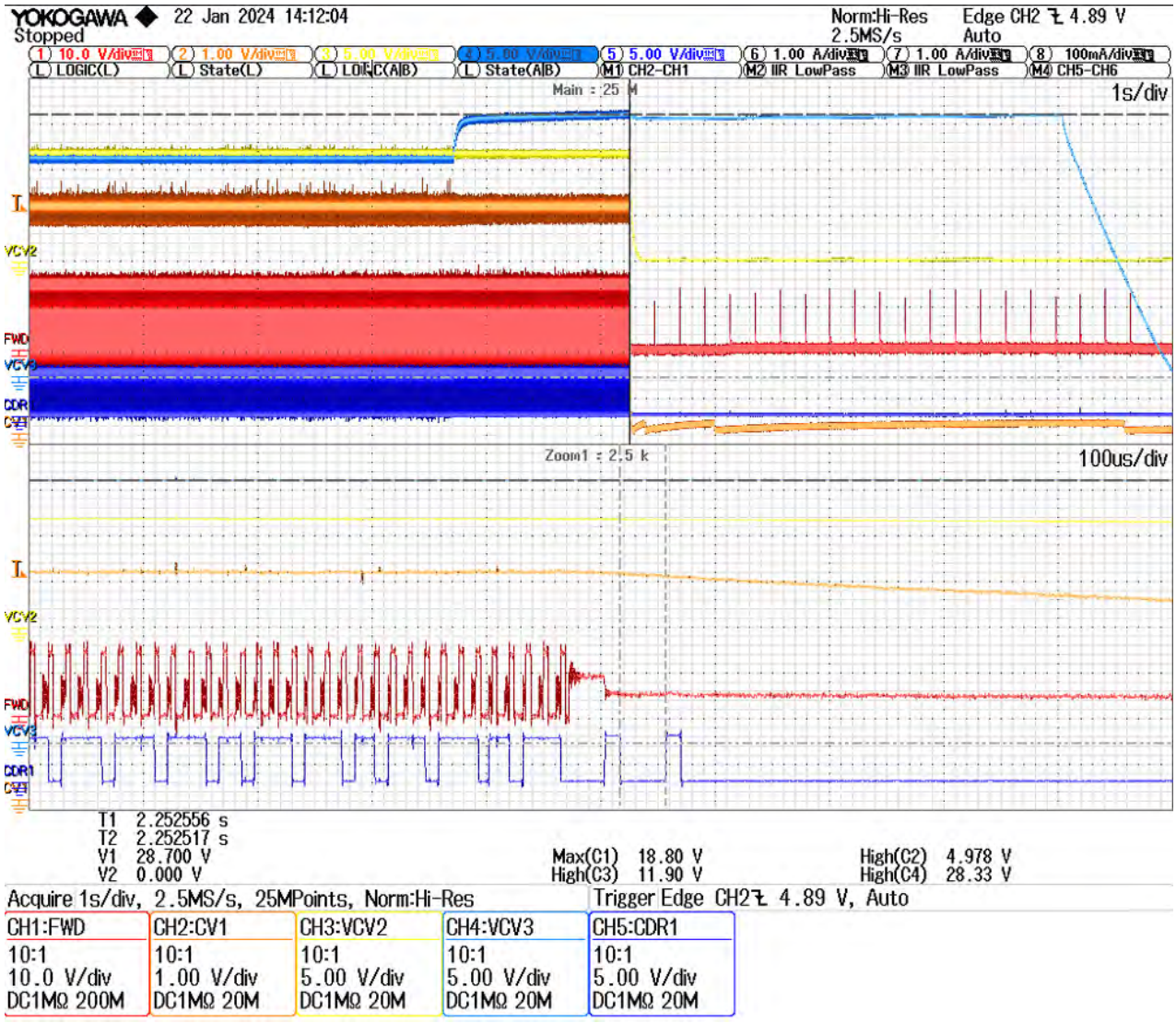



**Figure 97 –** CV3 OVP at Full CV1 and CV2 Load.

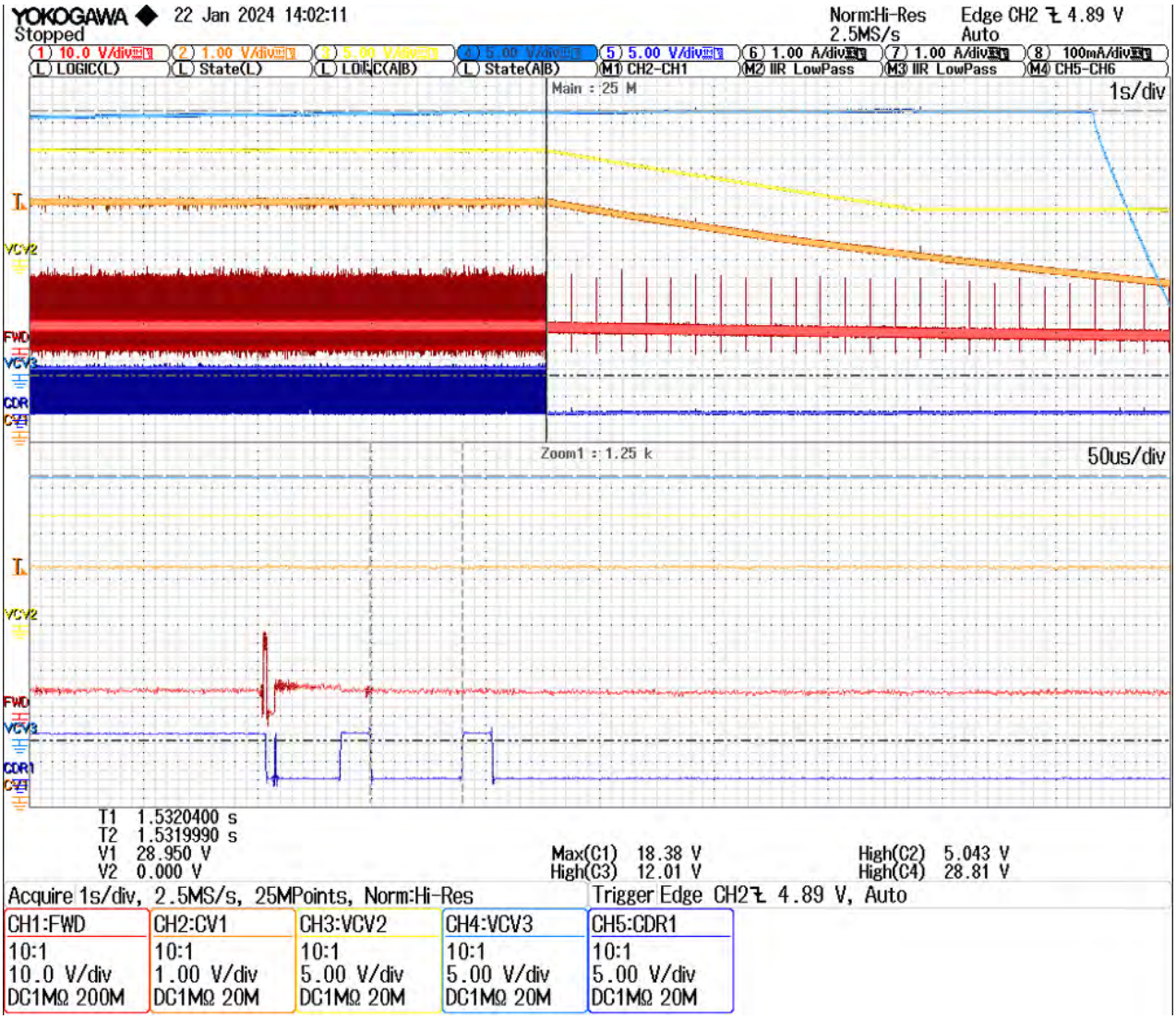



**Figure 98 –** CV3 OVP at No CV1 and CV2 Load.

### 9.11.2 Output Ripple Measurements

### 9.11.3 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to reduce noise pick-up. Details of the probe modification are provided below in Figure 96.

The probe adapter is shown below. It includes a coaxial cable with two parallel capacitors connected to the points of measurement. The capacitors include a ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.

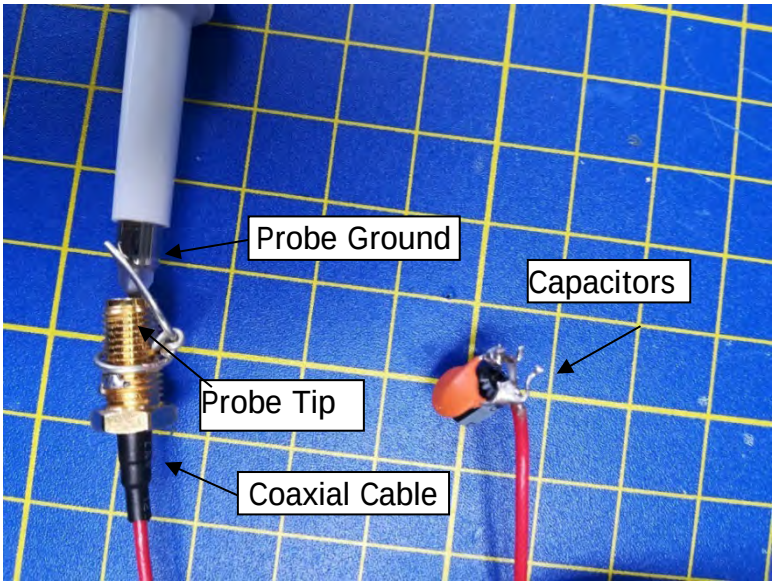



**Figure 99 –** Ripple Measurement Test Se-UP.

### 9.11.4 CV Output Ripple

- 90 VAC – 265 VAC
- Output CV1 = 5 V @ 20 W and output CV2 = 12 V @ 12 W and output CV3 = 24 V @ 30 W
- 20 MHz bandwidth in the scope

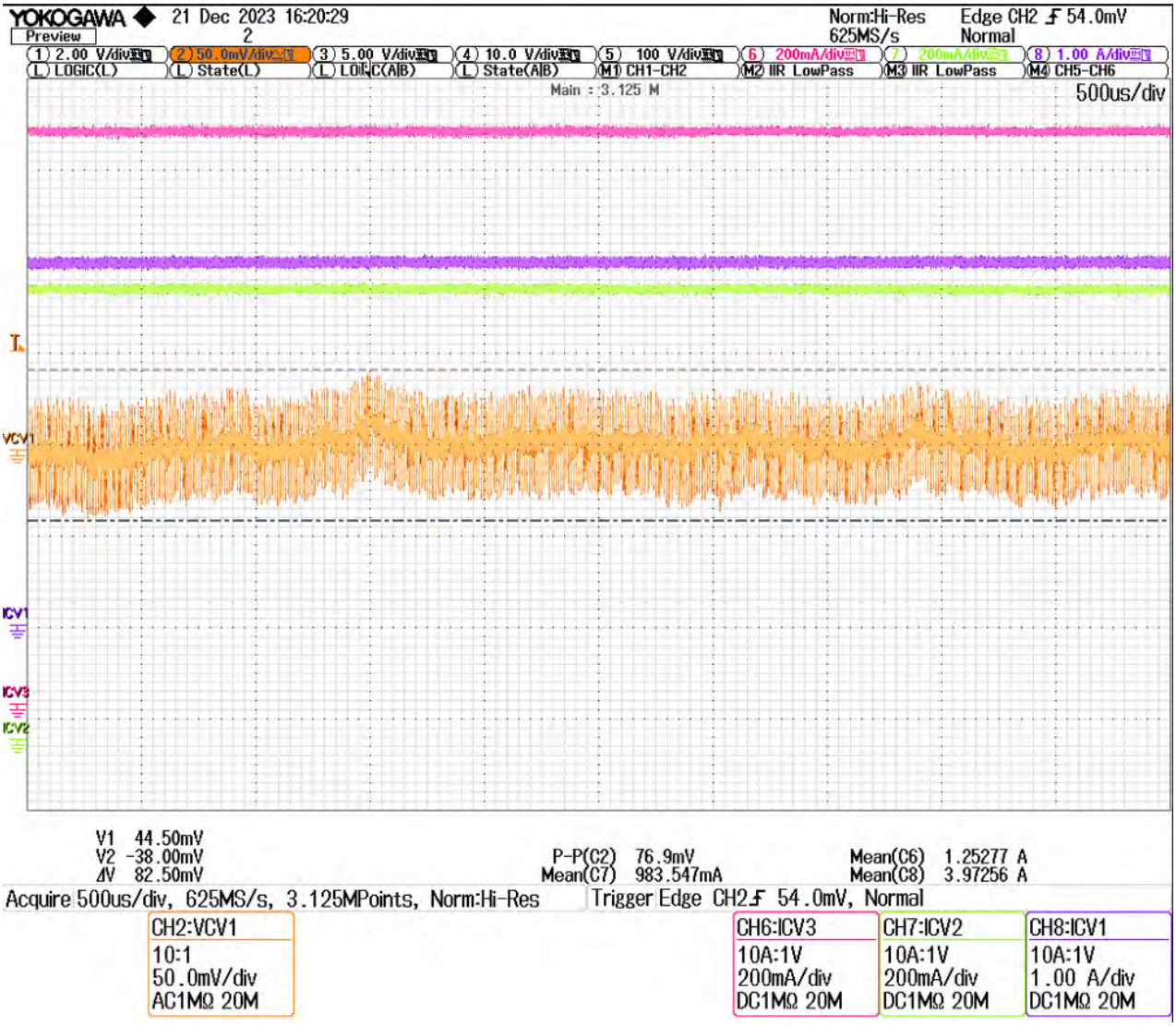



**Figure 100 –** VCV1 Ripple and Noise Under Nominal Load at 90 VAC.

Ch2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$


**Figure 101 –** VCV1 Ripple and Noise Under Nominal Load at 265 VAC.

Ch2: $V_{CV1}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

The worst-case ripple and noise at the CV1 output of the converter was measured as 80 $mV_{P-P}$ (<2%) at 20 MHz bandwidth at the connector output.

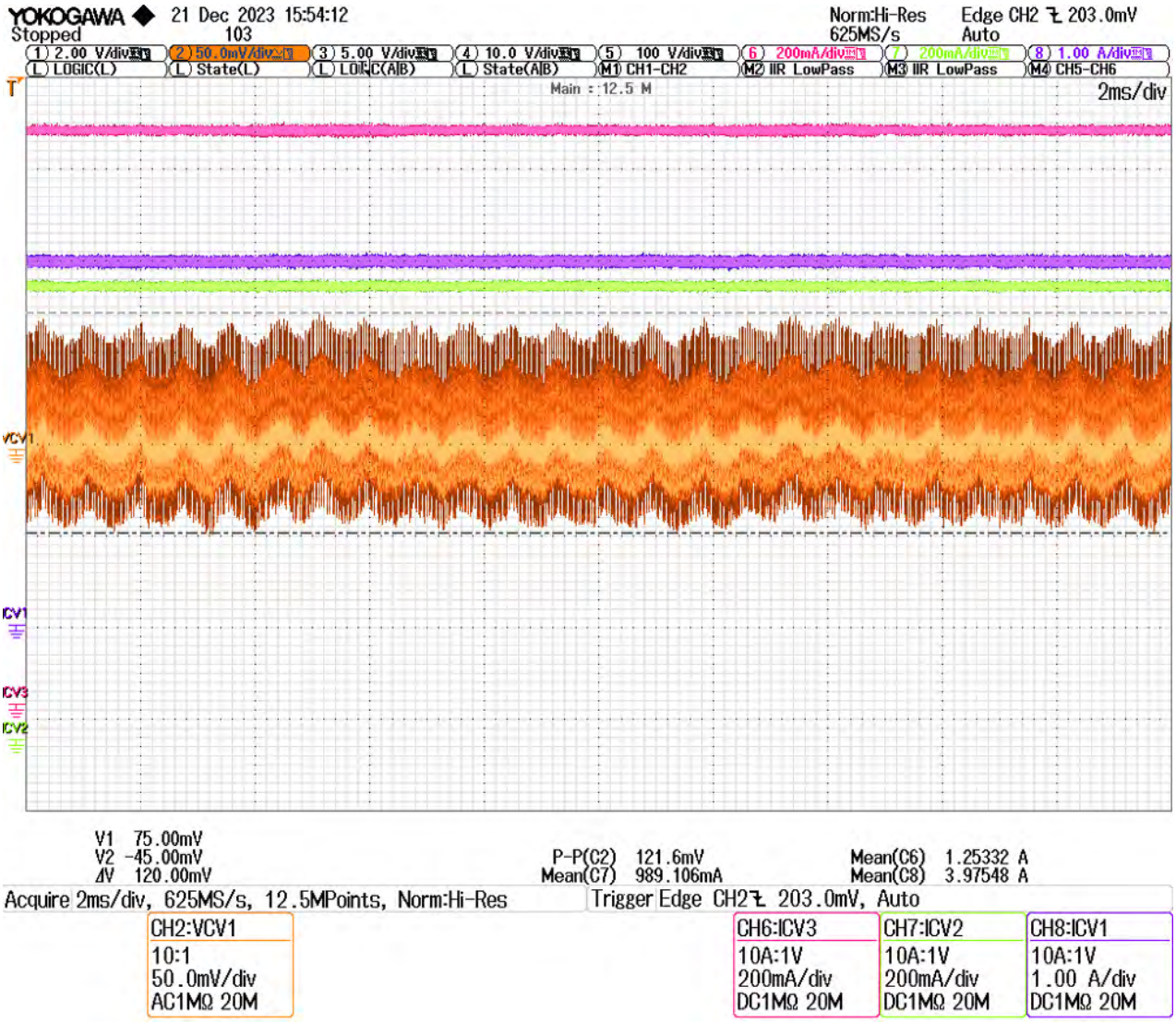



**Figure 102 –** VCV2 Ripple and Noise Under Nominal Load at 90 VAC.

Ch2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

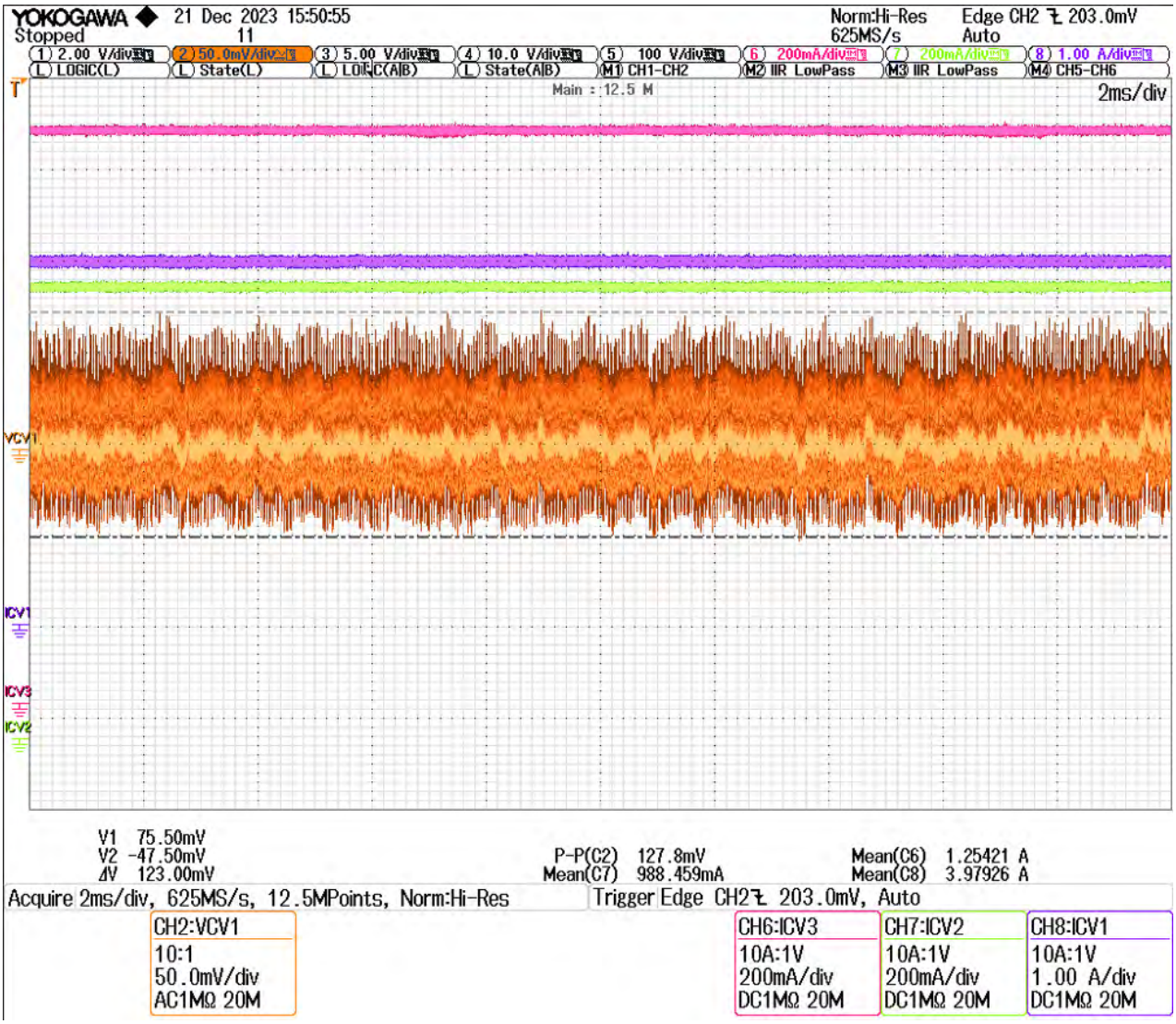



**Figure 103 –** VCV2 Ripple and Noise Under Nominal Load at 265 VAC.

Ch2: $V_{CV2}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

The worst-case ripple and noise at the CV2 output of the converter was measured as 128 $mV_{P-P}$ (<2%) at 20 MHz bandwidth at the connector output.

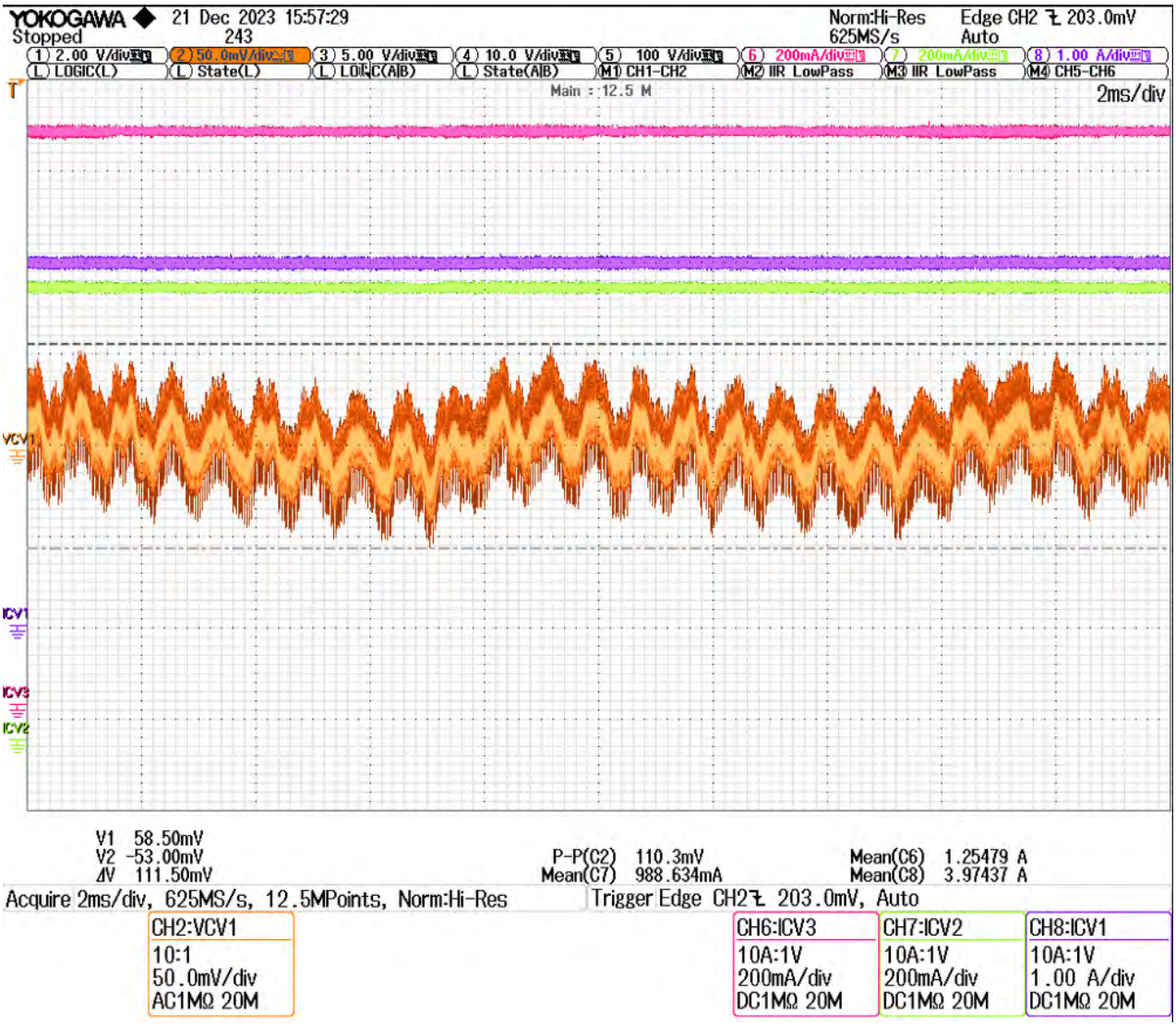



**Figure 104 –** VCV3 Ripple and Noise Under Nominal Load at 90 VAC.

Ch2: $V_{CV3}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

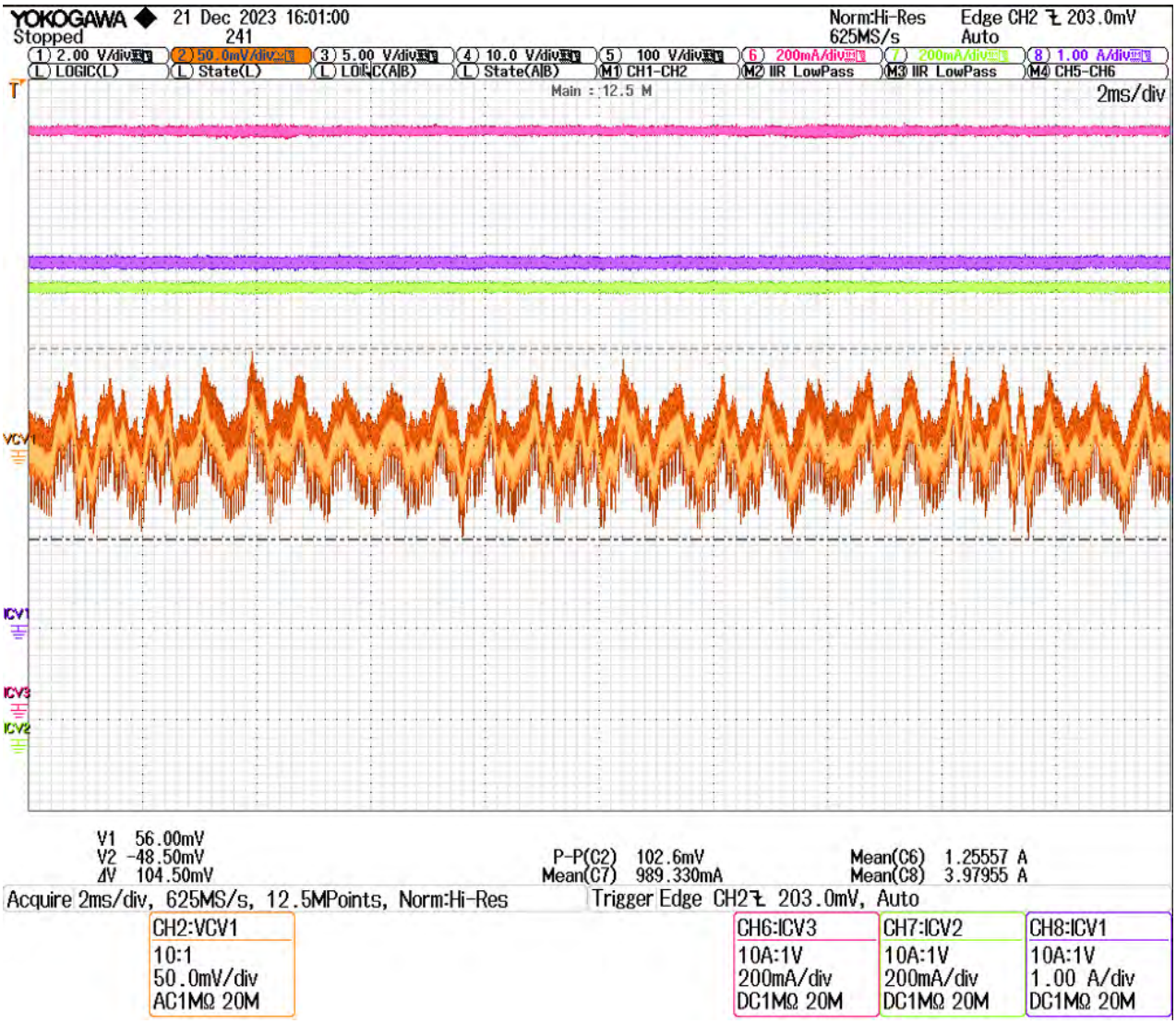



**Figure 105 –** VCV3 Ripple and Noise Under Nominal Load at 265 VAC.

Ch2: $V_{CV3}$, Ch6: $I_{CV3}$, Ch7: $I_{CV2}$, Ch8: $I_{CV1}$

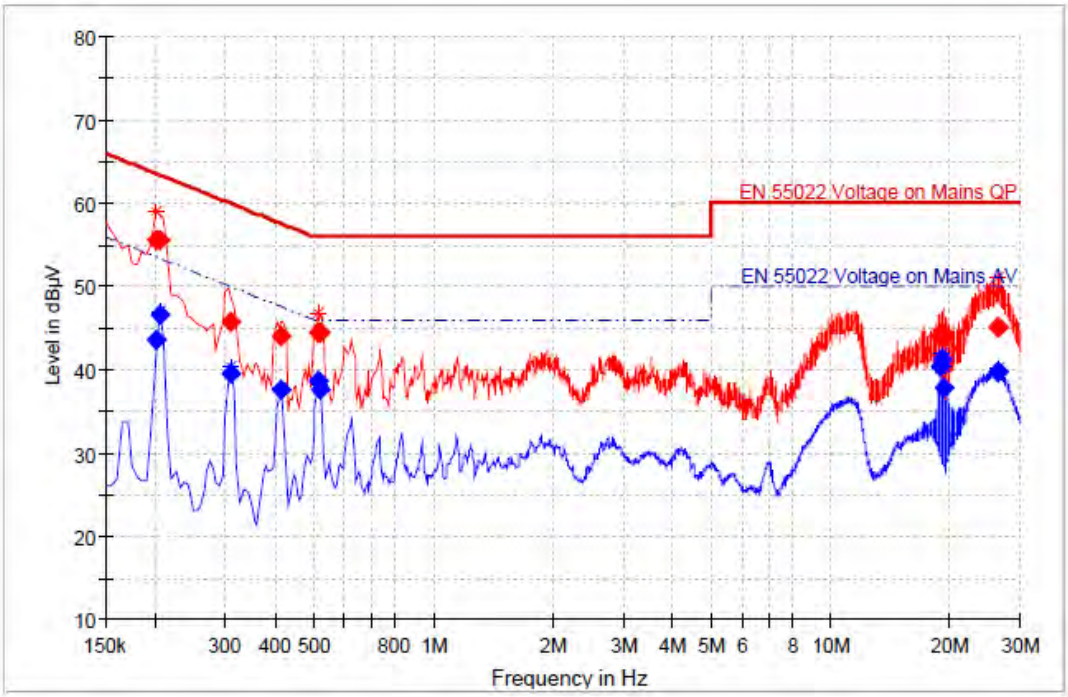
The worst-case ripple and noise at the CV2 output of the converter was measured as 110 $mV_{P-P}$ (<1%) at 20 MHz bandwidth at the connector output.

## *9.12 Conducted EMI*

The EMI scans were carried out at full power without Earth(PE) connection.

The conducted emissions were more than 6 dB below the limits set by CISPR22B / EN55022B.

### 9.12.1 Line Input 115 VAC

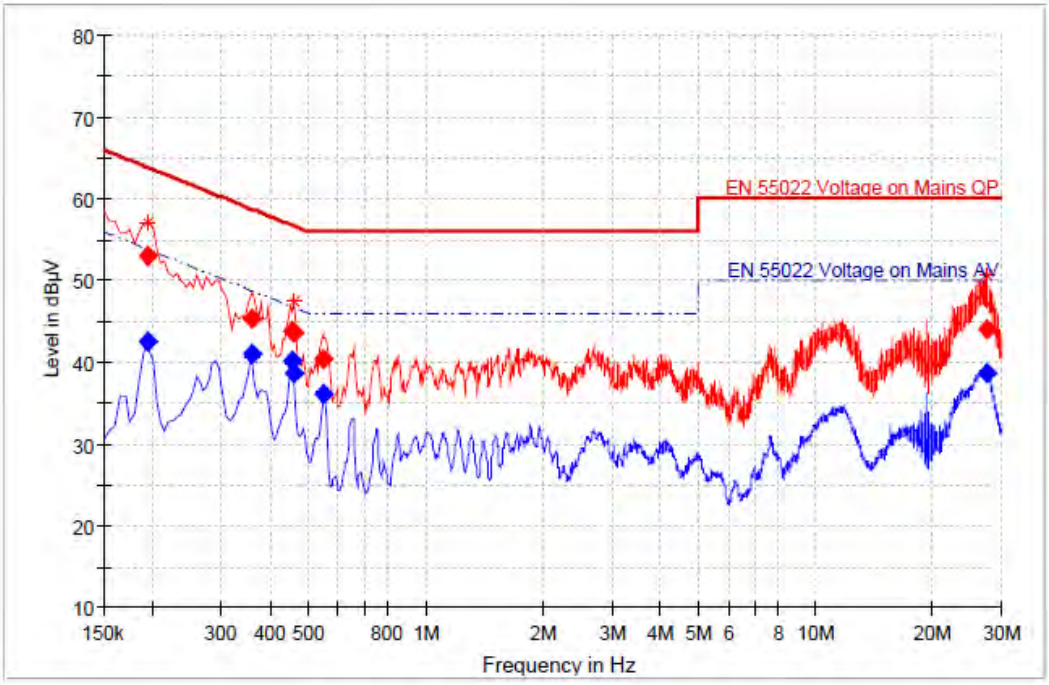



**Final Result**

| Frequency (MHz) | QuasiPeak (dBµV) | Average (dBµV) | Limit (dBµV) | Margin (dB) | Bandwidth (kHz) | Line | Filter | Corr. (dB) |
|---|---|---|---|---|---|---|---|---|
| 0.200000 | 55.56 | --- | 63.61 | 8.05 | 10.000 | N | ON | 20.3 |
| 0.200000 | --- | 43.62 | 53.61 | 9.99 | 10.000 | N | ON | 20.3 |
| 0.205000 | --- | 46.51 | 53.41 | 6.89 | 10.000 | N | ON | 20.3 |
| 0.205000 | 55.64 | --- | 63.41 | 7.76 | 10.000 | N | ON | 20.3 |
| 0.310000 | --- | 39.45 | 49.97 | 10.52 | 10.000 | N | ON | 20.3 |
| 0.310000 | 45.73 | --- | 59.97 | 14.24 | 10.000 | N | ON | 20.3 |
| 0.415000 | 43.93 | --- | 57.55 | 13.62 | 10.000 | N | ON | 20.4 |
| 0.415000 | --- | 37.67 | 47.55 | 9.88 | 10.000 | N | ON | 20.4 |
| 0.515000 | --- | 38.59 | 46.00 | 7.41 | 10.000 | N | ON | 20.4 |
| 0.515000 | 44.39 | --- | 56.00 | 11.61 | 10.000 | N | ON | 20.4 |
| 0.520000 | --- | 37.60 | 46.00 | 8.40 | 10.000 | N | ON | 20.4 |
| 0.520000 | 44.53 | --- | 56.00 | 11.47 | 10.000 | N | ON | 20.4 |
| 18.940000 | --- | 40.31 | 50.00 | 9.69 | 10.000 | L1 | ON | 20.4 |
| 18.940000 | 43.99 | --- | 60.00 | 16.01 | 10.000 | L1 | ON | 20.4 |
| 19.150000 | --- | 41.23 | 50.00 | 8.77 | 10.000 | L1 | ON | 20.4 |
| 19.150000 | 44.46 | --- | 60.00 | 15.54 | 10.000 | L1 | ON | 20.4 |
| 19.355000 | --- | 37.89 | 50.00 | 12.11 | 10.000 | L1 | ON | 20.4 |
| 19.355000 | 43.78 | --- | 60.00 | 16.22 | 10.000 | L1 | ON | 20.4 |
| 26.225000 | --- | 39.73 | 50.00 | 10.27 | 10.000 | L1 | ON | 20.4 |
| 26.225000 | 45.16 | --- | 60.00 | 14.84 | 10.000 | L1 | ON | 20.4 |
| 26.365000 | --- | 39.71 | 50.00 | 10.29 | 10.000 | L1 | ON | 20.4 |
| 26.365000 | 45.18 | --- | 60.00 | 14.82 | 10.000 | L1 | ON | 20.4 |

**Figure 106 –** EMI Test Results at 115 V.

### 9.12.2 Line Input 230 VAC




**Final Result**

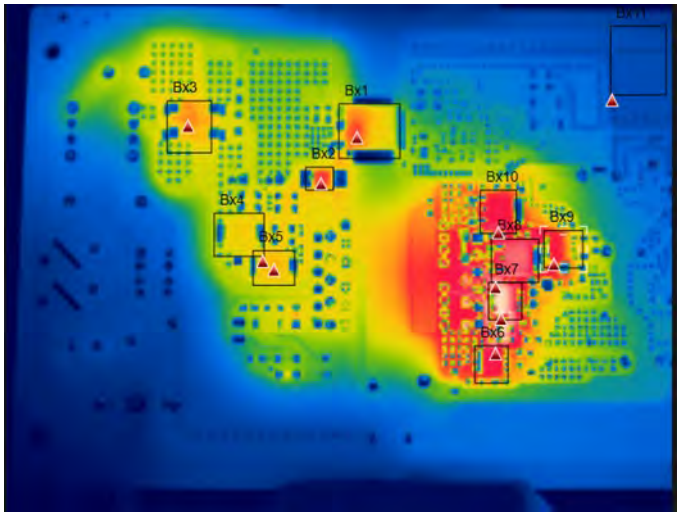
| Frequency (MHz) | QuasiPeak (dBµV) | Average (dBµV) | Limit (dBµV) | Margin (dB) | Bandwidth (kHz) | Line | Filter | Corr. (dB) |
|---|---|---|---|---|---|---|---|---|
| 0.195000 | 52.94 | --- | 63.82 | 10.88 | 10.000 | N | ON | 20.3 |
| 0.195000 | --- | 42.62 | 53.82 | 11.20 | 10.000 | N | ON | 20.3 |
| 0.360000 | --- | 40.94 | 48.73 | 7.79 | 10.000 | N | ON | 20.4 |
| 0.360000 | 45.23 | --- | 58.73 | 13.50 | 10.000 | N | ON | 20.4 |
| 0.455000 | 43.90 | --- | 56.78 | 12.89 | 10.000 | N | ON | 20.4 |
| 0.455000 | --- | 40.26 | 46.78 | 6.53 | 10.000 | N | ON | 20.4 |
| 0.460000 | 43.66 | --- | 56.69 | 13.04 | 10.000 | N | ON | 20.4 |
| 0.460000 | --- | 38.73 | 46.69 | 7.97 | 10.000 | N | ON | 20.4 |
| 0.550000 | 40.49 | --- | 56.00 | 15.51 | 10.000 | N | ON | 20.4 |
| 0.550000 | --- | 36.21 | 46.00 | 9.79 | 10.000 | N | ON | 20.4 |
| 27.405000 | --- | 38.65 | 50.00 | 11.35 | 10.000 | L1 | ON | 20.4 |
| 27.405000 | 44.05 | --- | 60.00 | 15.95 | 10.000 | L1 | ON | 20.4 |

**Figure 107 –** EMI Test Results at 230 V.

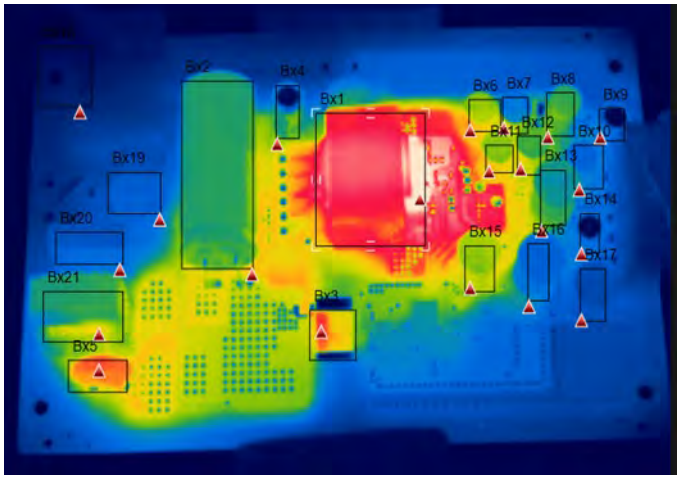
## 9.13 Thermal Performance

There are no heat sinks in cooling arrangements of the assembly. Copper pours are used for the cooling of the control IC. No forced air-cooling was deployed during the test. The temperatures of the hottest components in the assembly are shown in Table.

Ambient temperature is 25 ±2 ºC.

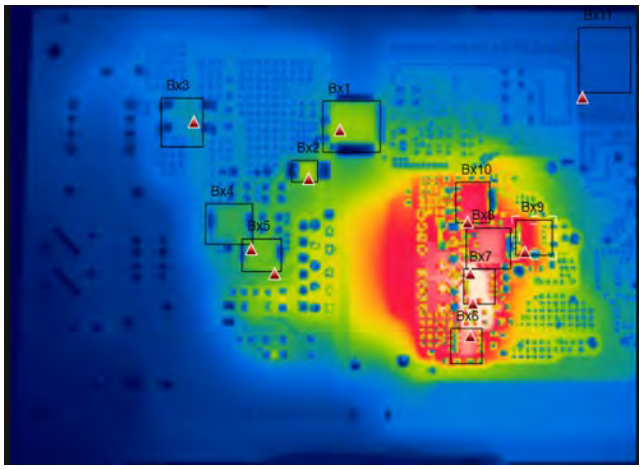



| | | |
|---|---|---|
| U1 InnoMux2-BL IC | BX1 | 82.7 |
| D2 Pri Snubber Diode | BX2 | 83.7 |
| BR1 Bridge Diode | BX3 | 80.2 |
| VR1 Pri Snubber | BX4 | 73.2 |
| VR2 Pri Snubber | BX5 | 74.7 |
| Q2 CV1 Selection Fet | BX6 | 91.2 |
| Q1 SR Fet | BX7 | 100 |
| D5 CV2 Diode | BX8 | 94.8 |
| Q4 CV2 Selection Fet | BX9 | 87.5 |
| D3 CV3 Diode | BX10 | 90.5 |

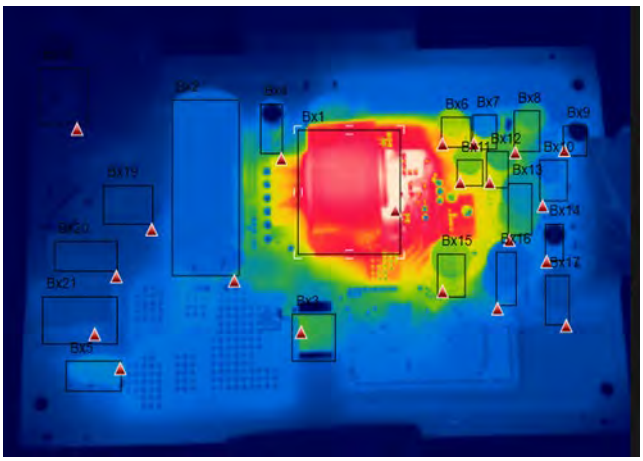



| | | |
|---|---|---|
| T1 Transformer | BX1 | 103.7 |
| C3 Bulk Capacitor | BX2 | 72.7 |
| U1 InnoMux2-BL IC | BX3 | 82.4 |
| C48 Pri Bias Capacitor | BX4 | 61.3 |
| R12 Thermistor | BX5 | 80.9 |
| C10 CV1 Output Capacitor | BX6 | 76.5 |
| C25 CV1 Output Capacitor | BX7 | 67.5 |
| L2 CV1 Output Inductor | BX8 | 61.1 |
| C44 CV1 Output Capacitor | BX9 | 49 |
| C26 CV1 Output Capacitor | BX10 | 54.5 |
| C13 CV2 Output Capacitor | BX11 | 74.7 |
| C35 CV2 Output Capacitor | BX12 | 69 |
| L3 CV2 Output Inductor | BX13 | 60.1 |
| C43 CV2 Output Capacitor | BX14 | 48.3 |
| C14 CV3 Output Capacitor | BX15 | 66.6 |
| L5 CV3 Output Inductor | BX16 | 52.8 |
| C15 CV3 Output Capacitor | BX17 | 42.2 |

**Figure 108 –** Line = 90 V Nominal Power - Thermal Image - Bottom and Top Views.




| | | |
|---|---|---|
| U1 InnoMux2-BL IC | BX1 | 63.1 |
| D2 Pri Snubber Diode | BX2 | 63.4 |
| BR1 Bridge Diode | BX3 | 53.3 |
| VR1 Pri Snubber | BX4 | 59.3 |
| VR2 Pri Snubber | BX5 | 61.3 |
| Q2 CV1 Selection Fet | BX6 | 97.8 |
| Q1 SRFet | BX7 | 107.7 |
| D5 CV2 Diode | BX8 | 100.8 |
| Q4 CV2 Selection Fet | BX9 | 88.2 |
| D3 CV3 Diode | BX10 | 91.4 |




| | | |
|---|---|---|
| T1 Transformer | BX1 | 107.2 |
| C3 Bulk Capacitor | BX2 | 57 |
| U1 InnoMux2-BL IC | BX3 | 61 |
| C48 Pri Bias Capacitor | BX4 | 59.6 |
| R12 Thermistor | BX5 | 54.2 |
| C10 CV1 Output Capacitor | BX6 | 81.8 |
| C25 CV1 Output Capacitor | BX7 | 70.9 |
| L2 CV1 Output Inductor | BX8 | 63.6 |
| C44 CV1 Output Capacitor | BX9 | 50.8 |
| C26 CV1 Output Capacitor | BX10 | 55.7 |
| C13 CV2 Output Capacitor | BX11 | 77 |
| C35 CV2 Output Capacitor | BX12 | 71.1 |
| L3 CV2 Output Inductor | BX13 | 62.3 |
| C43 CV2 Output Capacitor | BX14 | 49.4 |
| C14 CV3 Output Capacitor | BX15 | 67.2 |
| L5 CV3 Output Inductor | BX16 | 53.4 |
| C15 CV3 Output Capacitor | BX17 | 43.2 |

**Figure 109 –** Line = 265 V Nominal Power - Thermal Image - Bottom and Top Views.

### 9.13.1 Audible Noise Performance

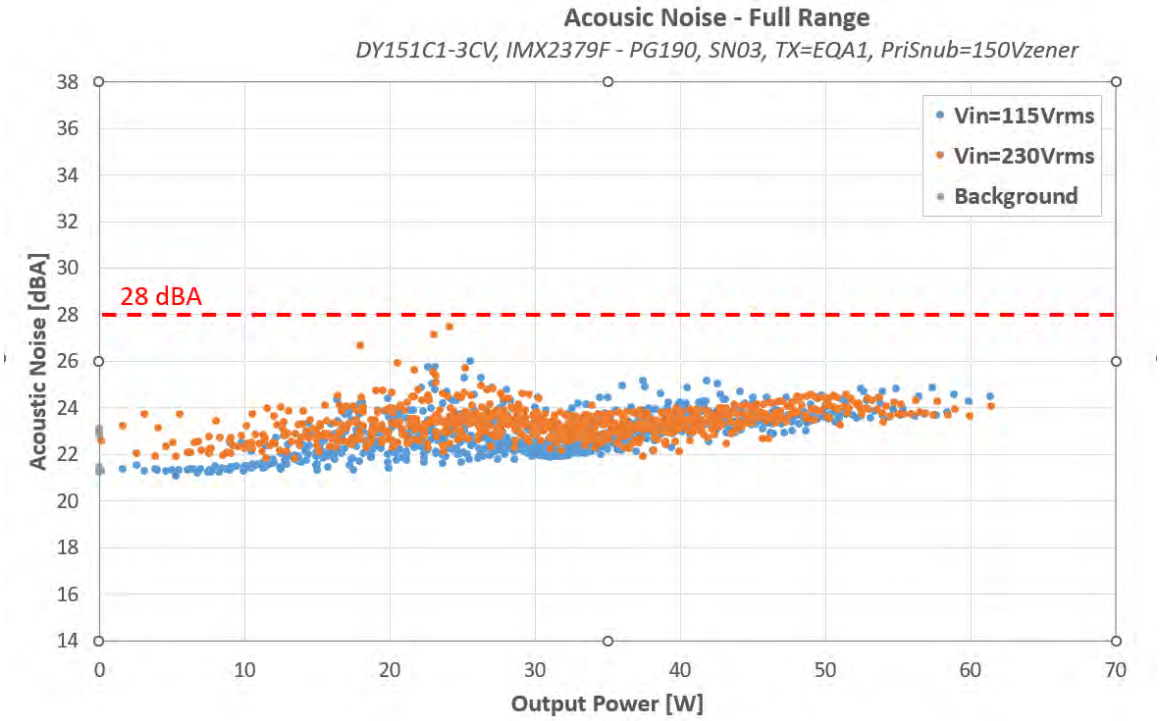



**Figure 110 –** Audible Noise at Normal Operation Mode.

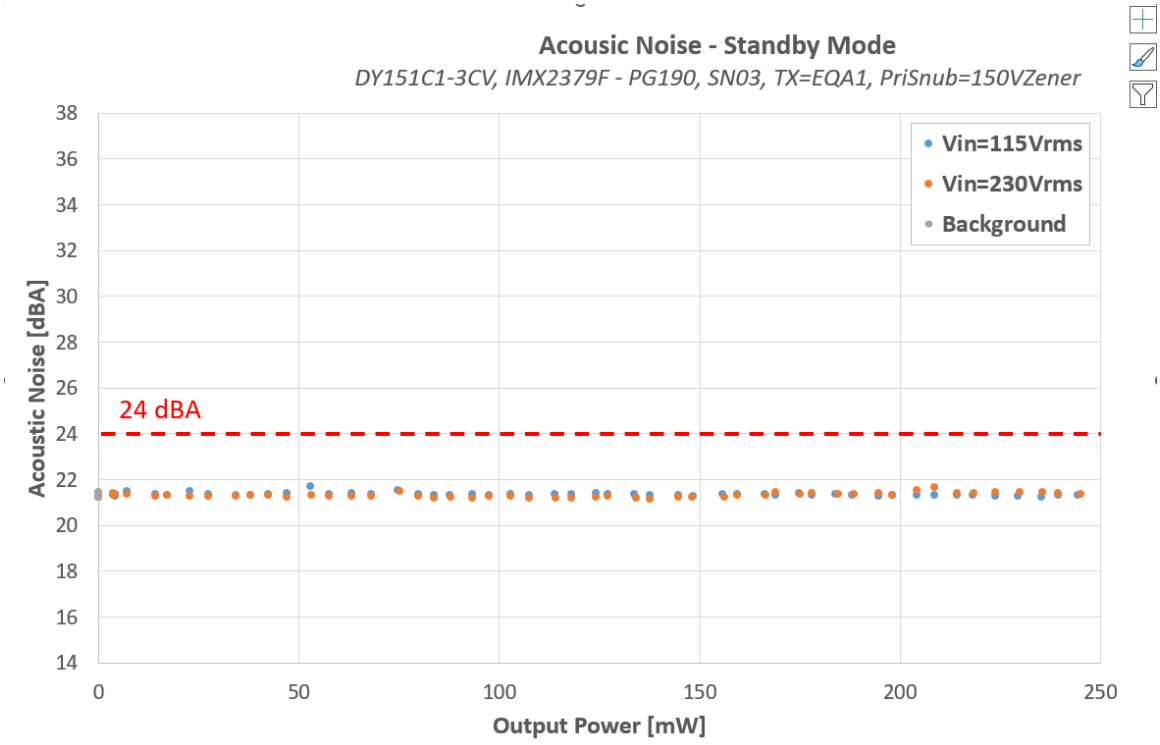



**Figure 111 –** Audible Noise at Standby Mode.

### 9.13.2 Combination Wave Surge Test

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 5 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

### 9.13.3 Differential Mode Surge (L1 to L2), 230 VAC Input

| Surge Level (V) | Injection Location | Injection Phase (°) | Test Result |
|---|---|---|---|
| +1000 | L1 to L2 | 0 | Pass |
| -1000 | L1 to L2 | 0 | Pass |
| +1000 | L1 to L2 | 90 | Pass |
| -1000 | L1 to L2 | 90 | Pass |
| +1000 | L1 to L2 | 180 | Pass |
| -1000 | L1 to L2 | 180 | Pass |
| +1000 | L1 to L2 | 270 | Pass |
| -1000 | L1 to L2 | 270 | Pass |

**Figure 112 –** Differential Mode Surge Test Result.

### 9.13.4 Common Mode Surge (L1 to PE), 230 VAC Input

| Surge level (V) | Injection Location | Injection Phase (°) | Test Result |
|---|---|---|---|
| +2000 | L1 to PE | 0 | Pass |
| -2000 | L1 to PE | 0 | Pass |
| +2000 | L1 to PE | 90 | Pass |
| -2000 | L1 to PE | 90 | Pass |
| +2000 | L1 to PE | 180 | Pass |
| -2000 | L1 to PE | 180 | Pass |
| +2000 | L1 to PE | 270 | Pass |
| -2000 | L1 to PE | 270 | Pass |

**Figure 113 –** Common Mode Surge Test Result – L1 to PE.

*PE is connected to secondary GND to perform common mode test.*

### 9.13.5 Common Mode Surge (L2 to PE), 230 VAC Input

| Surge Level (V) | Injection Location | Injection Phase (°) | Test Result |
|---|---|---|---|
| +2000 | L2 to PE | 0 | Pass |
| -2000 | L2 to PE | 0 | Pass |
| +2000 | L2 to PE | 90 | Pass |
| -2000 | L2 to PE | 90 | Pass |
| +2000 | L2 to PE | 180 | Pass |
| -2000 | L2 to PE | 180 | Pass |
| +2000 | L2 to PE | 270 | Pass |
| -2000 | L2 to PE | 270 | Pass |

**Figure 114 –** Common Mode Surge Test Result – L2 to PE.

*PE is connected to secondary GND to perform common mode test.*

### 9.13.6 Common Mode Surge (L1+L2+PE, 230 VAC Input

| Surge Level (V) | Injection Location | Injection Phase (°) | Test Result |
|---|---|---|---|
| +2000 | L1, L2 and PE | 0 | Pass |
| -2000 | L1, L2 and PE | 0 | Pass |
| +2000 | L1, L2 and PE | 90 | Pass |
| -2000 | L1, L2 and PE | 90 | Pass |
| +2000 | L1, L2 and PE | 180 | Pass |
| -2000 | L1, L2 and PE | 180 | Pass |
| +2000 | L1, L2 and PE | 270 | Pass |
| -2000 | L1, L2 and PE | 270 | Pass |

**Figure 115 –** Common Mode Surge Test Result – L1, L2 and PE

*PE is connected to secondary GND to perform common mode test.*

## 10 Revision History

| Date | Author | Revision | Description & Changes | Reviewed |
|---|---|---|---|---|
| 26-Feb-24 | FT | 1.0 | Draft Release. | Apps |
| | | | | |
| | | | | |
| | | | | |

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5245 Hellyer Avenue
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Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

**CHINA (SHANGHAI)**
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

**CHINA (SHENZHEN)**
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

**GERMANY**
(AC-DC/LED/Motor Control Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

**GERMANY** (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

**INDIA**
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

**ITALY**
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

**JAPAN**
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

**KOREA**
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

**SINGAPORE**
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

**TAIWAN**
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

**UK**
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com