Design Example Report

Title	*1.65 W Non-Isolated Tapped Buck Power Supply Using LinkSwitch™-TN2 LNK3204D*
Specification	85 VAC – 265 VAC Input; 3.3 V / 500 mA Output
Application	Home and Building Automation
Author	Applications Engineering Department
Document Number	DER-574
Date	February 3, 2017
Revision	1.1

Summary and Features

- LinkSwitch-TN2 – high energy efficient off-line switcher IC with integrated system level protection for lowest component count power supply
- 60% efficiency at full load 85 VAC to 265 VAC input
- All the benefits of secondary side control with the simplicity of primary side regulation
  - 5% output voltage regulation over line and load variation
  - Extremely fast transient response independent of load timing
  - Smaller, lower cost output capacitors
  - <10 mW no-load input power

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a single output 3.3 V, 500 mA design utilizing a device from the LinkSwitch-TN2 family of ICs. This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

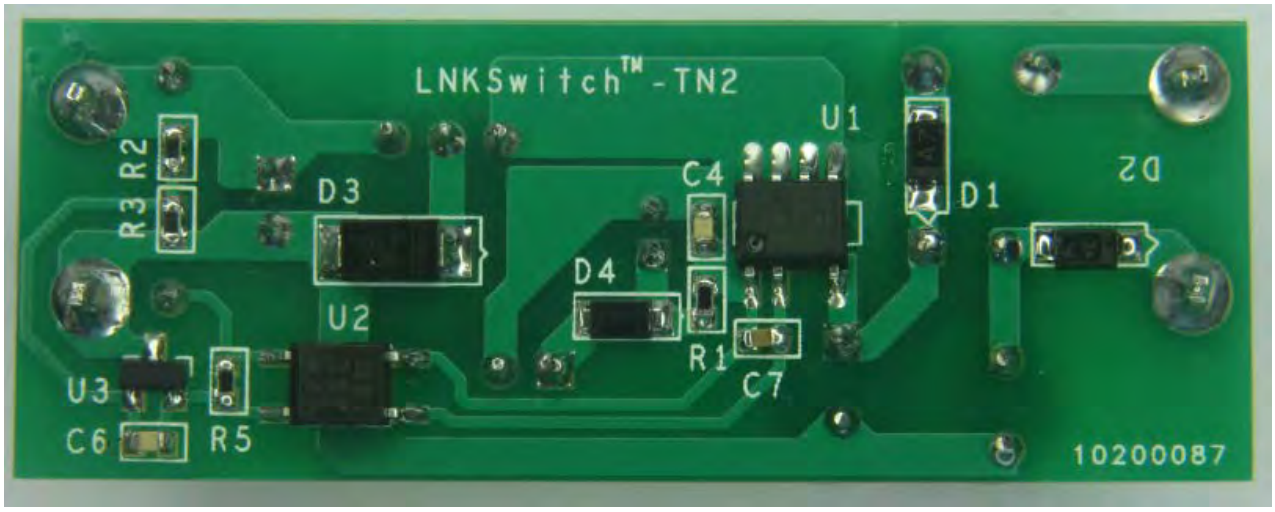

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – No P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				10	mW	100 VAC
Output						
Output Voltage	V_{OUT}	3.135	3.3	3.465	V	±5%
Output Current	I_{OUT}			500	mA	
Output Voltage Ripple	V_{RIPPLE}			100	mV	20 MHz Bandwidth.
Efficiency at 115 VAC / 230 VAC						
Full load	η	60			%	Measured at Output Terminal.
Environmental						
Conducted EMI		CISPR22B / EN55022B Floating or Grounded Load				Resistive Load, 6 dB Margin.
Line Surge						
Differential Mode				1	kV	1.2 μs / 50 μs Surge Mode, 2 Ω.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

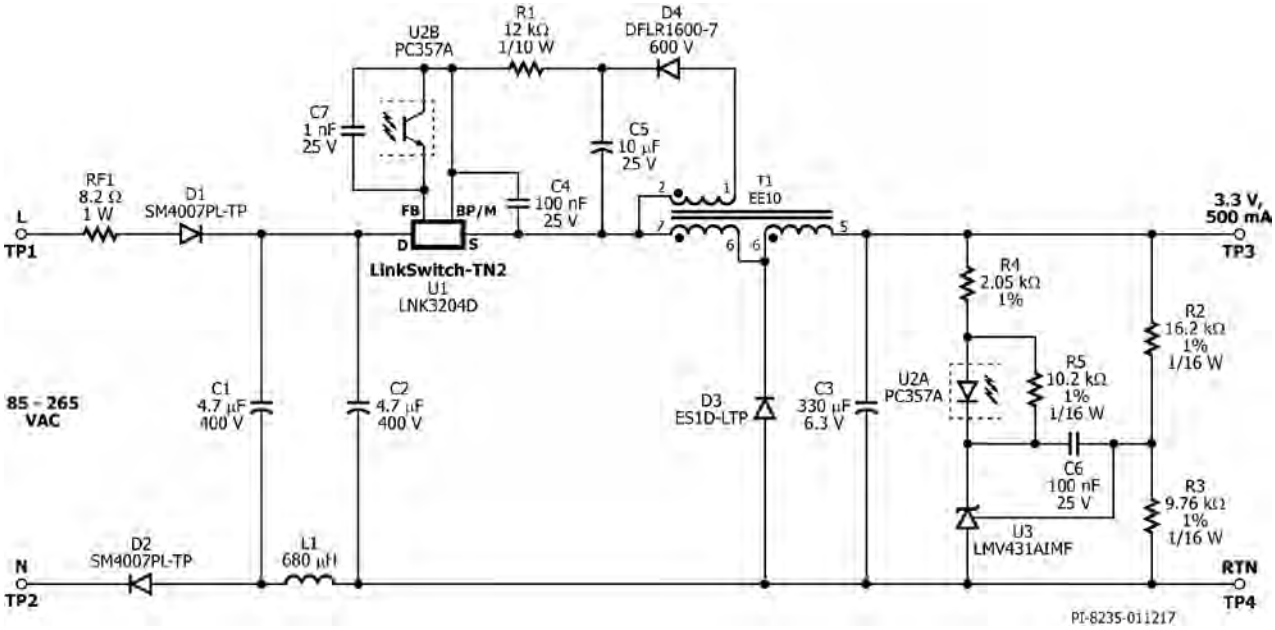

Figure 3 – Schematic.

4 Circuit Description

The LNK3204D IC from the LinkSwitch-TN2 family of devices combines a high-voltage power MOSFET, oscillator, simple On/Off control scheme, a high-voltage switched current source for self-biasing, frequency jittering, cycle-by-cycle current limit, hysteretic thermal shutdown, and output and input overvoltage protection circuitry in a single SO-8 package. The LNK3204D was configured to a 3.3 V with an output current of 500 mA.

4.1 *Input Protection and EMI Filtering*

The fusible resistor RF1 provides fuse safety, inrush current limiting and differential mode noise attenuation. Bridge rectifier D1 and D2 rectifies the AC line voltage and provides an half wave rectified DC across the C1. The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles differential surge withstand as the surge voltage is shared across two diodes. The circuit filter used was a PI filter consisting of C1, L1 and C2, that is capable of low and high frequency rejection.

4.2 *Controller Side*

The circuit topology is a tapped buck with common diode. During switch on-time, current flows through inductor T1 to the load. Energy is stored in the inductor during switch on-time. During off-time the energy stored in the inductor is transferred to the load through flywheel diode D1.

The IC is self-starting, using an internal high-voltage current source to charge the BYPASS (BP) pin capacitor, C4, when AC is first applied. At normal operation the primary side block is powered from the auxiliary output of the circuit, D4 and R1 during switch off-time.

The freewheeling diode, D3, should be an ultra-fast type. Reverse recovery time t_{RR} < 35 ns should be used at a temperature of 70 °C or below. Continuous mode of operation will always occur during start-up thus using slower diodes are not acceptable because it will provide high leading edge current spikes, terminating the operation and preventing the output reaches its regulation.

4.3 *Output Side and Feedback Loop*

The output voltage was 3.3 V and can deliver a maximum power of 1.65 W. For the regulation of the output voltage it utilizes an optocoupler feedback which also eliminates the use of a pre-load resistor. It consists of non safety rated optocoupler, LMV431 shunt regulator and voltage divider. A high capacitance C3 was used to suppress the output ripple to not greater than 100 mV.

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5 PCB Layout

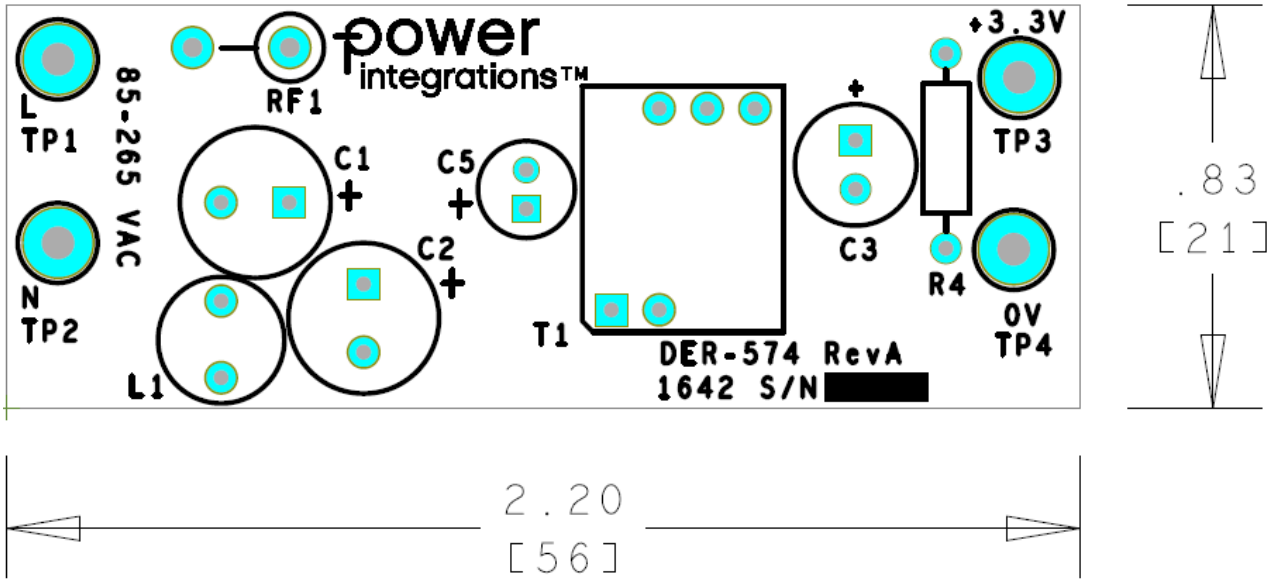

Figure 4 – Printed Circuit Layout, Top.

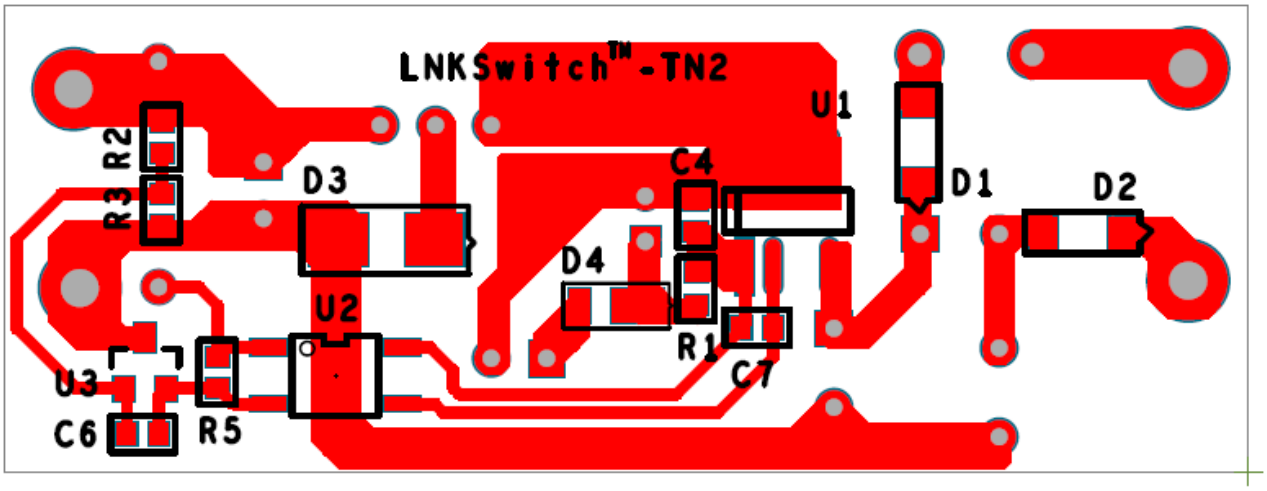

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	4.7 µF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon
2	1	C3	330 µF, 6.3 V, Electrolytic, Low ESR, (6.3 x 11)	6.3 ZLG 330M	Rubycon
3	1	C4	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
4	1	C5	10 µF, 25 V, Electrolytic, Gen. Purpose, (5 x 12)	ECA-1EM100	Panasonic
5	1	C6	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
6	1	C7	1 nF, 25 V, Ceramic, X7R, 0603	GRM188R71E102KA01D	Murata
7	1	D1	1000 V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
8	1	D2	1000 V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
9	1	D3	200 V, 1 A, Super Fast, 35 ns, DO-214AC, SMA	ES1D-LTP	Micro Commercial
10	1	D4	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
11	1	L1	680 µH, 0.21 A, 7 x 10.5 mm	SBC2-681-211	Tokin
12	1	R1	RES, 12 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ123V	Panasonic
13	1	R2	RES, 16.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1622V	Panasonic
14	1	R3	RES, 9.76 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9761V	Panasonic
15	1	R4	RES, 2.05 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-2K05	Yageo
16	1	R5	RES, 10.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1022V	Panasonic
17	1	RF1	RES, 8.2 Ω, 1 W, 5% , Fusible/Flame Proof Wire Wound	FKN1WSJR-52-8R2	Yageo
18	1	T1	Bobbin, EE10, Horizontal, 8 pins	EE10-8P-1S	Kunshan Fengshunhe
19	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
20	2	TP2 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
21	1	TP3	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
22	1	U1	LinkSwitch-TN2, SO-8C	LNK3204D	Power Integrations
23	1	U2	Optoisolator, Transistor Output, 3750 Vrms, 1 Channel, 4-Mini-Flat	PC357N1J000F	Sharp
24	1	U3	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF	National Semi

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7 Transformer Specification

7.1 *Electrical Diagram*

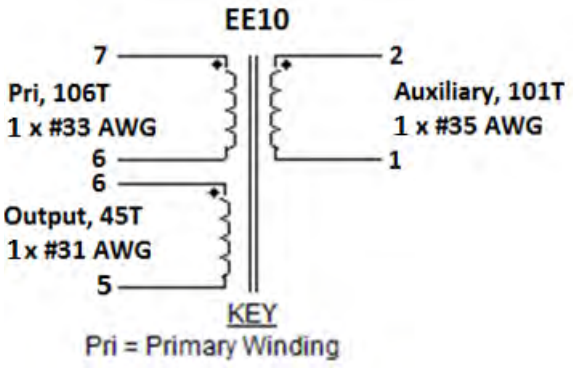

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Main Inductance	Pin 7 and pin 5 together, measured at 100 kHz, 1.0 V_{RMS}.	1294 µH ±5%
Electrical Strength	1 second, 60 Hz, from primary to secondary	n/a

7.3 *Material List*

Item	Description
[1]	Core: EE10.
[2]	Bobbin: EE10-H-8pins.
[3]	Barrier Tape: Polyester film [1 mil (25 µm) base thickness], 7 mm wide.
[4]	Magnet Wire: #35 AWG, Solderable Double Coated.
[5]	Magnet Wire: #31 AWG, Solderable Double Coated.
[6]	Core Tape: Polyester film [1 mil (25 µm) base thickness], 4.5 mm wide.
[7]	Varnish.

7.4 *Transformer Build Diagram*

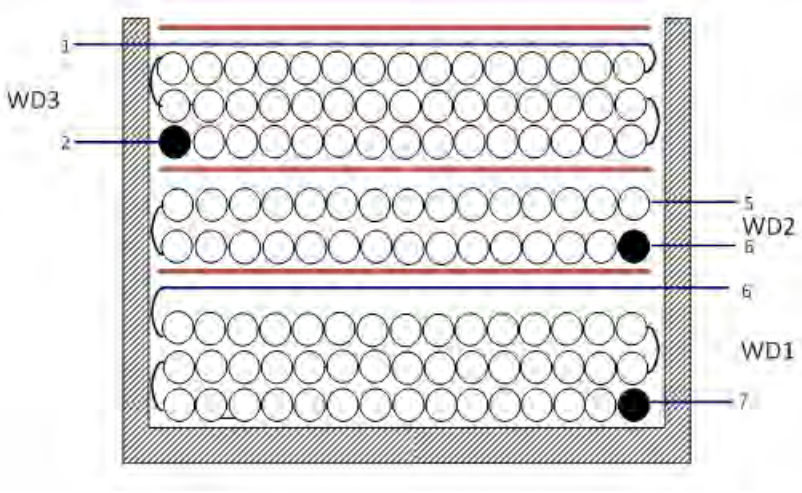

Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1	Starting at pin 7, wind 106 turns of wire (Item [4]) in three layers. Finish at pin 6.
Tape	Use 1 layer of tape (Item [3]) for insulation.
WD2	Starting at pin 6, wind 45 turns of wire (Item [5]) in two layer. Finish at pin 5.
Tape	Use 1 layer of tape (Item [3]) for insulation.
WD3	Starting at pin 2, wind 101 turns of wire (Item [4]) in three layers. Finish at pin 1.
Tape	Use 1 layer of tape (Item [3]) for insulation.
Assembly	Grind core halves for specified primary inductance, insert bobbin, and secure core halves.
Varnish	Dip varnish [8].

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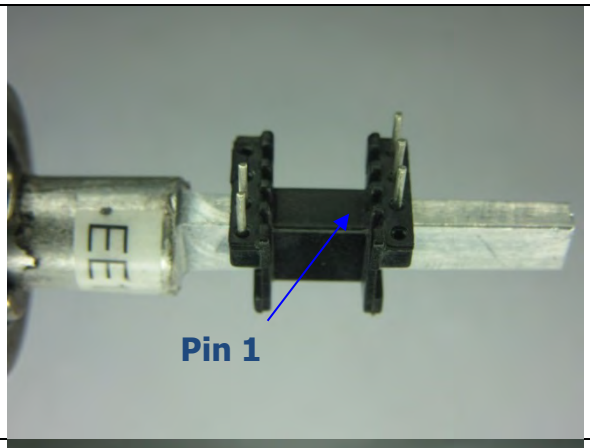
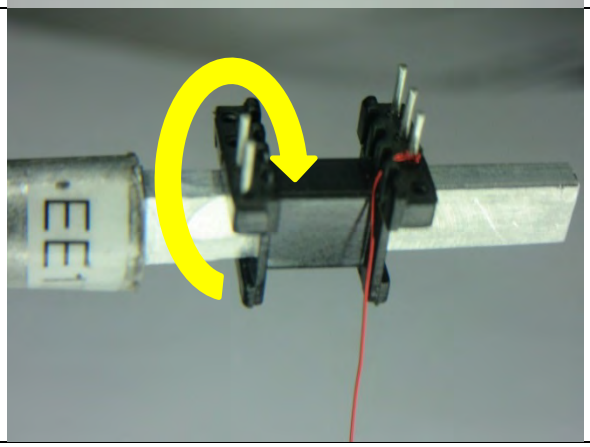
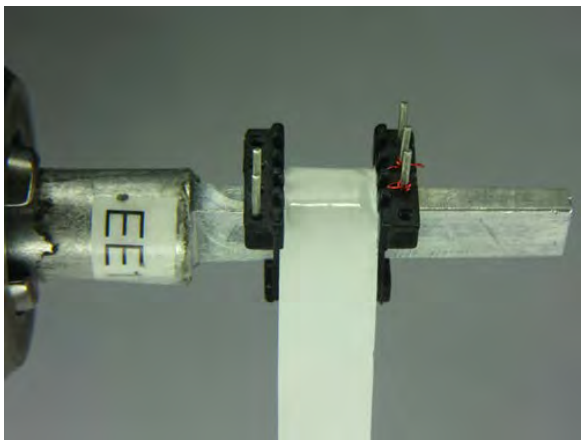
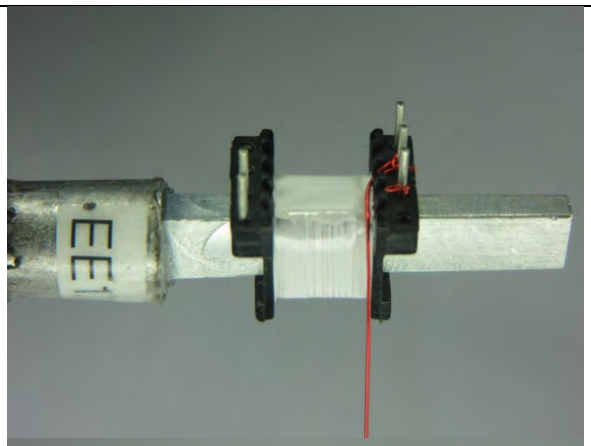
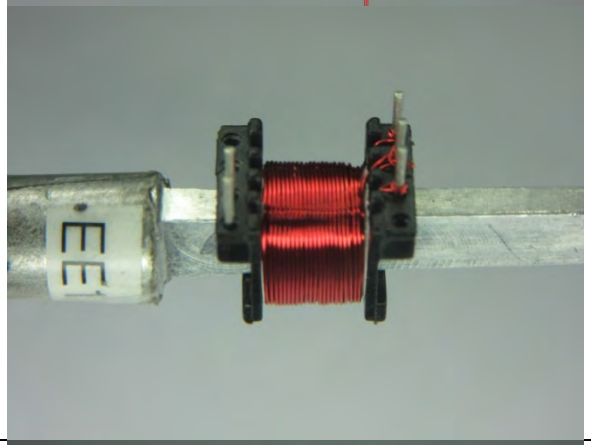
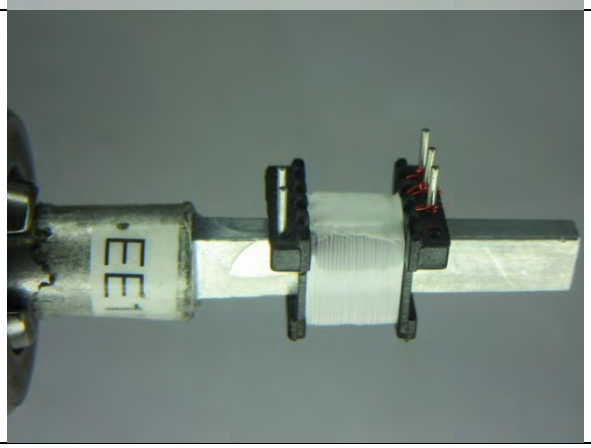
7.6 *Transformer Illustrations*

General Note		For the purpose of these instructions, bobbin is oriented on winder such that pin 1-4 side is on the left side (see illustration). Winding direction as shown is clockwise.
WD 1		Starting at pin 7, wind 106 turns of wire (Item [4]) in three layers.
Tape		Finish at pin 6. Apply one layer of tape (Item [3]) for insulation.

WD 2	 	Starting at pin 6, wind 45 turns of wire (Item [5]) in two layer
Tape		Finish at pin 5. Use 1 layer of tape (Item [3]) for insulation.

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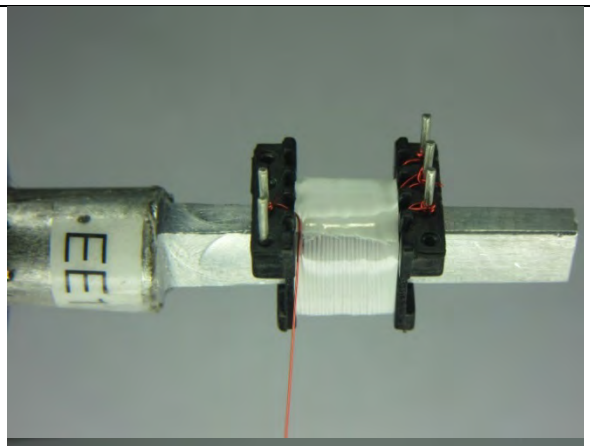
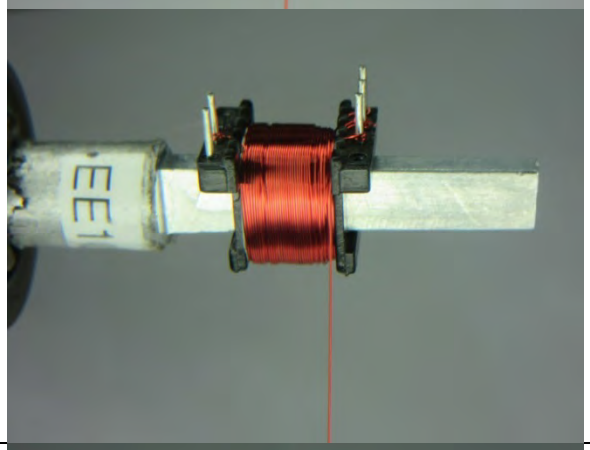
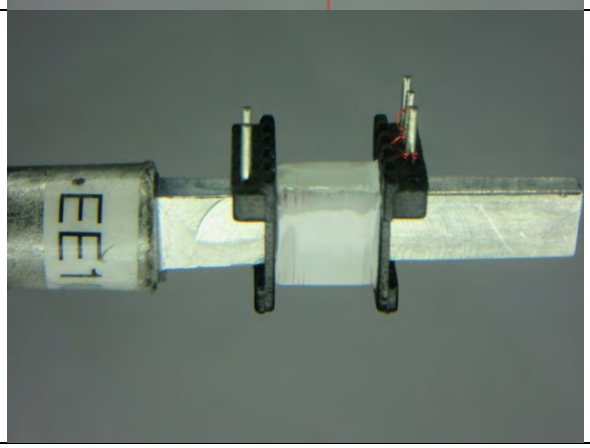
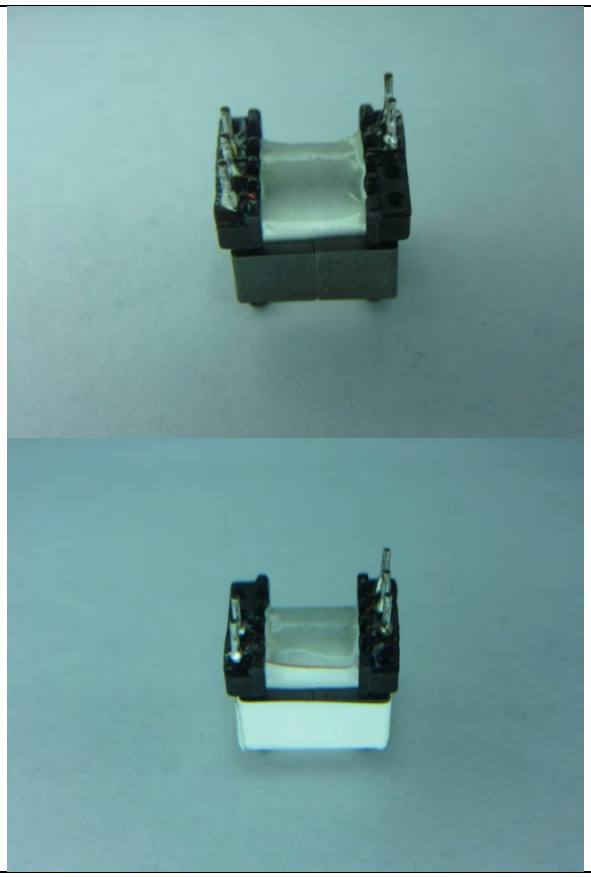
WD3	 	Starting at pin 2, wind 101 turns of wire (Item [4]) in three layers. Finish at pin 1.
Tape		Use 1 layer of tape (Item [3]) for insulation.

Assembly		Grind core halves for specified primary inductance, insert bobbin, and secure core halves. Dip varnish (Item [7]).

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8 Transformer Design Spreadsheet

ACDC_LinkSwitch-TN2_Tapped Inductor Buck_092016; Rev.1.0; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-TN2_Tapped Inductor Buck_092016_Rev1.xls; LinkSwitch-TN2 Tapped-Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	3.30			V	Output Voltage of LED strings
IO	0.50			A	Output Current riving LED strings
Power			1.65	W	Continuous Output Power
n	0.58		0.58		Efficiency Estimate at output terminals. Under 0.7 if no better data available
tC			3.50	ms	Bridge Rectifier Conduction Time Estimate
CIN	9.40			uF	Input Capacitance
DC INPUT VOLTAGE PARAMETERS					
VMIN	72.70		72.70	V	Minimum Input DC bus voltage
VMAX			374.77	V	Maximum Input DC bus voltage
ENTER LinkSwitch-II VARIABLES					
Chosen Device	**LNK3204**		LNK3204		Chosen LinkSwitch-TN2 device
Package	**DG**		DG		Select package (PG, GG or DG)
ILIMITMIN			0.24	A	Minimum Current Limit
ILIMITTYP			0.26	A	Typical Current Limit
ILIMITMAX			0.28	A	Maximum Current Limit
FS			66.00	kHz	Typical Device Switching Frequency at maximum power
VDS			10.00	V	LinkSwitch-TN2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
DESIGN PARAMETERS					
DCON			29.73	us	Output diode conduction time.
TON			4.53	us	LinkSwitch-TN2 On-time (calculated at minimum inductance)
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	**EE10**		EE10		Enter Transformer Core
Bobbin			EE10_BOBBIN		Generic EE10_BOBBIN
AE			12.10	mm^2	Core Effective Cross Sectional Area
LE			26.10	mm^2	Core Effective Path Length
AL			850.00	nH/turn^2	Ungapped Core Effective Inductance
BW			6.60	mm	Bobbin Physical Winding Width
INDUCTOR DESIGN PARAMETERS					
LPMIN			1164.33	uH	Minimum Inductance (Includes inductance of input and output winding)
LPTYP			1293.70	uH	Typical inductance (Includes inductance of input and output winding)
LP_TOLERANCE			10.00	%	Tolerance in inductance
NL_TOTAL			151.00		Total number of turns (Includes input and output winding turns). To adjust Total number of turns change BM_TARGET
ALG			56.17	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	1810.00		1810.00	Gauss	Target Flux Density
BM			1801.53	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 3000 is recommended
BP			2120.47	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3300 is recommended

BAC			900.76	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			145.90		Relative Permeability of Ungapped Core
LG			0.28	mm	Gap Length (LG > 0.1 mm)
INDUCTOR_RATIO	0.30		0.30		Ratio of Output winding turns to Total inductor turns. Adjust ratio to ensure discontinuous operation
Input Section					Section of winding that conducts only during ON time of the LINKSwitch-TN2
NL_INPUT			106.00		Number of turns in Input section.
AWG			38.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
L			2.00		Number of Layers (Input section)
CMA			200.00	Cmils	Primary Winding Current Capacity (200 < CMA < 500)
Output Section					Section of winding that conducts both when the Linkswitch-TN2 is ON and OFF.
NL_OUTPUT			45.00		Number of Turns in Output winding. To adjust number of turns change INDUCTOR_RATIO
AWG_OUTPUT			28.00		Output Winidng Wire Gauge (Rounded to next smaller standard AWG value)
L_OUTPUT			2.49		Number of Layers (Output winding)
CMA_OUTPUT			200.00	Cmils	Output Winding Current Capacity (200 < CMA < 500)
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.30		Maximum duty cycle measured at VMIN
IAVG			0.04	A	Input Average current
IP			0.24	A	Peak primary current
ID_PK			0.92	A	
ISW_RMS			0.08	A	Switch RMS current
ID_RMS			0.70	A	Freewheeling Diode RMS current
IL_RMS			0.08	A	Inductor - Input section RMS current
IL_TAP_RMS			0.70	A	Inductor - Output winding section RMS current
IR			0.24	A	Primary ripple current
FEEDBACK WINDING PARAMETERS					
NFB			101.00		Feedback winding turns (Assume 8.5V FB supply)
VFLY			256.96	V	Voltage across diode at turn off
VFOR			8.53	V	Voltage across Output winidng of inductor when switch is on.
VOLTAGE STRESS PARAMETERS					
VDRAIN			435.84	V	Maximum Drain Voltage Estimate (Assumes 50 V leakage spike)
VOR			11.07	V	Reflected output voltage at turn off (appears in series with LinkSwitch-TN2)
PIVS			111.69	V	Output Rectifier Maximum Peak Inverse Voltage

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9 Performance Data

9.1 *Full Load Efficiency vs. Input Line Voltage*

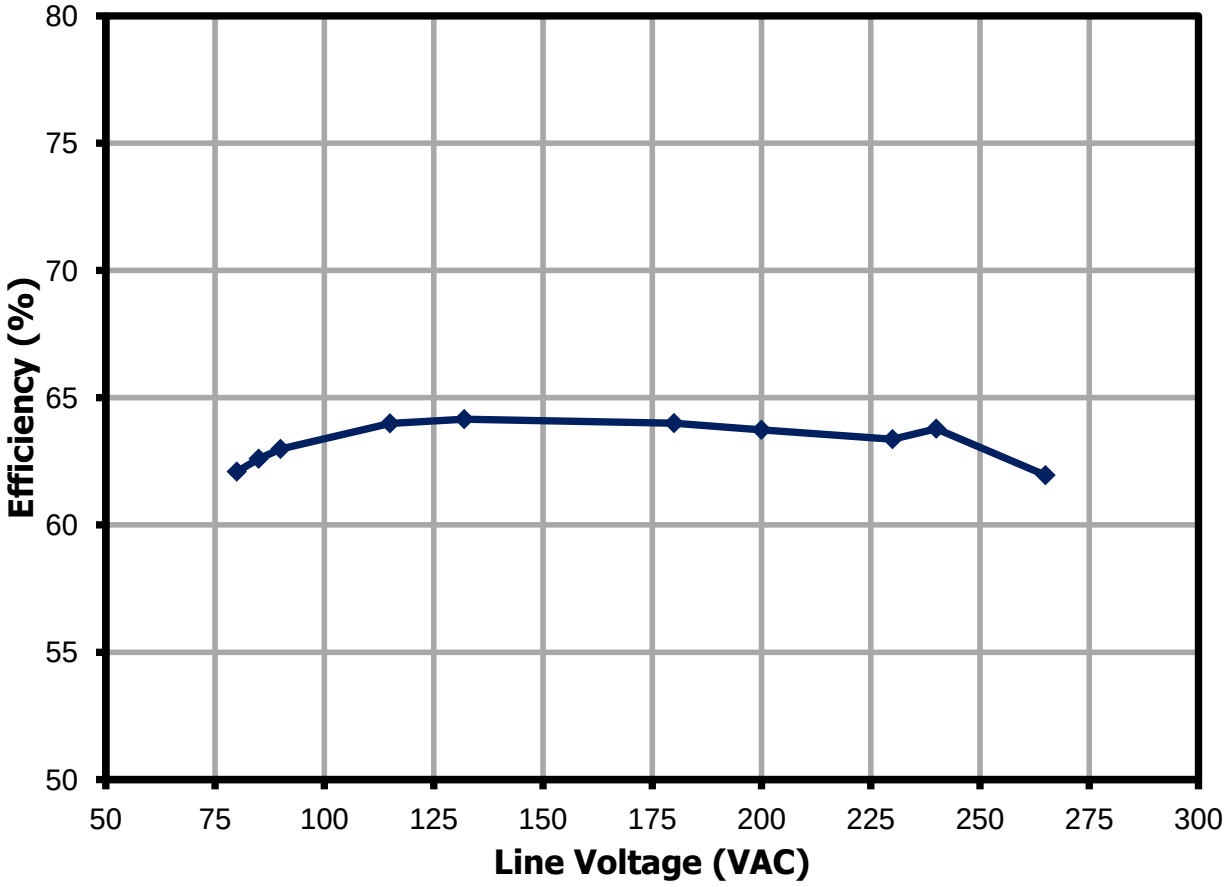

Figure 8 – Efficiency vs. Line Voltage, Room Temperature.

9.2 *Efficiency vs. Load*

Efficiency at 3.3 V Output *(25 mA – 500 mA Load)*

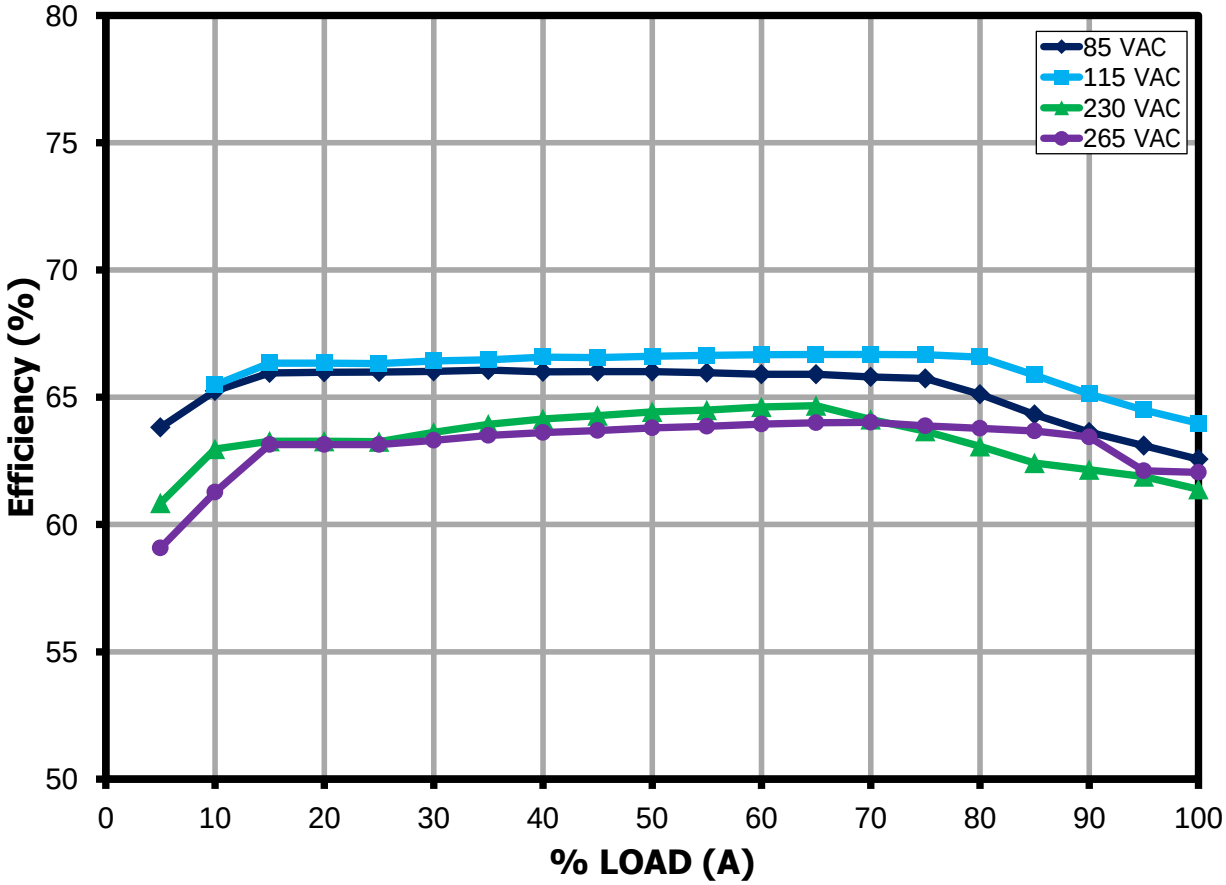

Figure 9 – Efficiency vs. Load, Room Ambient (measured at the Output Terminal).

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9.3 *No-Load Input Power*

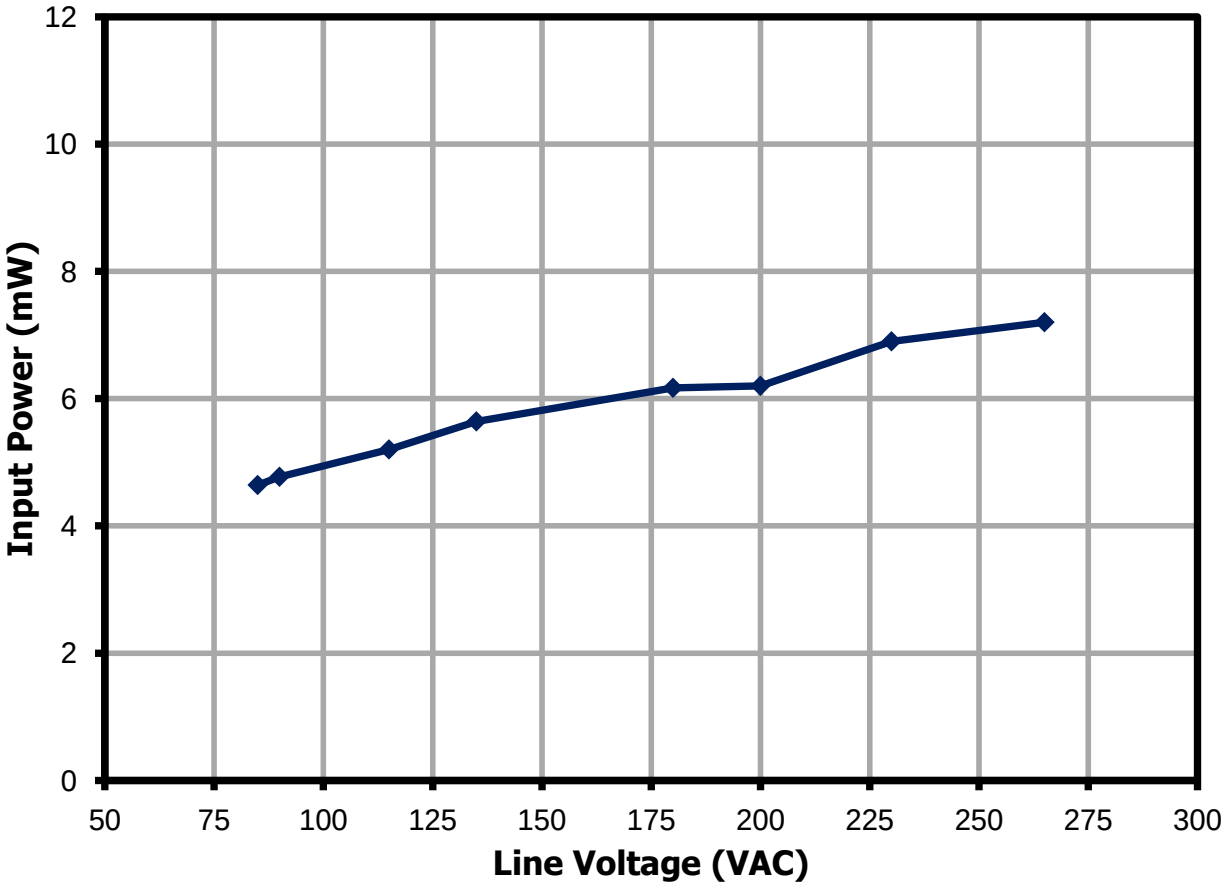

Figure 10 – Input Power vs. Input Line Voltage at No-Load, Room Temperature.

9.4 *Line and Load Regulation*

9.4.1 Line Regulation

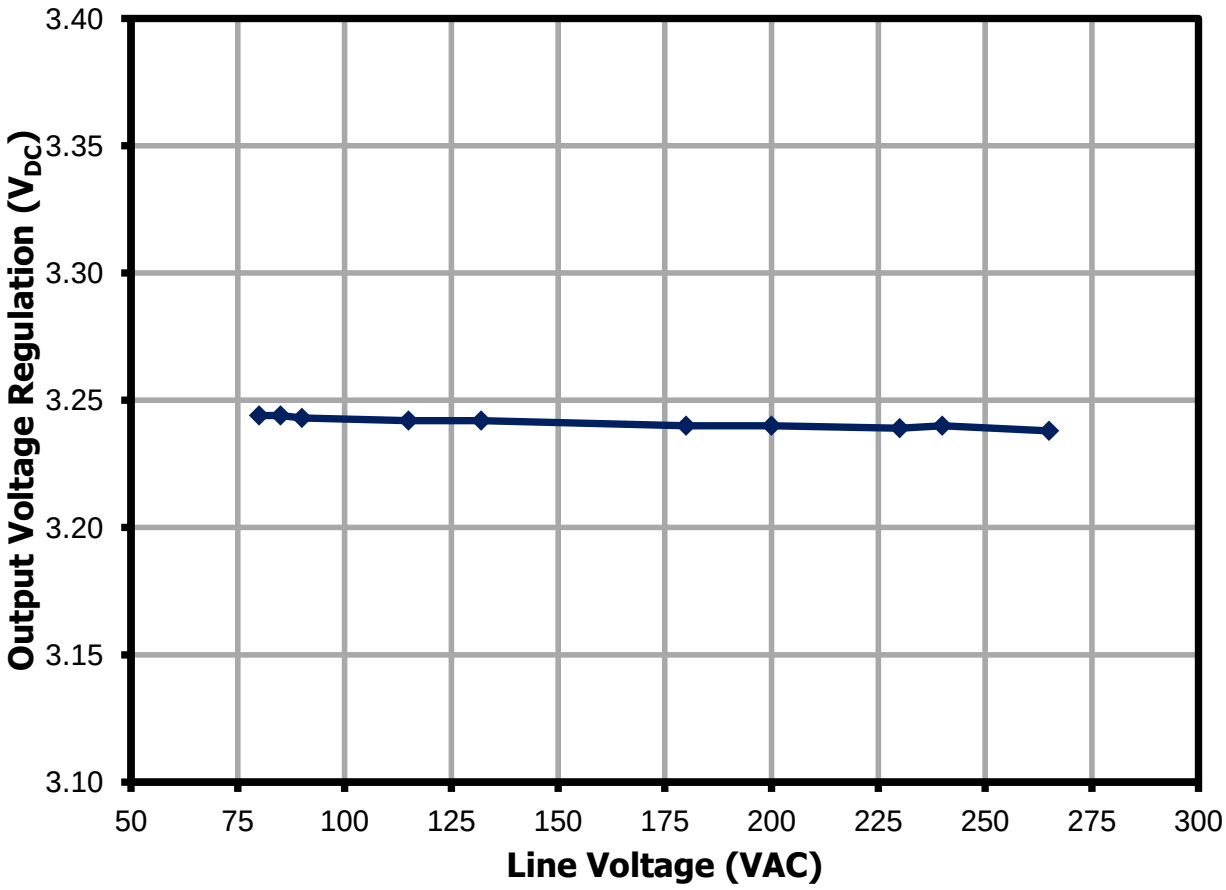

Figure 11 – Output Voltage vs. Input Line Voltage at Full load, Room Temperature.

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9.4.2 Load Regulation

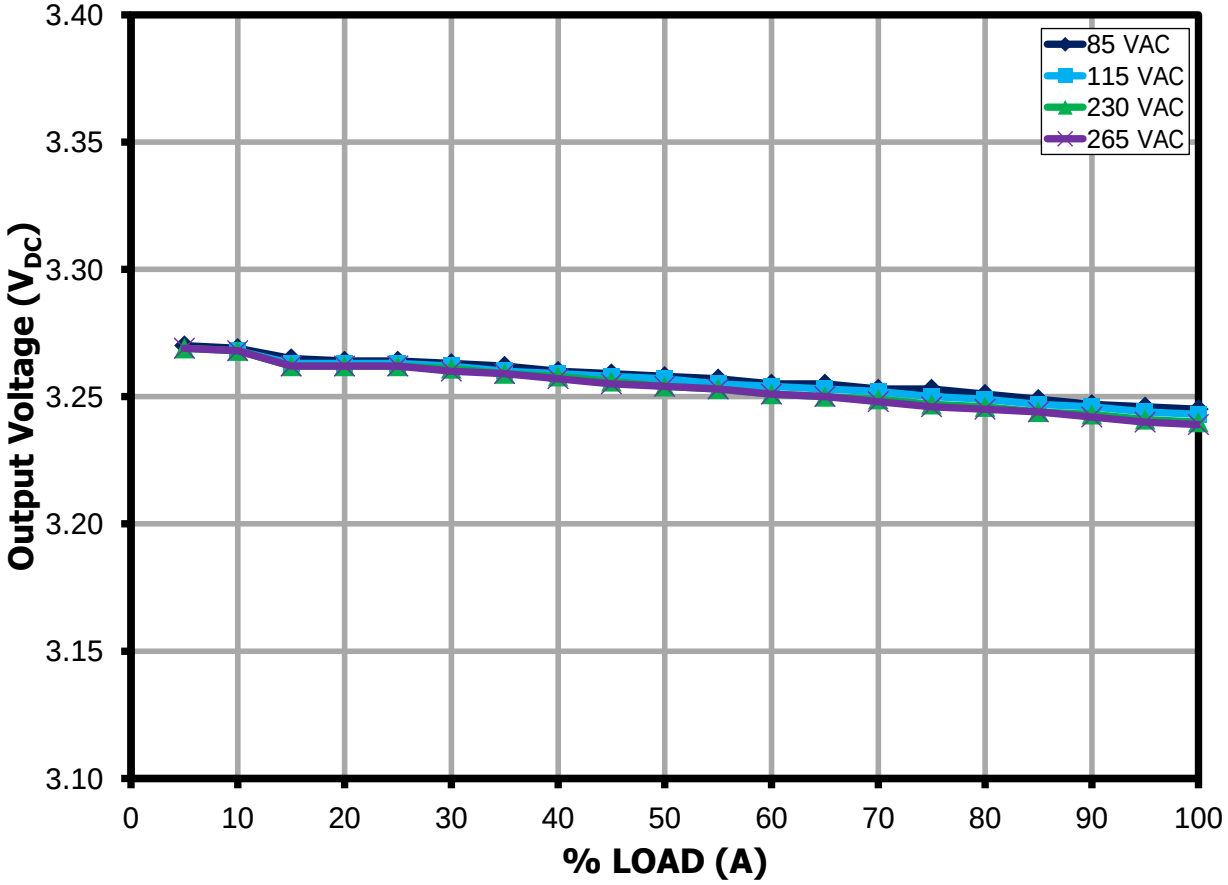


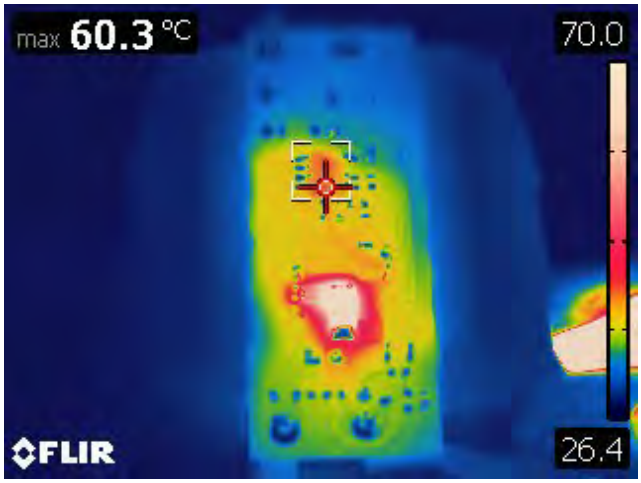
Figure 12 – Output Voltage vs. Varying load, Room Temperature.

10 Thermal Performance

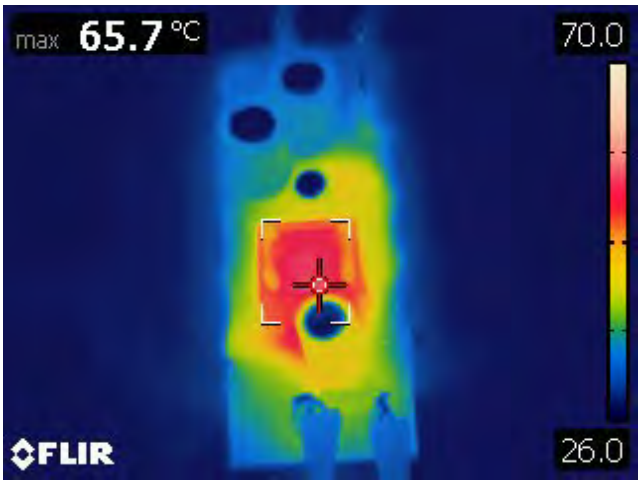
10.1 *Open Case*

For thermal measurement, soak the power supply first for 2 hours. It is recommended that the power supply be placed in an enclosure box to ensure a controlled room temperature environment. Add a thermocouple to monitor ambient temperature.

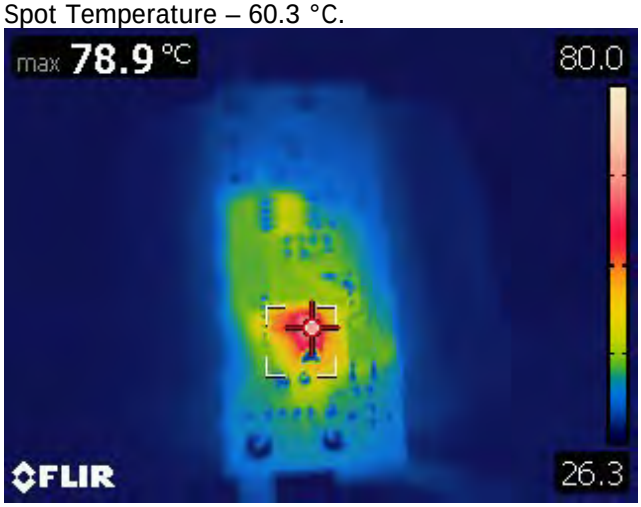
10.1.1 85 VAC at Room Temperature



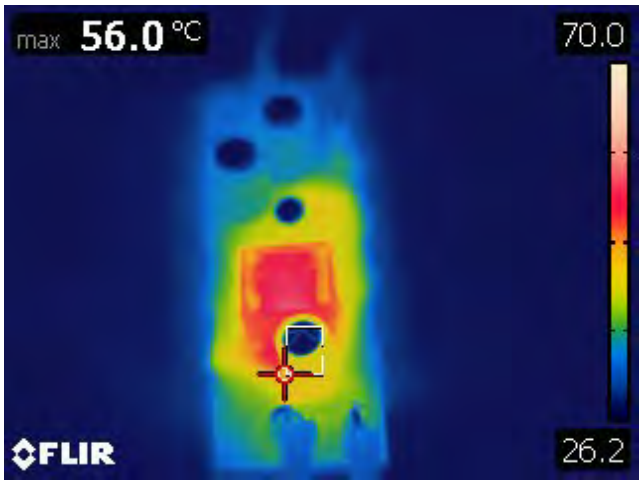
U1 – LinkSwitch-TN2.
Spot Temperature – 60.3 °C.



T1 – Transformer.
Spot Temperature – 65.7 °C.



D3 – Free Wheel Diode.
Spot Temperature – 78.9 °C.



C3 – Output Capacitor.
Spot Temperature – 56.0 °C.

Figure 13 – Measured Temperature at 1.65 W with an Ambient Temperature of 25.0 °C.

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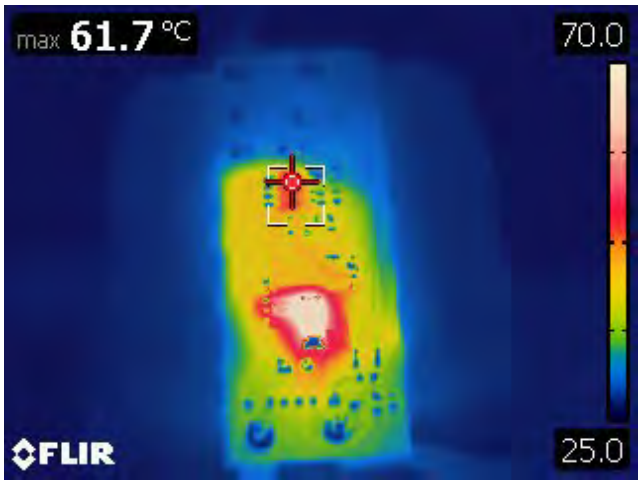
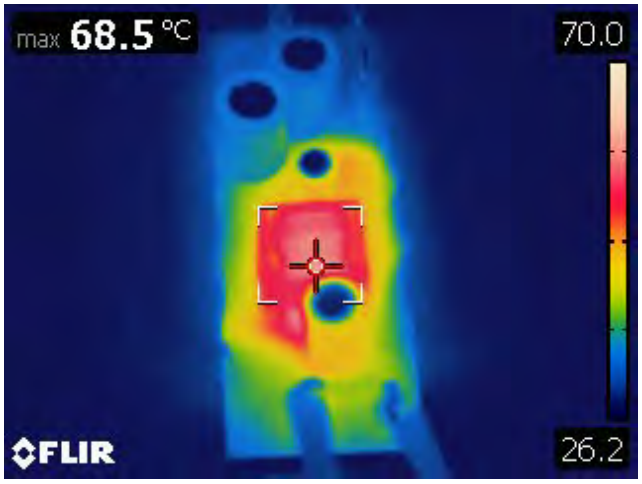
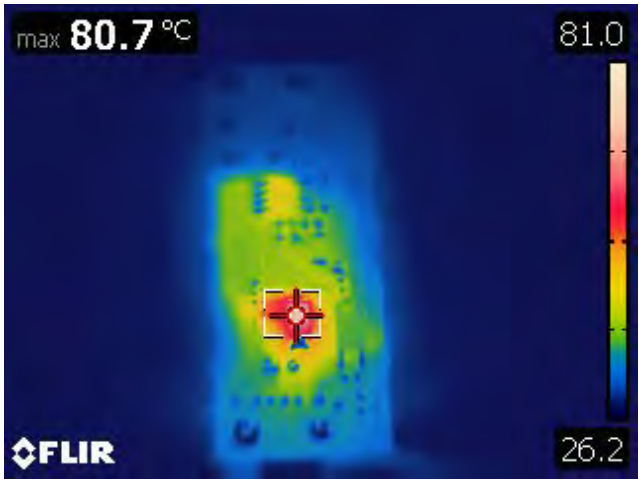
10.1.2 265 VAC at Room Temperature



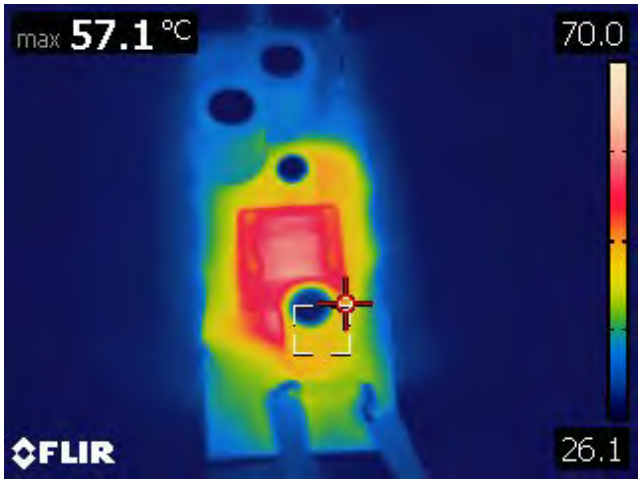
U1 – LinkSwitch-TN2.
Spot Temperature – 61.7 °C.



T1 – Transformer.
Spot Temperature – 68.5 °C.



D3 – Free Wheel Diode.
Spot Temperature – 80.7 °C.



C3 – Output Capacitor.
Spot Temperature – 57.1 °C.

Figure 14 – Measured Temperature at 1.65 W with an Ambient Temperature of 25.0 °C.

11 Waveforms

11.1 *Output Load Transient Response*

Results were taken at the output terminal. The +3.3 V output is step load from 50% to 100% and 0% to 100%

Figure 15 – 85 VAC, 50-100% Load Step.
V_{MAX}: 3.339 V.
V_{MIN}: 3.1494 V.
Upper: V_{OUT}, 400m V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

Figure 16 – 265 VAC, 50-100% Load Step.
V_{MAX}: 3.323 V.
V_{MIN}: 3.117 V.
Upper: V_{OUT}, 400m V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

Figure 17 – 85 VAC, 0-100% Load Step.
V_{MAX}: 3.354 V.
V_{MIN}: 3.070 V.
Upper: V_{OUT}, 400m V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

Figure 18 – 265 VAC, 0-100% Load Step.
V_{MAX}: 3.339 V.
V_{MIN}: 3.0545 V.
Upper: V_{OUT}, 400m V / div.
Lower: I_{LOAD}, 100 mA / div., 10 ms / div.

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11.2 *Switching Waveforms*

11.2.1 Drain to Source Voltage, Current and Freewheel During Normal Operation.

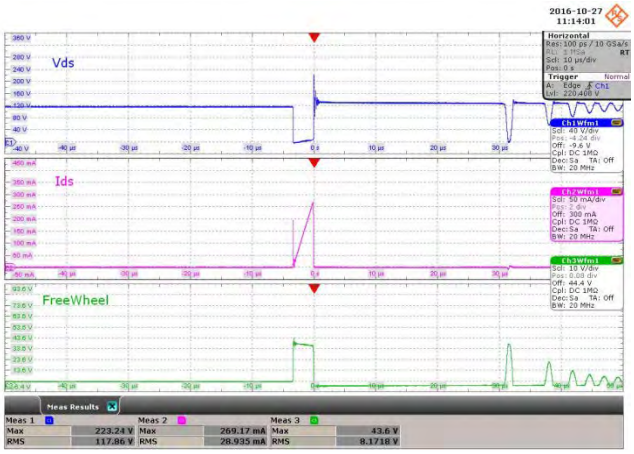

Figure 19 – 85 VAC Input.
Condition: 3.3 V – 0 mA.
Upper: V_{DS}, 40 V / div.
Middle: I_{DS}, 50 mA / div.
Lower: V_{FWL}, 10 V / div. 10 μs / div.

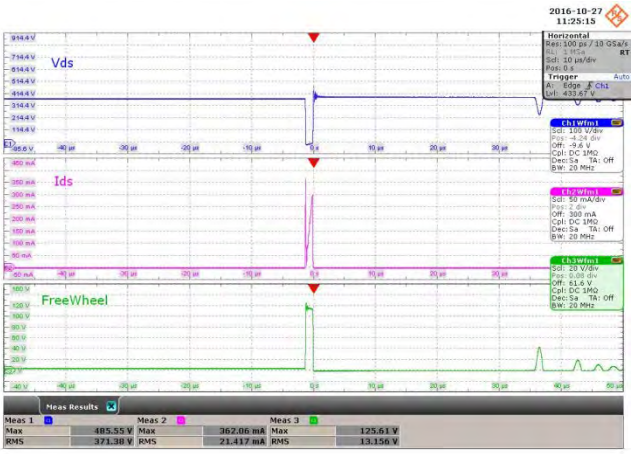

Figure 20 – 265 VAC Input.
Condition: 3.3 V – 0 mA.
Upper: V_{DS}, 100 V / div.
Middle: I_{DS}, 50 mA / div.
Lower: V_{FWL}, 20 V / div. 10 μs / div.

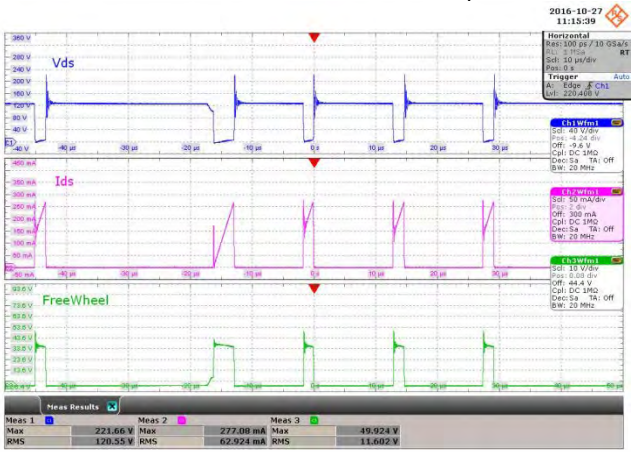

Figure 21 – 85 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{DS}, 40 V / div.
Middle: I_{DS}, 50 mA / div.
Lower: V_{FWL}, 10 V / div. 10 μs / div.

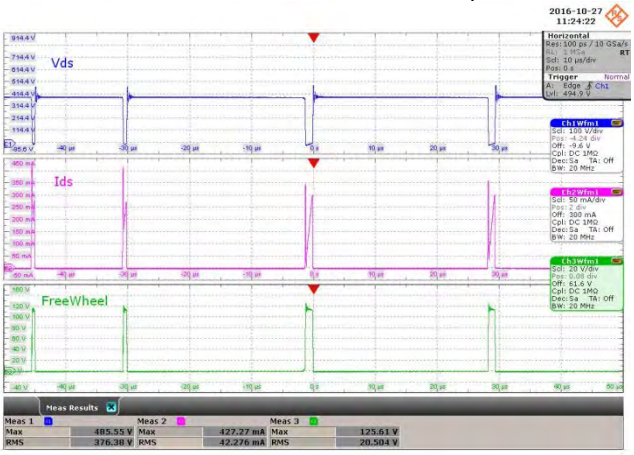

Figure 22 – 265 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{DS}, 100 V / div.
Middle: I_{DS}, 50 mA / div.
Lower: V_{FWL}, 20 V / div. 10 μs / div.

11.2.2 Drain to Source Voltage and Current Waveforms During Turn-On

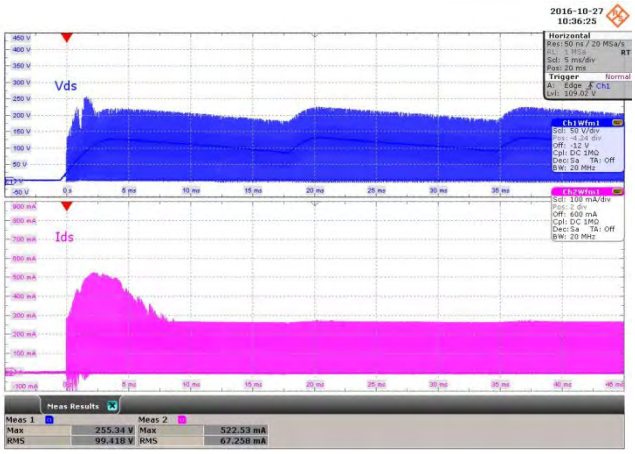

Figure 23 – 85 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{DS}, 50 V, 5 ms / div.
Lower: I_{DS}, 100 mA / div.

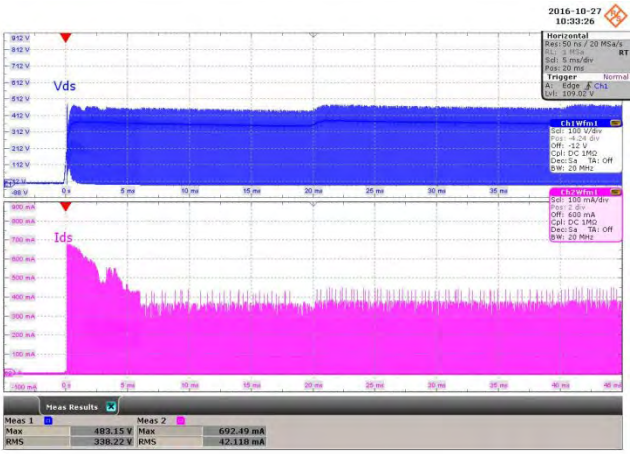

Figure 24 – 265 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{DS}, 100 V, 5 ms / div.
Lower: I_{DS}, 100 mA / div.

11.2.3 Input and Output Voltages Waveforms during Turn-On

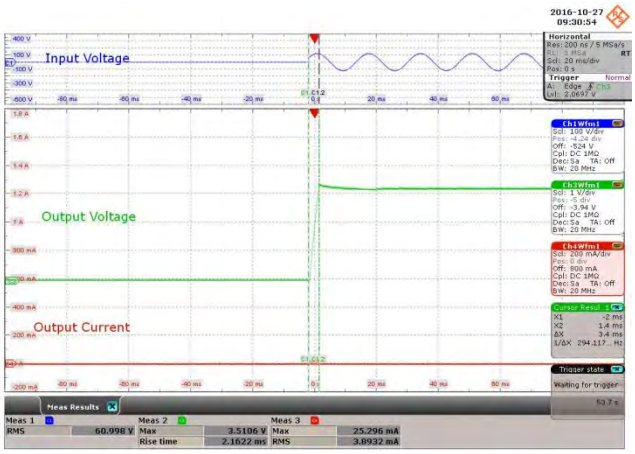

Figure 25 – 85 VAC Input.
Condition: 3.3 V – 0 mA.
Upper: V_{IN}, 100 V, 20 ms / div.
Middle:V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div.

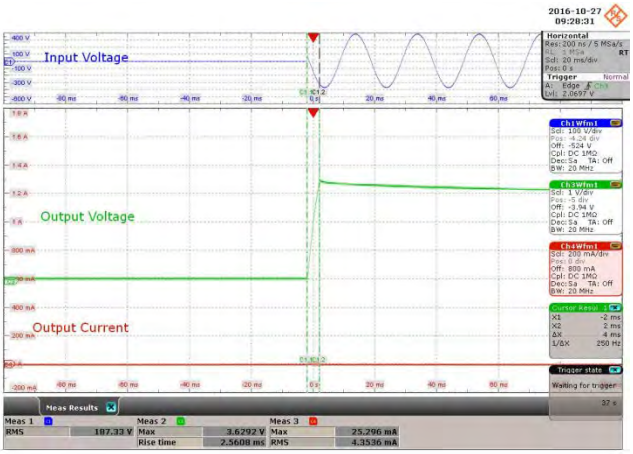

Figure 26 – 265 VAC Input.
Condition: 3.3V – 0 mA.
Upper: V_{IN}, 100 V, 20 ms / div.
Middle:V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div.

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Figure 27 – 85 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{IN}, 100 V, 20 ms / div.
Middle:V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div.

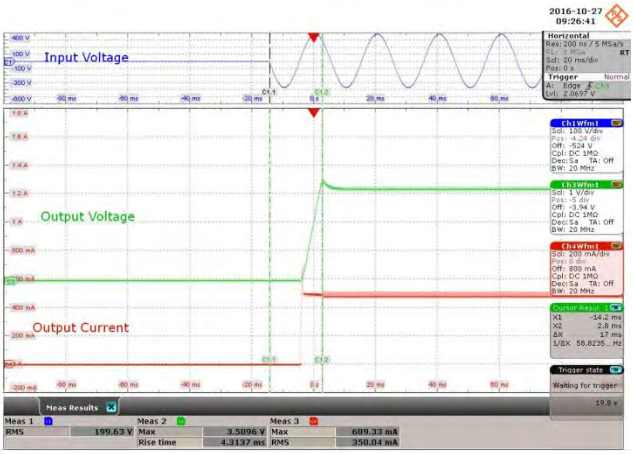

Figure 28 – 265 VAC Input.
Condition: 3.3 V – 500 mA.
Upper: V_{IN}, 100 V, 20 ms / div.
Middle:V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div.

11.2.4 Output Short Auto-Restart

Short the main output (3.3 V) and monitor V_{DS}, I_{DS}, output voltage and output current. Auto-restart is typical = 1.5 s.

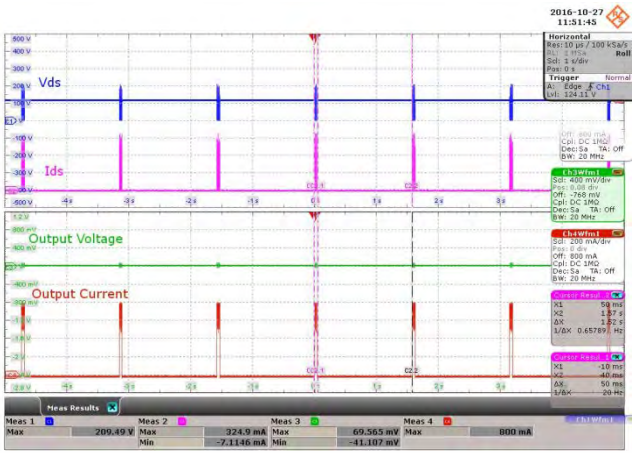

Figure 29 – 85 VAC Input.
Condition: 3.3 V – Shorted.
Auto-Restart: 1.52 s.
Upper: V_{DS}, 100 V / div, 1.0 s / div.
Upper Middle: I_{DS}, 200 mA / div.
Lower Middle: V_{OUT}, 400 mV / div.
Lower: I_{OUT}, 400 mA / div.

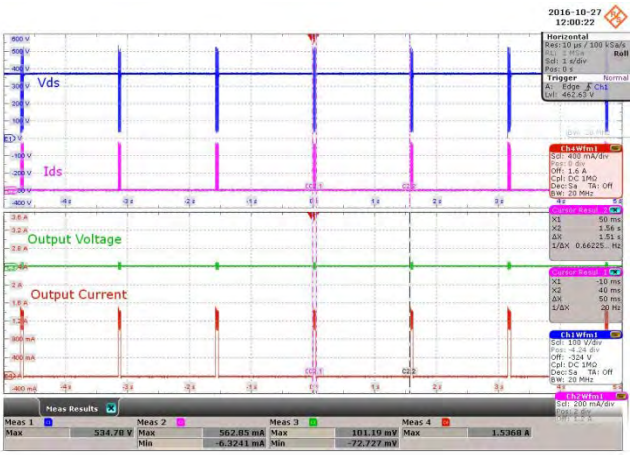

Figure 30 – 265 VAC Input.
Condition: 3.3 V – Shorted.
Auto-Restart: 1.51 s.
Upper: V_{DS}, 100 V / div, 1.0 s / div.
Upper Middle: I_{DS}, 200 mA / div.
Lower Middle: V_{OUT}, 400 mV / div.
Lower: I_{OUT}, 400 mA / div.

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11.3 *Output Ripple Measurements*

11.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1 uF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

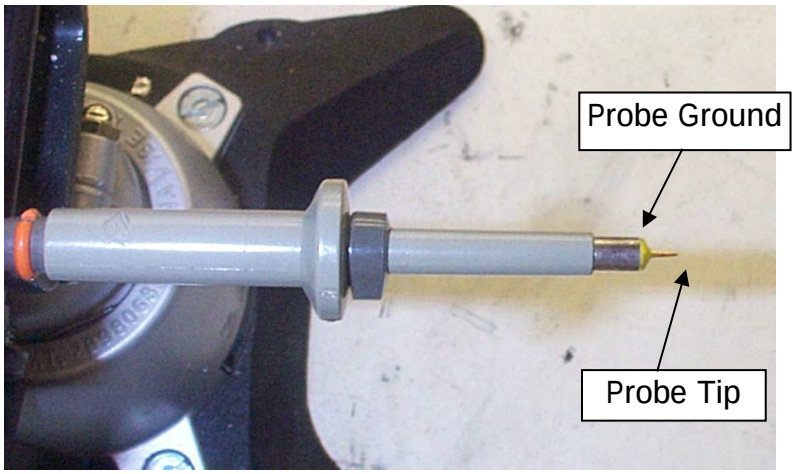

Figure 31 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

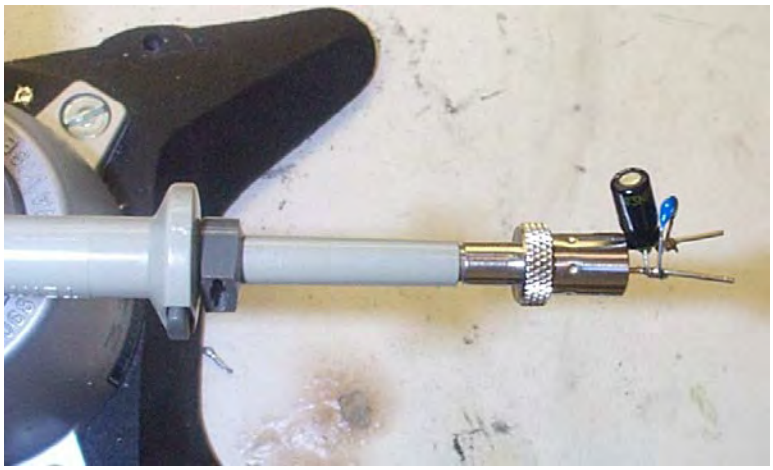

Figure 32 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.3.2 Measurement Results

11.3.3 Measured at the Output Terminal of 3.3 V Output

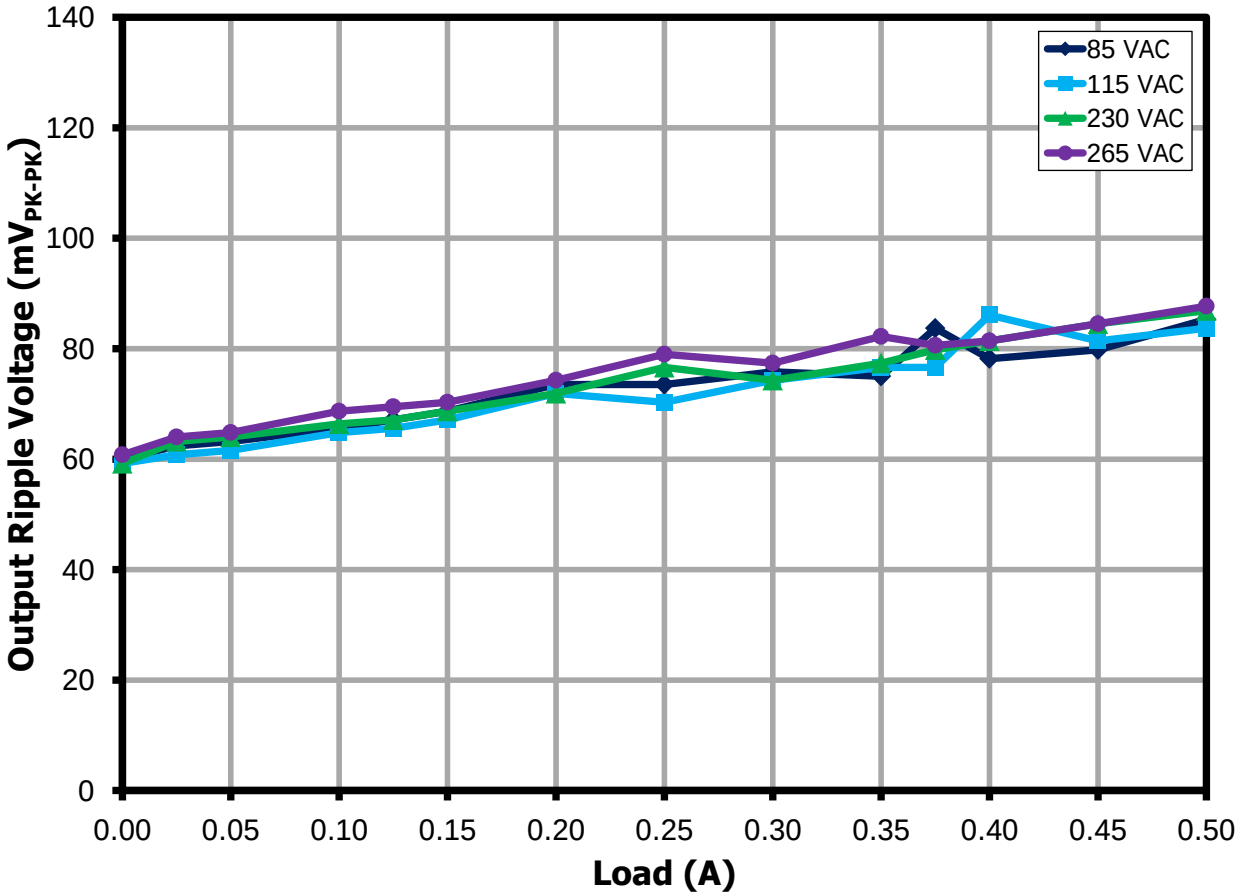

Figure 33 – Output Ripple Voltage at 1.65 W.

85 V RIPPLE (mV_{PK-PK})	115 V RIPPLE (mV_{PK-PK})	230 V RIPPLE (mV_{PK-PK})	265 V RIPPLE (mV_{PK-PK})
85.3	83.7	86.9	87.7

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11.3.4 Output Ripple Voltage Waveforms for 3.3 V Output

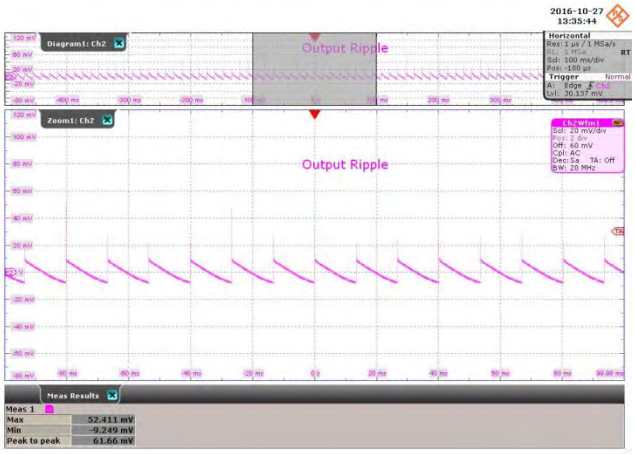


Figure 34 – 85 VAC Input.
Condition: 3.3 V – 0 A.
V_{RIPPLE}, 20 mV / div., 100 ms, 20 ms / div.

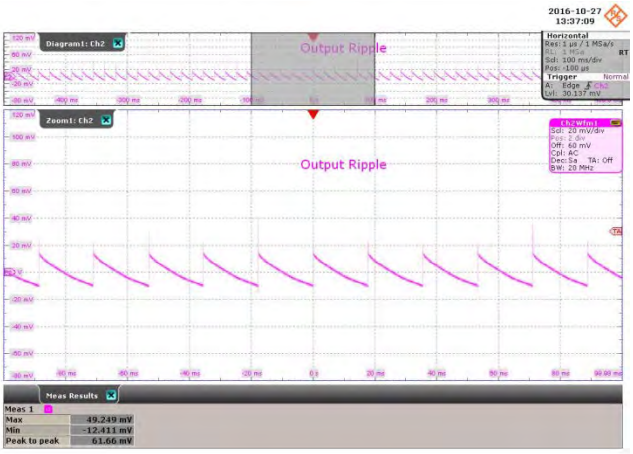


Figure 35 – 265 VAC Input.
Condition: 3.3 V – 0 A.
V_{RIPPLE}, 20 mV / div., 100 ms, 20 ms / div.

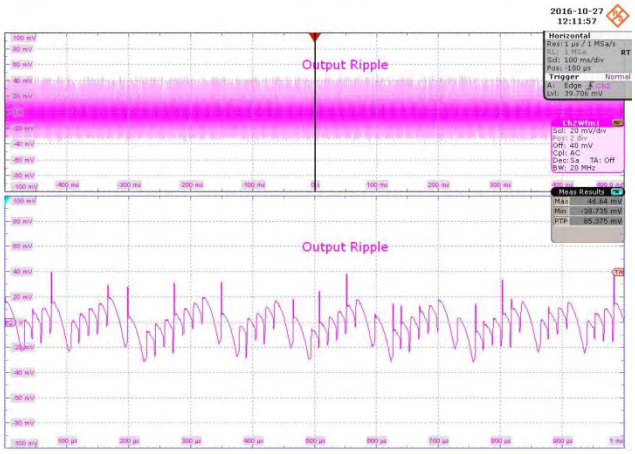


Figure 36 – 85 VAC Input.
Condition:3.3 V – 500 mA.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

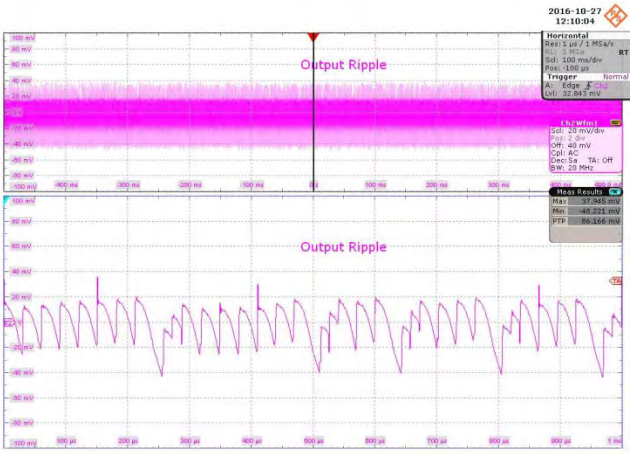


Figure 37 – 265 VAC Input.
Condition: 3.3 V – 500 mA.
V_{RIPPLE}, 20 mV / div., 100 ms, 100 µs / div.

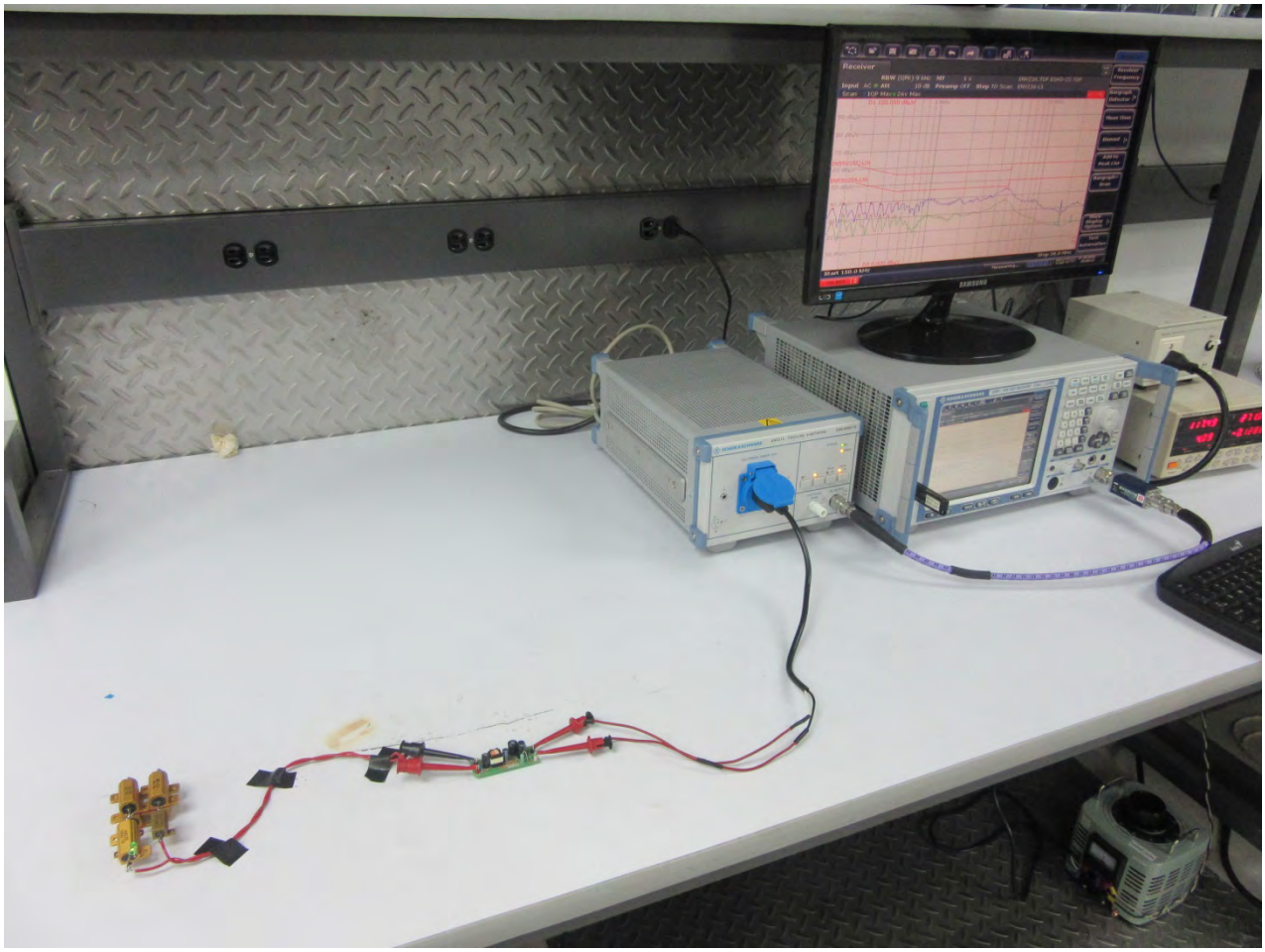
12 Conducted EMI

12.1 *Test Set-up Equipment*

12.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power meter Hi-tester.
4. Chroma measurement test fixture.

12.1.2 Test Set-up



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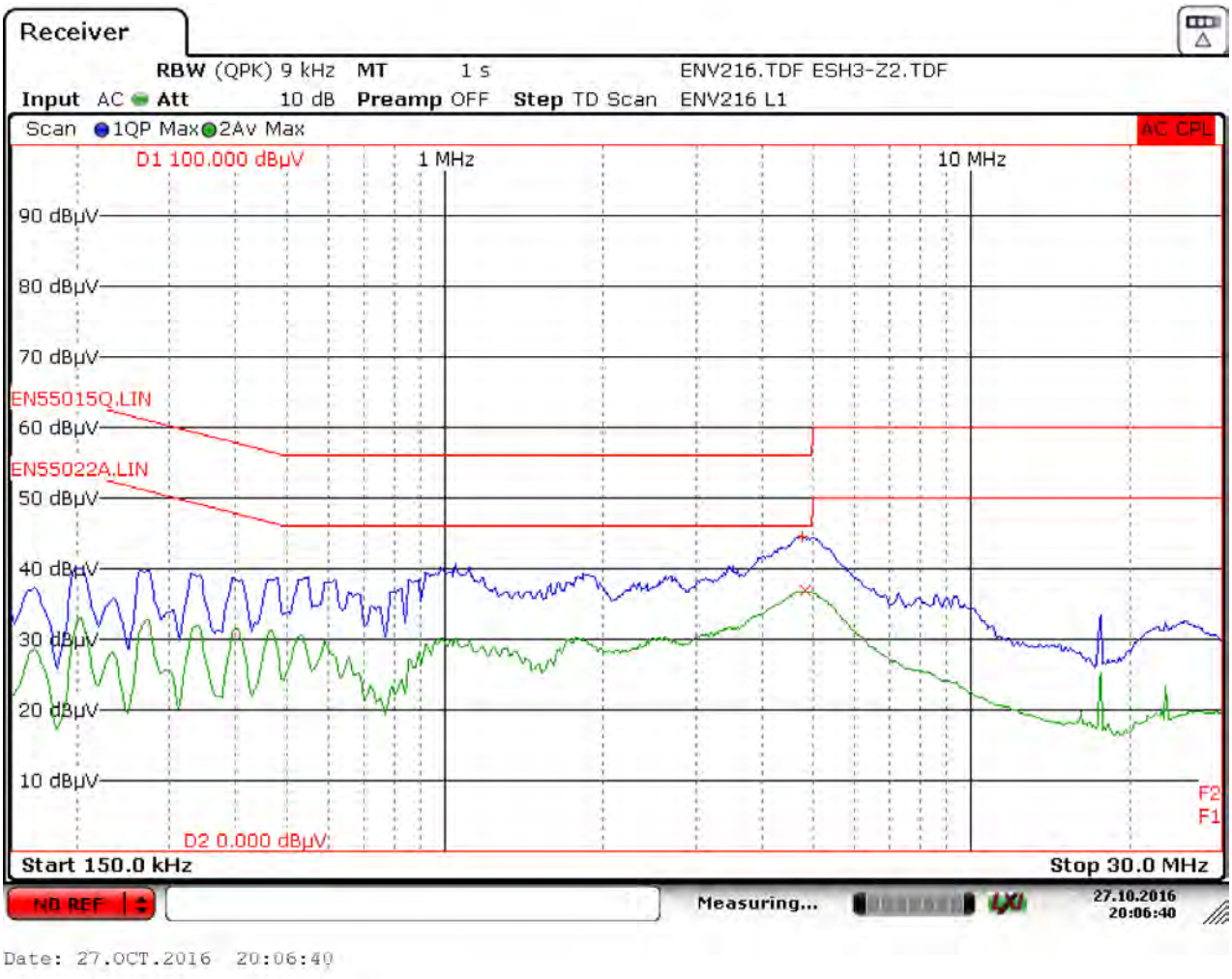
12.2 *Floating Output (QP / AV)*

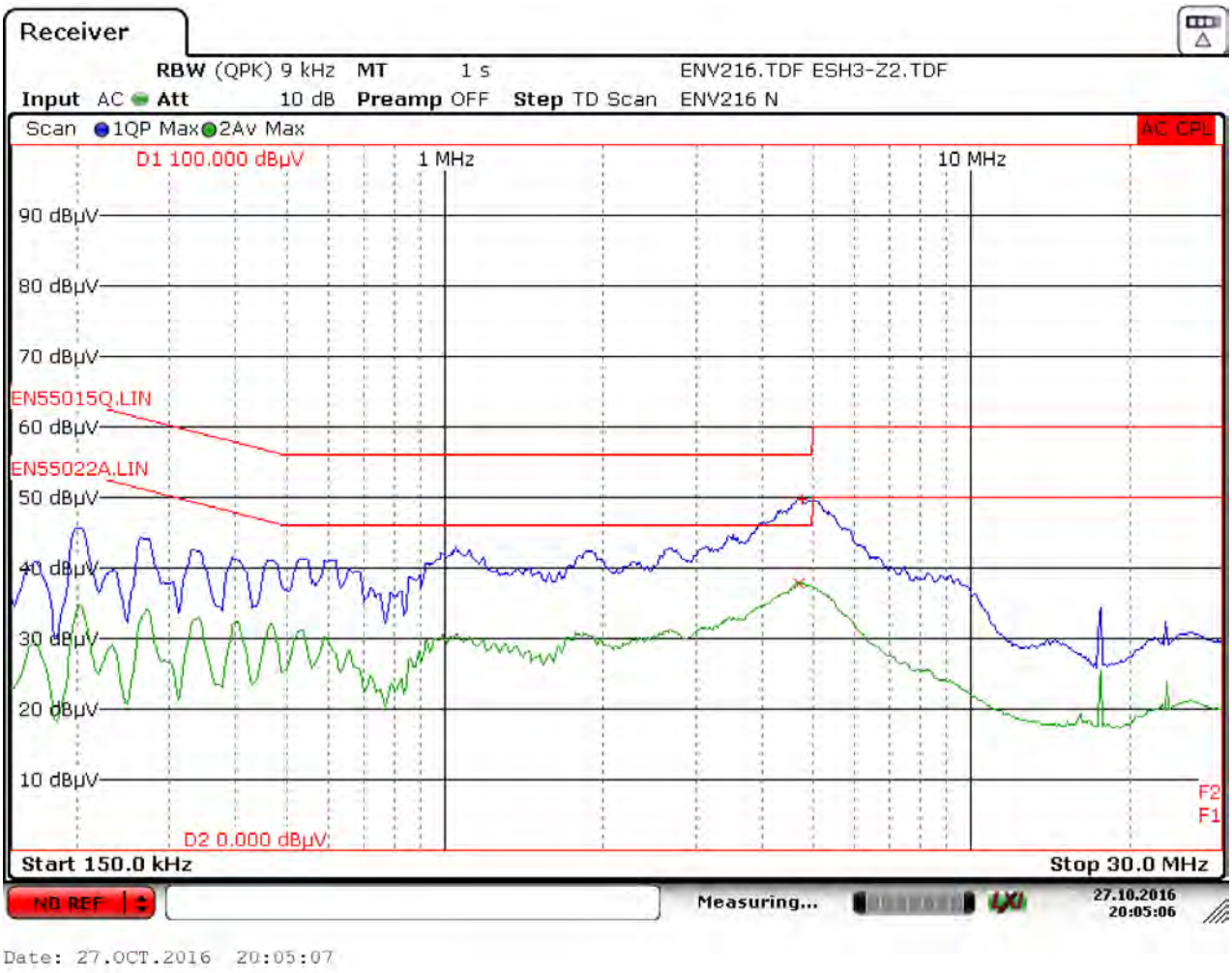
12.2.1 115 VAC



Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	4.8255 MHz	36.85 L1	-9.15 dB
1 Quasi Peak	4.7603 MHz	44.58 L1	-11.42 dB

Figure 38 – Floating Negative Output at 115 VAC, line.



Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	4.7625 MHz	49.86 N	-6.14 dB
2 Average	4.7198 MHz	37.93 N	-8.07 dB

Figure 39 – Floating Negative Output at 115 VAC, Neutral.

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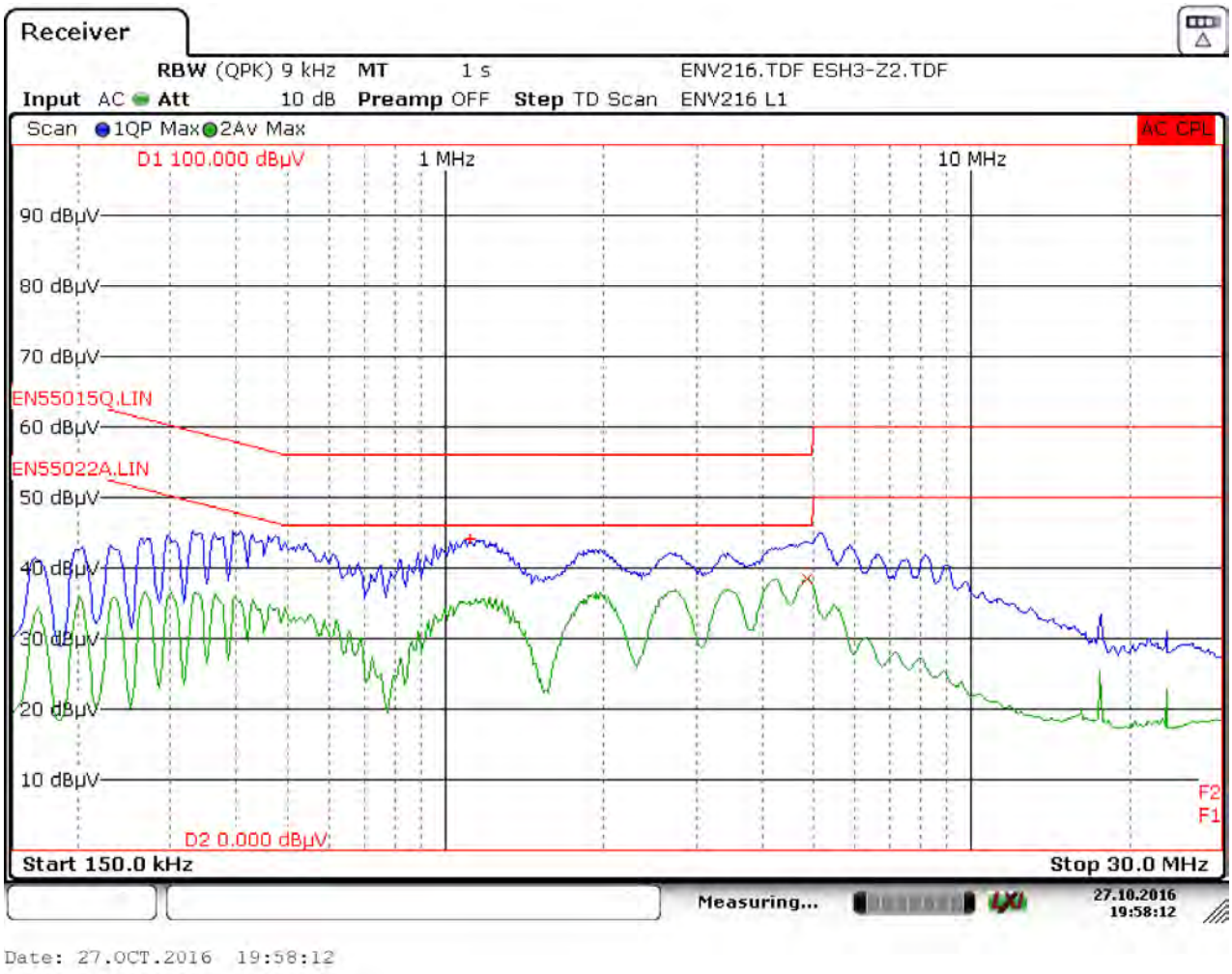
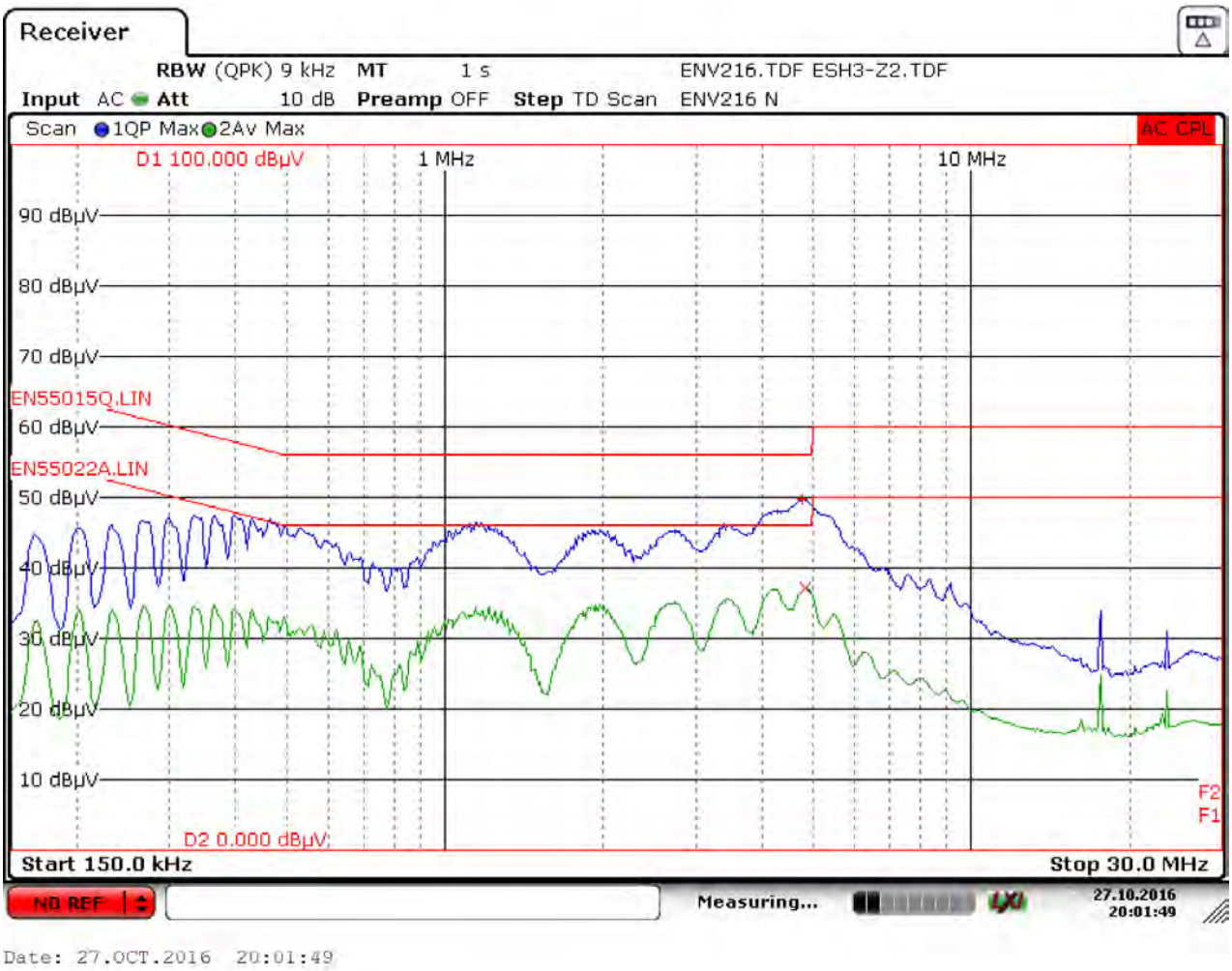
12.2.2 230 VAC



Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	4.8593 MHz	38.45 L1	-7.55 dB
1 Quasi Peak	1.1130 MHz	44.16 L1	-11.84 dB

Figure 40– Floating Negative Output at 230 VAC, line.



Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	4.7828 MHz	49.71 N	-6.29 dB
2 Average	4.8255 MHz	37.13 N	-8.87 dB

Figure 41 – Floating Negative Output at 230 VAC, Neutral.

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13 Surge Test

Test condition: 1.65 W (3.3 V full load, 6.6 Ω resistive load)

13.1 *Differential Mode Surge Test*

Passed ±1 kV, (L1/L2)

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	2	10	PASS
1	90	2	10	PASS
1	180	2	10	PASS
1	270	2	10	PASS
-1	0	2	10	PASS
-1	90	2	10	PASS
-1	180	2	10	PASS
-1	270	2	10	PASS

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
12-Jan-17	JRV	1.0	Initial Release	Mktg & Apps
03-Feb-17	KM	1.1	Minor Corrections	

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