Design Example Report

Title	***65 W Isolated Flyback Power Supply Using InnoSwitch™3-EP PowiGaN™ INN3679C-H606 and MinE-CAP™ MIN1072M***
Specification	90 VAC – 265 VAC Input; 20 V, 3.25 A Output
Application	Adapters
Author	Applications Engineering Department
Document Number	DER-713
Date	March 25, 2021
Revision	1.0

Summary and Features

- 65 W output power capability at 20 V
- Very high power density design enabled by MinE-CAP MIN1072M
- >92% average efficiency at nominal AC inputs
- <50 mW no-load input power at nominal AC inputs
- Integrate protection and reliability features
  - Output short-circuit
  - Line and output OVP
  - Over-temperature shutdown
- Synchronous rectification for higher efficiency
- Input voltage monitor with accurate brown-in/brown-out protection
- Meets EN55022 and CISPR-22 Class B conducted EMI
- Meets IEC 1.0 kV differential surge
- ±16 kV ESD Class B

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes an isolated flyback converter designed to provide a 20 V 3.25 A output from a wide input voltage range of 90 VAC to 265 VAC. This power supply utilizes the INN3679C-H606 from the InnoSwitch3-EP family of IC's.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

Figure 1 – Prototype Top View

Figure 2 – Prototype Bottom View

Note: PCB vias should be solder-filled.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				<50	mW	
Output						
Output Voltage	V_{OUT}	19	20	21	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			450	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			3.25	A	
Total Output Power						
Continuous Output Power	P_{OUT}			65	W	
Efficiency						
Full Load @ 115 VAC	η	92			%	
Full Load @ 230 VAC	η	93			%	Measured at P_{OUT} 25 °C.
Average @ 115 VAC	η	92			%	
Average @ 230 VAC	η	93			%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				1	kV	1.2/50 µs Surge, IEC 61000-4-5, Impedance: 2 Ω
ESD – Air Discharge				±16	kV	
ESD – Contact Discharge				±8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 Schematic

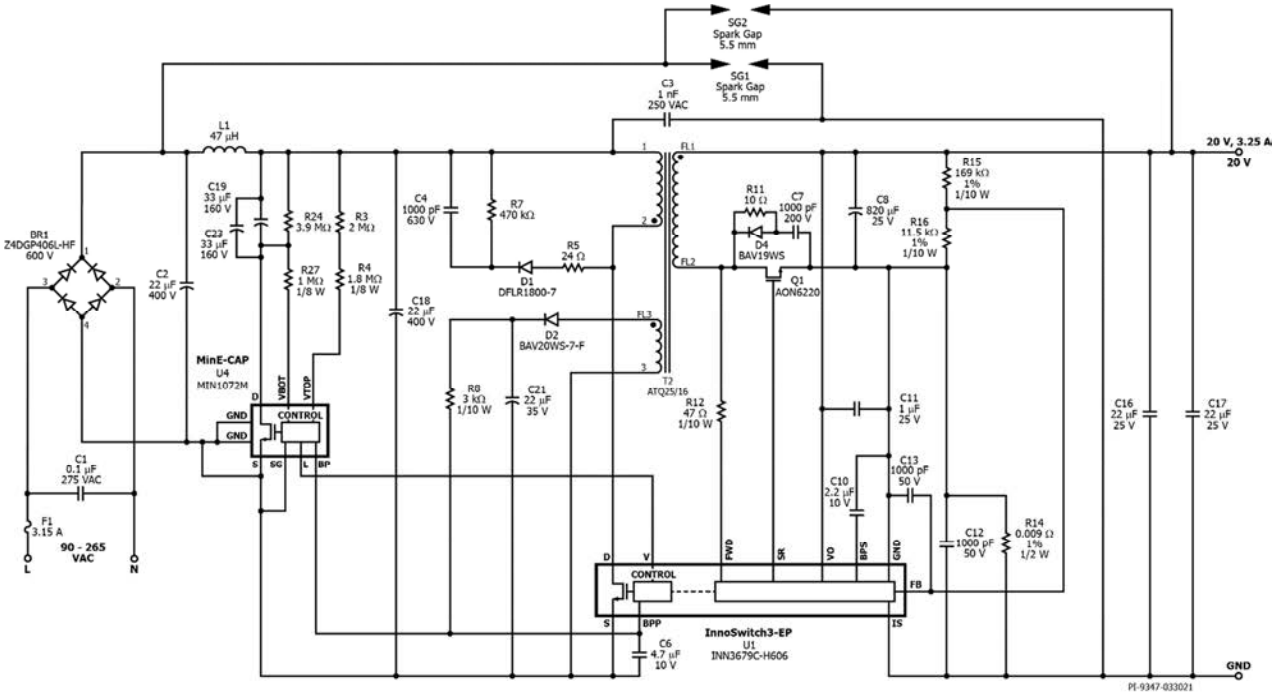

Figure 3 – Schematic.

4 Circuit Description

The InnoSwitch3-EP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification, and the Fluxlink™ technology which eliminates the optocoupler needed on a secondary-sensed feedback system.

4.1 *Input Rectifier and Filter*

Fuse F1 isolates the circuit and provides protection from component failure. Bridge rectifier BR1 converts the AC line voltage into the DC voltage seen across the input filter network. EMI filtering is provided by the X capacitor C1 and mainly by the pi filter combination of C2, L1, and C18. Capacitors C19 and C23 further bolsters EMI suppression at lower input voltages.

4.2 *MinE-CAP MIN1072M*

The MinE-CAP U4 basically connects the low voltage (LV) capacitors C19 and C23 when the input voltage is low and disconnects both capacitors when the input voltage is high. By connecting the L pin to the V pin of the Innoswitch3-EP IC, the MinE-CAP provides the input AC input information to the InnoSwitch3-EP IC for undervoltage and overvoltage levels. MinE-CAP also reduces inrush currents by way of controlled charging of the LV capacitors thereby eliminating the need for inrush NTC's. Information needed for proper control is provided by the network of sense resistors R3 and R4 and R27 via the voltages measured on the VTOP and VBOT pins. R24 is a bleeder resistor used to help regulate the voltage across the LV capacitor.

4.3 *InnoSwitch3-EP Primary-Side*

The primary-side of INN3679C IC combines a high-voltage power MOSFET and the primary-side controller into a low cost monolithic IC.

When AC is first applied, an internal current source connected to the DRAIN (D) pin charges C6 to power the controller inside the IC. During steady-state, the device controller will now be powered via a bias winding through the current limiting resistor R8 to minimize losses.

The power transformer T2 is designed for a flyback topology power supply. The start winding of the transformer is connected to the DRAIN pin of the MOSFET inside the INN3679C IC, while the end of the winding is connected to the rectified DC bus. A low cost RCD clamp consisting of diode D1, capacitor C4, and resistors R5 and R7 limits to acceptable levels the effects of leakage energy generated by the transformer leakage inductance.

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4.4 *InnoSwitch3-EP Secondary-Side*

The secondary-side of INN3679C provides output voltage sensing, output current sensing, and internal gate driver for a synchronous rectifier (SR) MOSFET. The secondary-side is powered by an internal 4.4 V regulator which draws current from either VOUT pin or the current-limited FWD pin via R12. Its output is connected to an external decoupling capacitor C10, also referred to as BPS capacitor.

The FWD pin also provides negative edge detection by sensing the transformer's secondary pin through resistor R12. The voltage sensed by the FWD pin is used for both the primary-secondary handshake at start-up, and for timing the turn-on instant of the SR FET Q1. This ensures quasi-resonant operation when operating at discontinuous conduction mode (DCM).

The SR FET Q1 is driven by the SR pin of U1. The RCD snubber consisting of R11, C7, and D4 limits the drain to source voltage spike across the SR FET.

The feedback network comprised of resistors R15 and R16, and capacitor C13 is connected between the output voltage and secondary ground. The sensed voltage across R16 is connected to the FB pin. The external current sense resistor R14 connected between the ISENSE and SECONDARY GROUND pins sets the maximum output current limit.

A low ESR capacitor C8 provides output filtering. Output voltage ripple is further reduced by the ceramic capacitors C16 and C17.

5 PCB Layout

PCB material: FR4, Thickness: 1 mm, Copper: 2 layers, 2 oz.
Max PSU Height: 23 mm

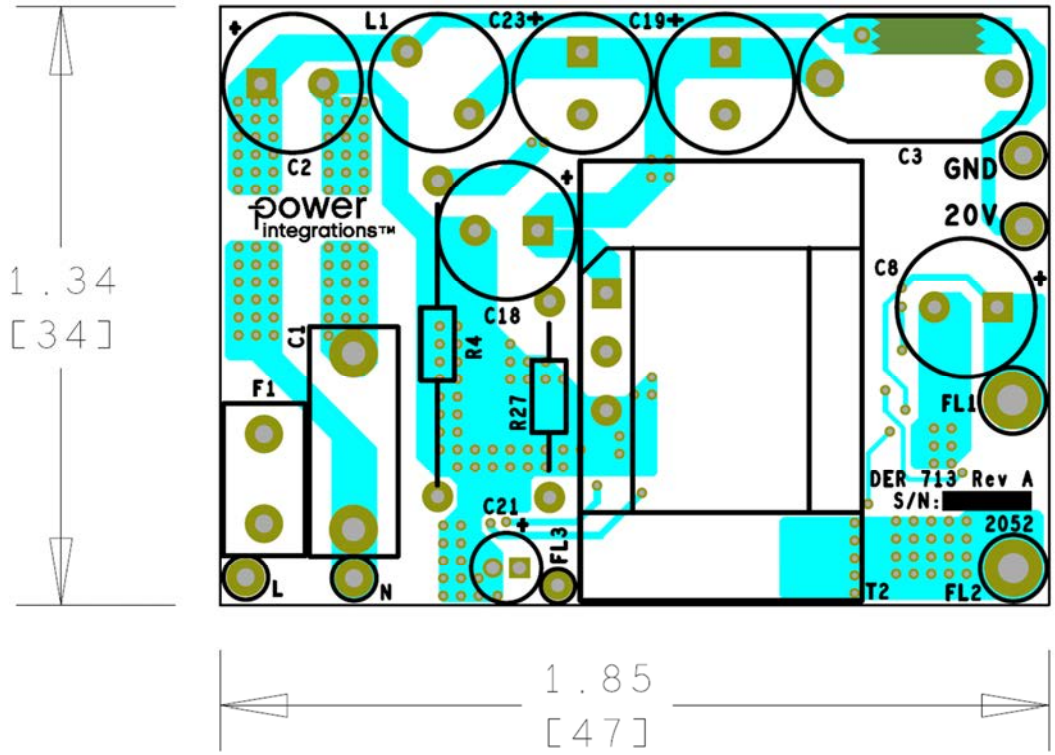

Figure 4 – Populated Circuit Board, Top View.

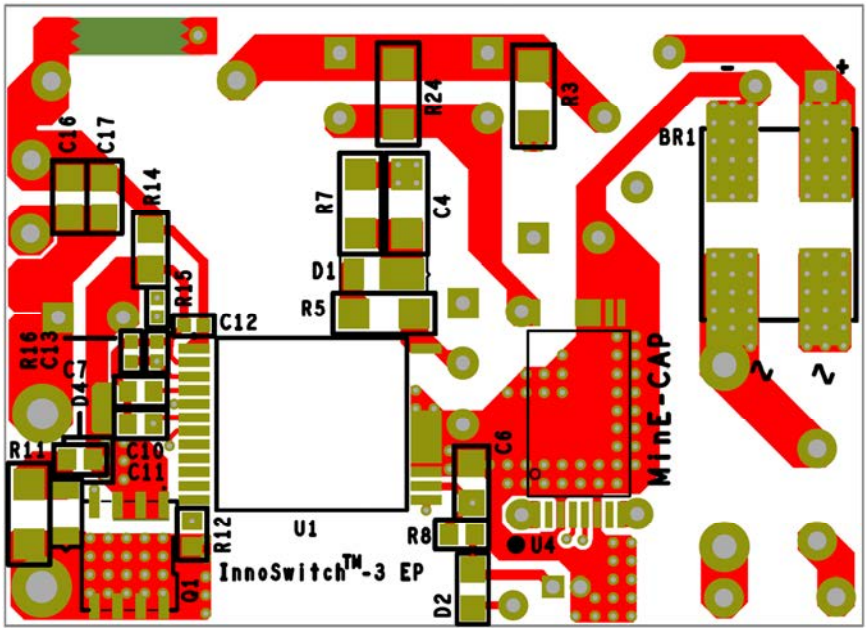

Figure 5 – Populated Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 600 V, 4 A, Z4-D, -55°C ~ 175°C (TJ)	Z4DGP406L-HF	Comchip
2	1	C1	0.1 µF, 20%, 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	1	C2, C18	22 µF, 400 V, Electrolytic, 8 x 16	ERK2G9220F16OTO	Aishi
4	1	C3	1 nF, 250 VAC, Ceramic, Y1	440LD10-R	Vishay
5	1	C4	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
6	1	C6	4.7 µF ±10% 10V Ceramic X7R 0805	LMK212B7475KGHT	Taiyu Yuden
7	1	C7	1000 pF, 200 V, Ceramic, X7R, 0603	06032C102KAT2A	AVX
8	1	C8	820 µF, 25 V, Electrolytic, Low ESR, (8 x 16)	SPZ1EM821F16O00RAXXX	Aishi
9	1	C10	2.2 µF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
10	1	C11	1 µF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
11	2	C12, C13	1000 pF, ±10%, 50 V, X7R, -55°C ~ 125°C, Low ESL, 0402	C0402C102K5RACTU	Kemet
12	2	C16, C17	22 µF, ±20%, 25 V, Ceramic, X5R, 0805	GRM21BR61E226ME44L	Murata
13	1	C19, C23	33 µF, 160 V, Electrolytic, Low ESR, (8 x 16)	EWH2CM330F16OT	Aishi
14	1	C21	22 µF, 35 V, Electrolytic, Gen. Purpose, (4 x 12.5)	UVR1V220MDD6TP	Nichicon
15	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
16	1	D2	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
17	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
18	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
19	1	L1	47 µH, ±10%, Unshielded, Wirewound Inductor, 1.56 A, 140 mΩ Max, Radial	RLB0914-470KL	Bourns
20	1	Q1	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
21	1	R3	RES, 2.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
22	1	R4	RES, 1.8 MΩ, 5%, 1/8 W, Carbon Film	CF18JT1M80	Stackpole
23	1	R5	RES, 24 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ240V	Panasonic
24	1	R7	RES, 470 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic
25	1	R8	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
26	1	R11	RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
27	1	R12	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
28	1	R14	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
29	1	R15	RES, 169.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1693X	Panasonic
30	1	R16	RES, 11.5 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1152X	Panasonic
31	1	R24	RES, 3.9 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ395V	Panasonic
32	1	R27	RES, 1 MΩ, 5%, 1/8 W, Carbon Film	299-1M-RC	Xicon
33	1	T2	Bobbin, ATQ25/16, Horizontal, 8 pins		
34	1	U1	InnoSwitch-4, InSOP24D	INN3679C-H606	Power Integrations
35	1	U4	MinE-CAP	MIN1072M	Power Integrations

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	20V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
2	2	GND, L	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

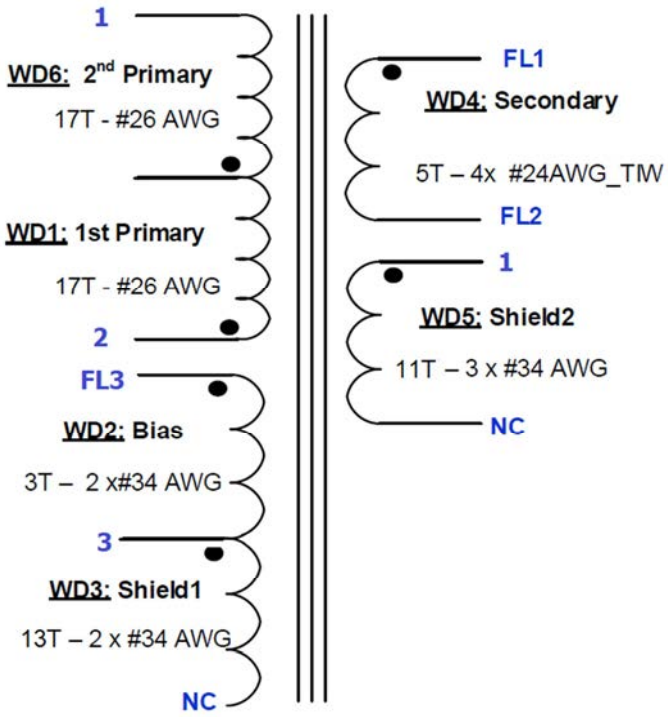

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and pin 5 with all other windings open.	531 µH
Tolerance	Tolerance of Primary Inductance.	±5 %
Leakage Inductance	Measured across primary winding with all other windings shorted.	<6 µH

7.3 *Material List*

Item	Description
[1]	Core: ATQ25/16 3C95.
[2]	Bobbin: ATQ25/16, Vertical, 8 Pins.
[3]	Magnet Wire: #26 AWG.
[4]	Magnet Wire: #34 AWG.
[5]	Tripe Insulated Wire: #24 AWG.
[6]	Polyester Tape: 8 mm.
[7]	Polyester Tape: 16.7 mm.
[8]	Polyester Tape: 10 mm x 15 mm.
[9]	Varnish: Dolph BC 359 or Equivalent.

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7.4 *Transformer Build Diagram*

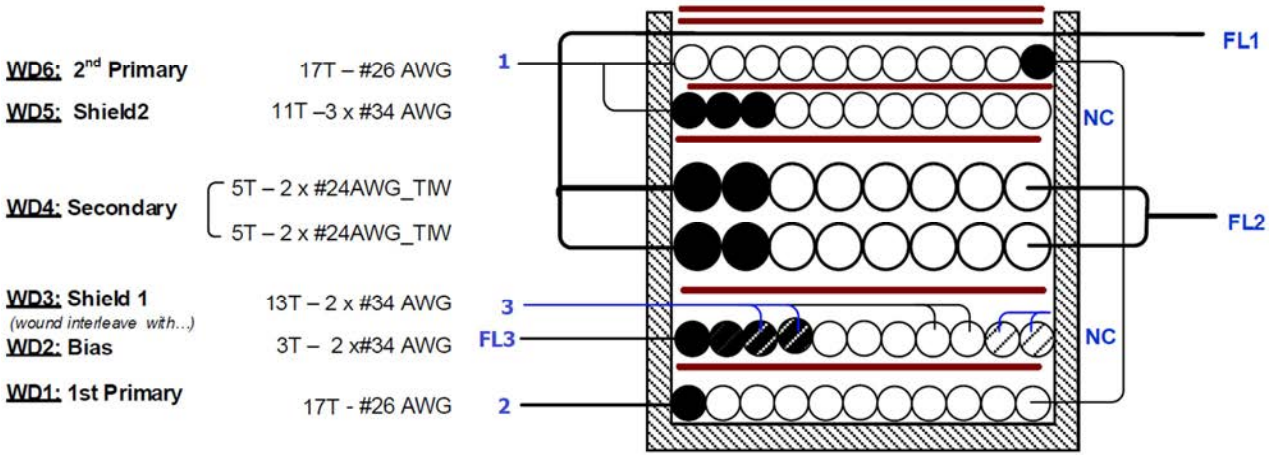
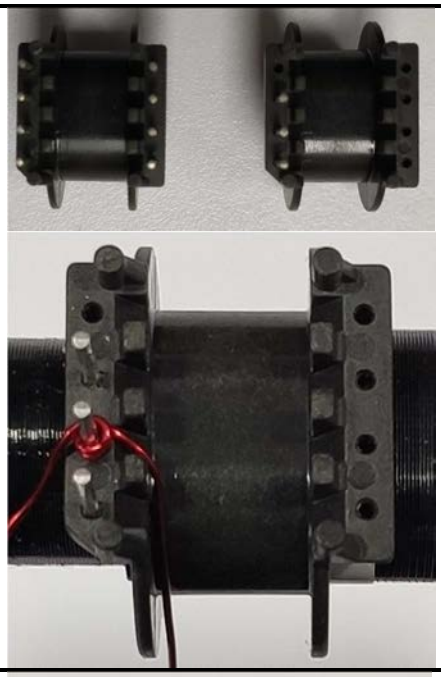
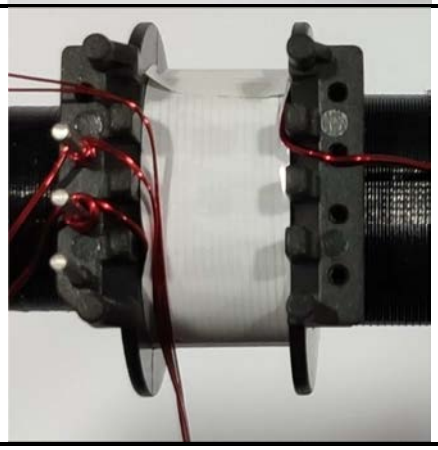


Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Bobbin Preparation	For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 4, 5, 6, 7, and 8.
WD1 1st Primary	Start at pin 2, wind 17 turns of wire Item [3] in a single layer. Leave ~3 feet long for 2nd primary winding.
Insulation	1 layer of tape Item [6]
WD2: Bias Winding, WD3: Shield Winding	Prepare 4 strands of wire Item [4] for both windings. For WD2, start 2 strands of the wire as FL3 and leave ~13 mm length of excess wire. For WD3, start the other 2 strands at pin 3. Wind all 4 wires in parallel. At the 3rd turn, place a piece of tape to hold the wires and terminate WD2 to pin 3. Continue WD3 for 10 more turns and then cut the wire to leave it as No-Connect.
Insulation	1 layer of tape Item [6]
WD4 Secondary	Start at left side of the bobbin. Use 2 wires Item [5], and leave ~25 mm length of excess wire, then mark as FL1. Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right side of the bobbin, also leaving ~15 mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation	1 layer of tape Item [6]
WD5 Shield2	Start at pin 1, wind 11 turns of 3 strands of wire Item [4] in 1 layer. Finish the winding at the right side and then cut the wire to leave it as No-Connect.
Insulation	1 layer of tape Item [6]
WD6 2nd Primary	Use hanging wire from WD1 and continue winding 16 turns from right to left. Bring 4 wires marked as FL1 to the right before finishing the last turn of WD6 at pin 1.
Insulation	2 layers of tape Item [6]
Finish	Gap cores to get 531 µH. Wrap the body of transformer with 2 layers of tape Item [7]. Use Item [8] to wrap both bottom secondary side halves of the exposed core as shown. Varnish using Item [9].

7.6 *Transformer Winding Illustrations*

Bobbin Preparation		For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 4, 5, 6, 7, and 8.
WD1 1st Primary		Start at pin 2, wind 17 turns of wire Item [3] in a single layer. Leave ~3 feet long for 2nd primary winding.
Insulation		1 layer of tape Item [6]

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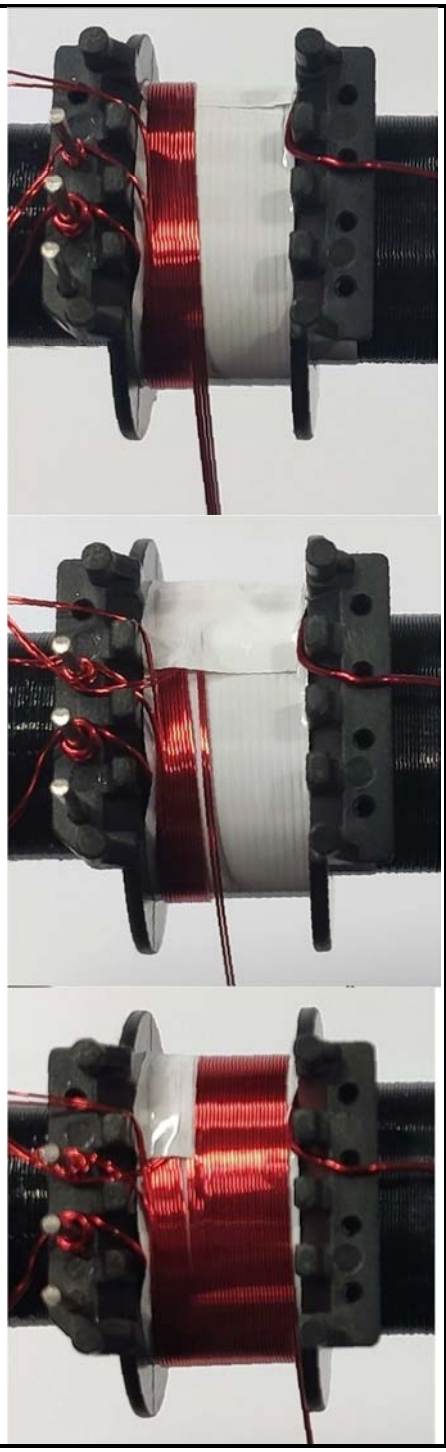
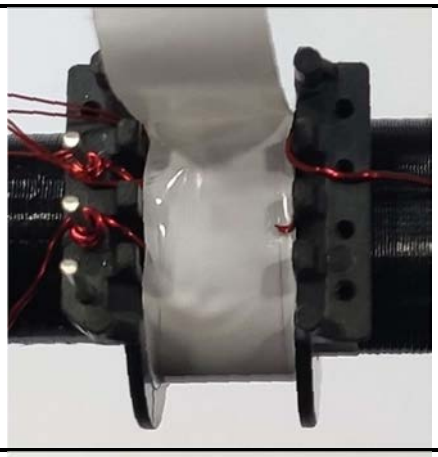
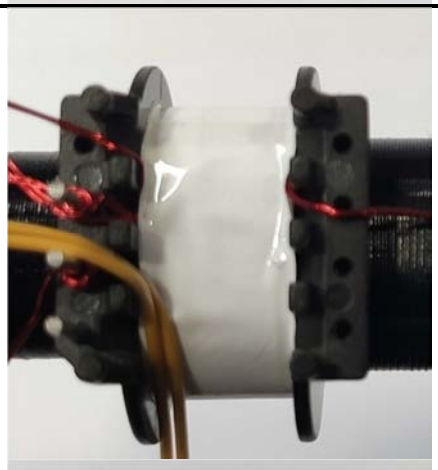
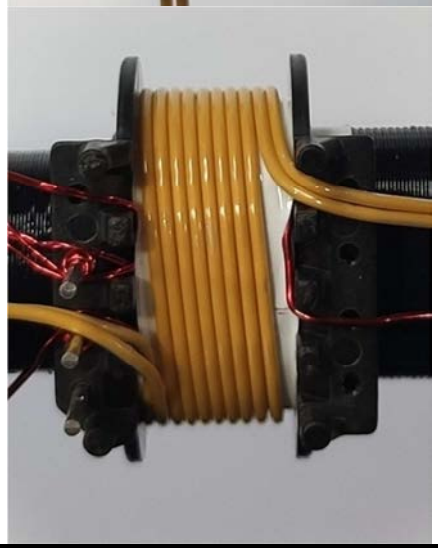
WD2: Bias Winding, WD3: Shield Winding		Prepare 4 strands of wire Item [4] for both windings. For WD2, start 2 strands of the wire as FL3 and leave ~13 mm length of excess wire. For WD3, start the other 2 strands at pin 3. Wind all 4 wires in parallel. At the 3rd turn, place a piece of tape to hold the wires and terminate WD2 to pin 3. Continue WD3 for 10 more turns and then cut the wire to leave it as No-Connect.

Insulation		1 layer of tape Item [6]
WD4 Secondary	 	Start at left side of the bobbin. Use 2 wires Item [5], and leave ~25 mm length of excess wire, then mark as FL1. Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right side of the bobbin, also leaving ~15 mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.

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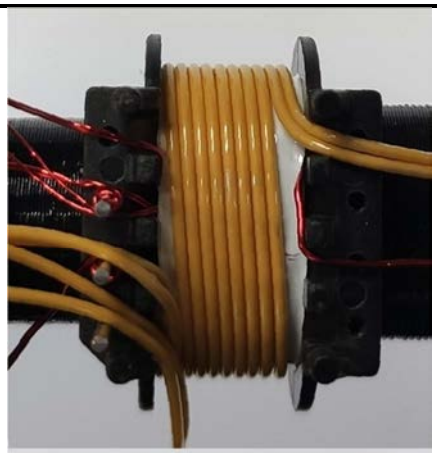
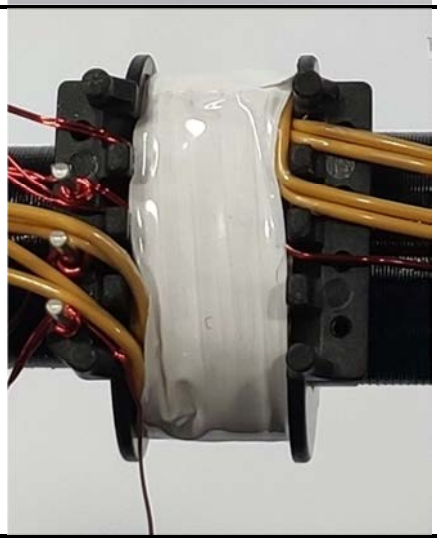
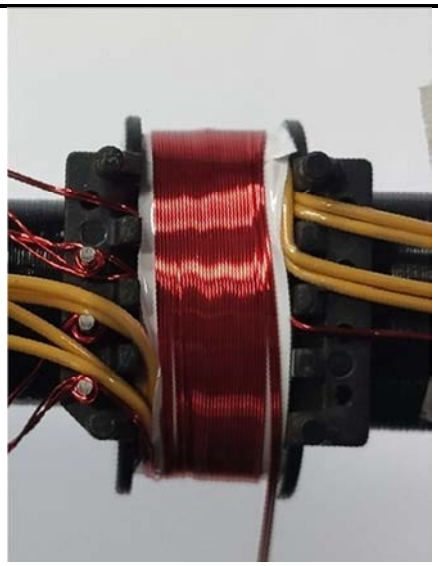
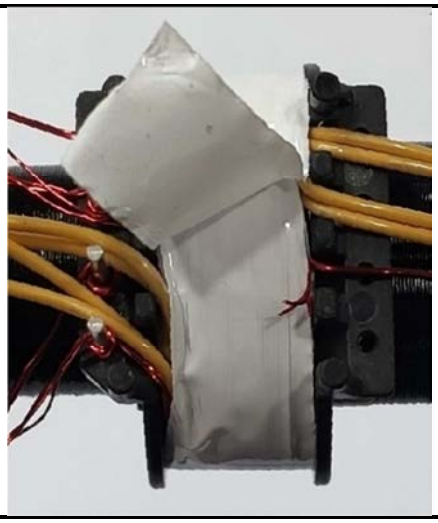
	 	
Insulation		1 layer of tape Item [6]

WD5 Shield2		Start at pin 1, wind 11 turns of 3 strands of wire Item [4] in 1 layer. Finish the winding at the right side and then cut the wire to leave it as No-Connect.
Insulation		1 layer of tape Item [6]

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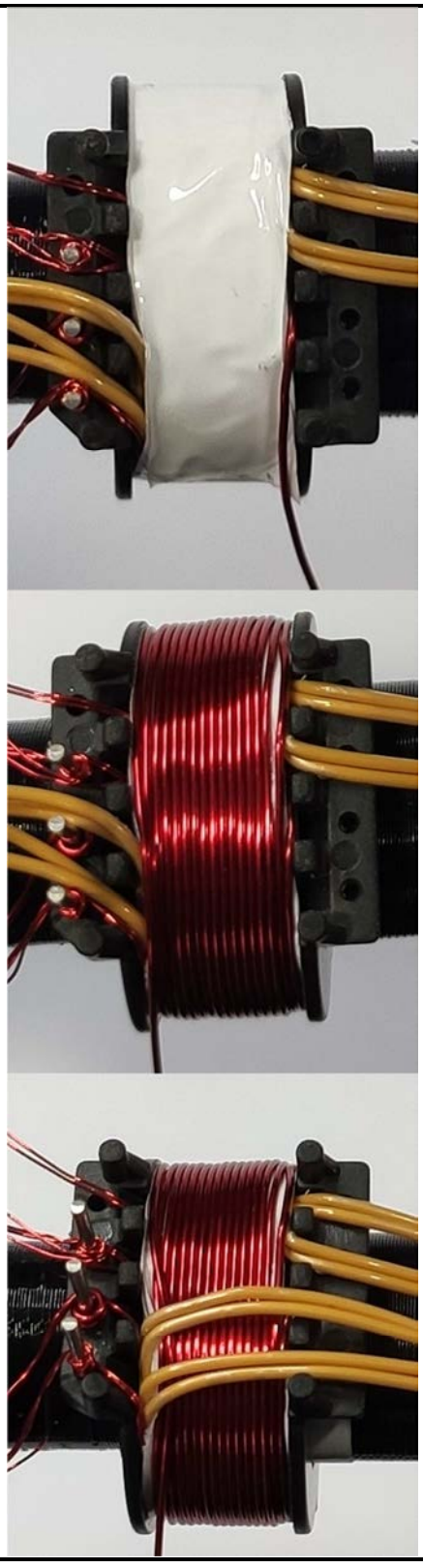
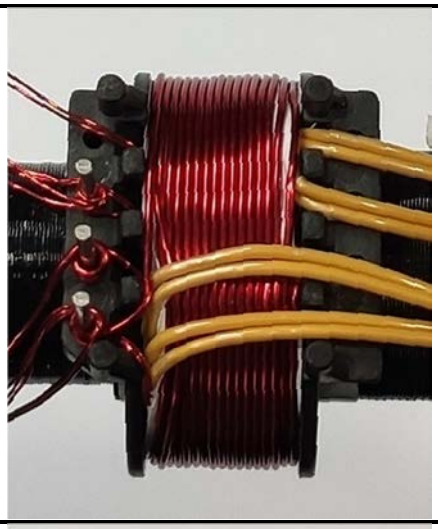
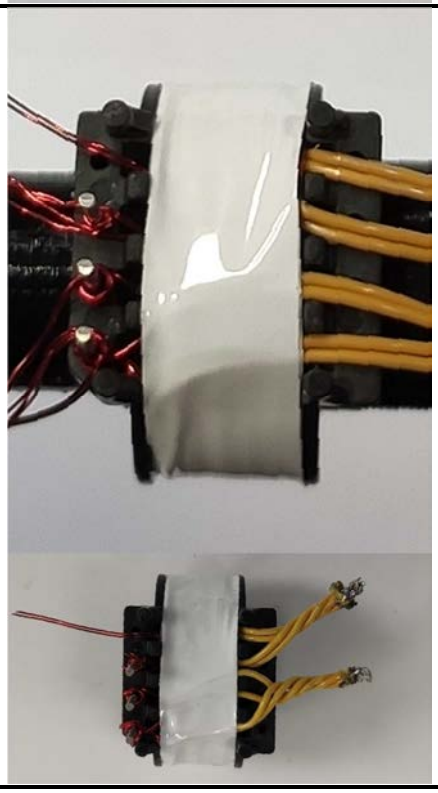
WD6 **2nd Primary**		Use hanging wire from WD1 and continue winding 16 turns from right to left. Bring 4 wires marked as FL1 to the right before finishing the last turn of WD6 at pin 1.

		
Insulation		2 layers of tape Item [6]

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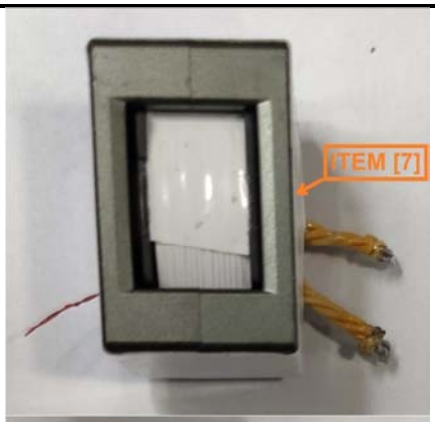
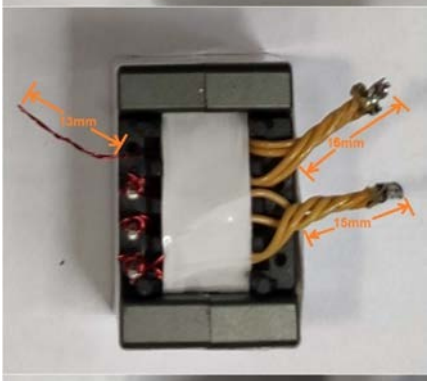
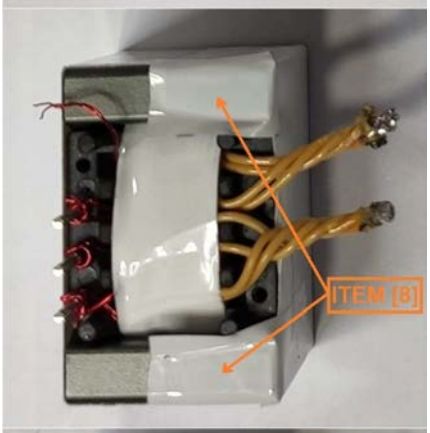
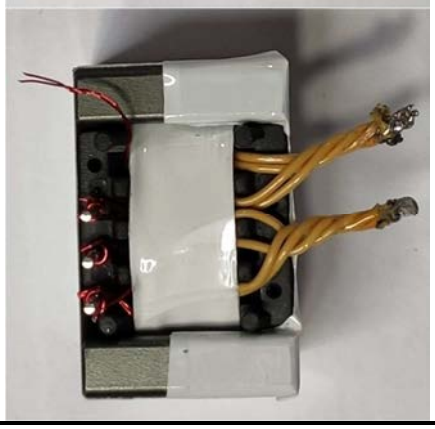
Finish	   	Gap cores to get 531 uH. Wrap the body of transformer with 2 layers of tape Item [7]. Use Item [8] to wrap both bottom secondary side halves of the exposed core as shown. Varnish using Item [9].

8 Design Spreadsheet

1	ACDC_InnoSwitch3-EP_Flyback_090320; Rev.1.6; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN	90		90	V	Minimum AC input voltage
4	VIN_MAX			265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	110.0		110.0	uF	Input capacitor
8	VOUT	20.00		20.00	V	Output voltage at the board
9	CDC			0.00	mV	Cable drop compensation desired at full load
10	IOUT	3.250		3.250	A	Output current
11	POUT			65.00	W	Output power
12	EFFICIENCY	0.91		0.91		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
15	**PRIMARY CONTROLLER SELECTION**					
16	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
17	DEVICE_GENERIC	INN36X9		INN36X9		Generic device code
18	DEVICE_CODE			INN3679C		Actual device code
19	POUT_MAX			75	W	Power capability of the device based on thermal performance
20	RDSON_100DEG			0.62	Ω	Primary switch on time drain resistance at 100 degC
21	ILIMIT_MIN			1.980	A	Minimum current limit of the primary switch
22	ILIMIT_TYP			2.130	A	Typical current limit of the primary switch
23	ILIMIT_MAX			2.279	A	Maximum current limit of the primary switch
24	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
25	VDRAIN_ON_PRSW			0.47	V	Primary switch on time drain voltage
26	VDRAIN_OFF_PRSW			578.4	V	Peak drain voltage on the primary switch during turn-off
27	**WORST CASE ELECTRICAL PARAMETERS**					
28	FSWITCHING_MAX	80000		80000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
29	VOR	135.0		135.0	V	Secondary voltage reflected to the primary when the primary switch turns off
30	VMIN			90.14	V	Valley of the minimum input AC voltage at full load
31	KP			0.68		Measure of continuous/discontinuous mode of operation
32	MODE_OPERATION			CCM		Mode of operation
33	DUTYCYCLE			0.601		Primary switch duty cycle
34	TIME_ON			11.97	us	Primary switch on-time
35	TIME_OFF			4.99	us	Primary switch off-time
36	LPRIMARY_MIN			504.7	uH	Minimum primary inductance

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37	LPRIMARY_TYP			531.2	uH	Typical primary inductance
38	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
39	LPRIMARY_MAX			557.8	uH	Maximum primary inductance
40	**PRIMARY CURRENT**					
41	IPEAK_PRIMARY			2.141	A	Primary switch peak current
42	IPEDESTAL_PRIMARY			0.617	A	Primary switch current pedestal
43	IAVG_PRIMARY			0.761	A	Primary switch average current
44	IRIPPLE_PRIMARY			1.749	A	Primary switch ripple current
45	IRMS_PRIMARY			1.057	A	Primary switch RMS current
46	**SECONDARY CURRENT**					
47	IPEAK_SECONDARY			14.556	A	Secondary winding peak current
48	IPEDESTAL_SECONDARY			4.193	A	Secondary winding current pedestal
49	IRMS_SECONDARY			5.855	A	Secondary winding RMS current
50	**TRANSFORMER CONSTRUCTION PARAMETERS**					
51	**CORE SELECTION**					
52	CORE	ATQ25/16	Info	ATQ25/16		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
53	CORE CODE			ATQ25/16		Core code
54	AE			102.00	mm^2	Core cross sectional area
55	LE			40.80	mm	Core magnetic path length
56	AL			6700	nH/turns^2	Ungapped core effective inductance
57	VE			4162.0	mm^3	Core volume
58	BOBBIN			TBI-238-09011.11XX		Bobbin
59	AW			25.60	mm^2	Window area of the bobbin
60	BW			8.00	mm	Bobbin width
61	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
62	**PRIMARY WINDING**					
63	NPRIMARY			34		Primary turns
64	BPEAK			3752	Gauss	Peak flux density
65	BMAX			3401	Gauss	Maximum flux density
66	BAC			1365	Gauss	AC flux density (0.5 x Peak to Peak)
67	ALG			460	nH/turns^2	Typical gapped core effective inductance
68	LG			0.260	mm	Core gap length
69	LAYERS_PRIMARY			2		Number of primary layers
70	AWG_PRIMARY			26	AWG	Primary winding wire AWG
71	OD_PRIMARY_INSULATED			0.465	mm	Primary winding wire outer diameter with insulation
72	OD_PRIMARY_BARE			0.405	mm	Primary winding wire outer diameter without insulation
73	CMA_PRIMARY			241	Cmil/A	Primary winding wire CMA
74	**SECONDARY WINDING**					
75	NSECONDARY	5		5		Secondary turns
76	AWG_SECONDARY			19	AWG	Secondary winding wire AWG
77	OD_SECONDARY_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation

78	OD_SECONDARY_BARE			0.912	mm	Secondary winding wire outer diameter without insulation
79	CMA_SECONDARY			220	Cmil/A	Secondary winding wire CMA
80	**BIAS WINDING**					
81	NBIAS			3		Bias turns
82	**PRIMARY COMPONENTS SELECTION**					
83	**LINE UNDERVOLTAGE**					
84	BROWN-IN REQURED			72.0	V	Required AC RMS line voltage brown-in threshold
85	RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
86	BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
87	BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
88	**LINE OVERVOLTAGE**					
89	OVERVOLTAGE_LINE			304.2	V	Actual AC RMS line over-voltage threshold
90	**BIAS DIODE**					
91	VBIAS	11.0		11.0	V	Rectified bias voltage
92	VF_BIAS			0.70	V	Bias winding diode forward drop
93	VREVERSE_BIASDIODE			43.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
94	CBIAS			22	uF	Bias winding rectification capacitor
95	CBPP			4.70	uF	BPP pin capacitor
96	**SECONDARY COMPONENTS**					
97	RFB_UPPER	169.00		169.00	kΩ	Upper feedback resistor (connected to the first output voltage)
98	RFB_LOWER			11.50	kΩ	Lower feedback resistor
99	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
100	**MULTIPLE OUTPUT PARAMETERS**					
101	OUTPUT 1					
102	VOUT1			20.00	V	Output 1 voltage
103	IOUT1			3.25	A	Output 1 current
104	POUT1			65.00	W	Output 1 power
105	IRMS_SECONDARY1			5.855	A	Root mean squared value of the secondary current for output 1
106	IRIPPLE_CAP_OUTPUT1			4.871	A	Current ripple on the secondary waveform for output 1
107	AWG_SECONDARY1			19	AWG	Wire size for output 1
108	OD_SECONDARY1_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation for output 1
109	OD_SECONDARY1_BARE			0.912	mm	Secondary winding wire outer diameter without insulation for output 1
110	CM_SECONDARY1			1171	Cmils	Bare conductor effective area in circular mils for output 1
111	NSECONDARY1			5		Number of turns for output 1
112	VREVERSE_RECTIFIER1			74.91	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
113	SRFET1	AUTO		AO4294		Secondary rectifier (Logic

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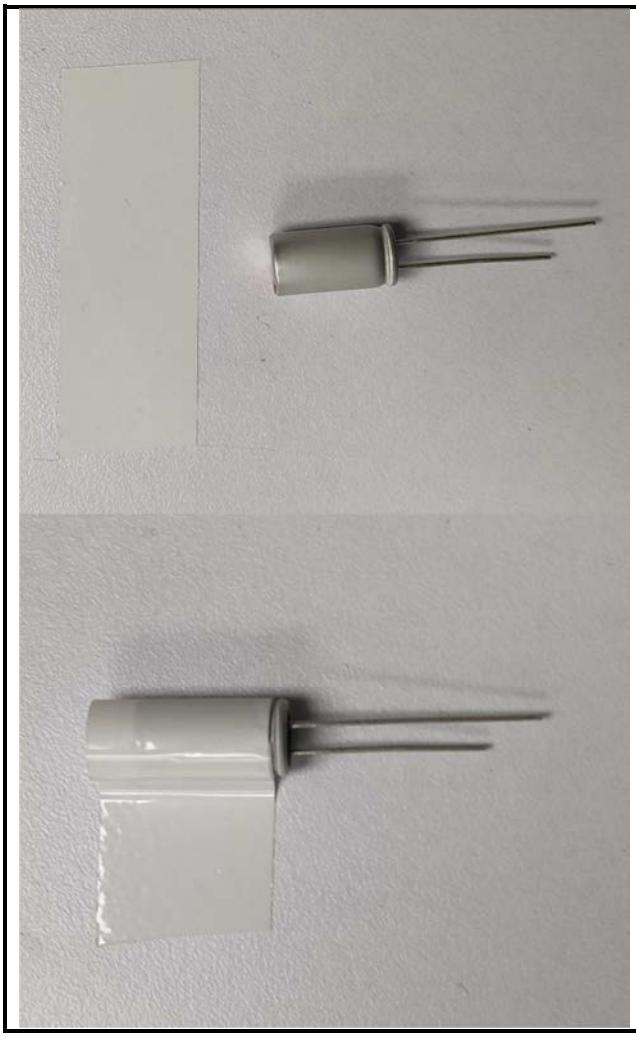
						MOSFET) for output 1
114	VF_SRFET1			0.050	V	SRFET on-time drain voltage for output 1
115	VBREAKDOWN_SRFET1			100	V	SRFET breakdown voltage for output 1
116	RDSON_SRFET1			15.5	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
117	PO_TOTAL			65.00	W	Total power of all outputs
118	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
119	**TOLERANCE ANALYSIS**					
120	USER_VAC			90	V	Input AC RMS voltage corner to be evaluated
121	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
122	USER_LPRIMARY	TYP		531.2	uH	Primary inductance corner to be evaluated
123	MODE_OPERATION			CCM		Mode of operation
124	KP			0.752		Measure of continuous/discontinuous mode of operation
125	FSWITCHING			66536	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
126	VMIN			90.14	V	Valley of the minimum input AC voltage at full load
127	DUTYCYCLE			0.601		Steady state duty cycle
128	TIME_ON			9.03	us	Primary switch on-time
129	TIME_OFF			6.00	us	Primary switch off-time
130	IPEAK_PRIMARY			2.028	A	Primary switch peak current
131	IPEDESTAL_PRIMARY			0.504	A	Primary switch current pedestal
132	IAVERAGE_PRIMARY			0.761	A	Primary switch average current
133	IRIPPLE_PRIMARY			1.524	A	Primary switch ripple current
134	IRMS_PRIMARY			1.039	A	Primary switch RMS current
135	BPEAK			3340	Gauss	Peak flux density
136	BMAX			3107	Gauss	Maximum flux density
137	BAC			1168	Gauss	AC flux density (0.5 x Peak to Peak)

9 PCB Assembly Instructions

9.1 *Materials*

Item	Description
[1]	Capacitor C8 on DER-713 Schematic.
[2]	Polyester Tape: 20 mm X 40 mm.
[3]	Polyester Tape: 5 mm X 20 mm.

9.2 *Output Capacitor Assembly Instructions*



Wrap C8 with tape Item [2] to insulate the capacitor from the transformer core.

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Fold the tape on top of the capacitor and secure using Item [3].

Please take note on the polarity of the electrolytic capacitor C8 during insertion to the PCB.

Finish assembly.

Note: Cut all the TH pins to <0.5 mm on the bottom side of the board after completing the assembly.

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10 Performance Data

10.1 *Efficiency*

10.1.1 Average Efficiency

10.1.1.1 90 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	90	1302.10	68.72	19.43	3249.60	63.14	91.88
75%	90	1013.50	51.14	19.51	2436.90	47.54	92.86
50%	90	728.80	34.23	19.64	1625.00	31.92	93.25
25%	90	422.00	17.17	19.70	812.50	16.01	93.25
						Average	**92.81**

10.1.1.2 115 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} $m(A_{DC})$	P_{OUT} (W)	Efficiency at PCB (%)
100%	115	1210.40	68.43	19.50	3249.50	63.37	92.61
75%	115	969.80	51.25	19.58	2436.80	47.72	93.11
50%	115	708.70	34.24	19.66	1624.90	31.95	93.31
25%	115	326.60	17.18	19.72	812.50	16.02	93.25
						Average	**93.02**

10.1.1.3 230 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	230	555.60	67.35	19.58	3249.50	63.64	94.49
75%	230	442.40	50.67	19.64	2436.90	47.85	94.43
50%	230	322.90	33.94	19.68	1625.00	31.97	94.20
25%	230	191.02	17.16	19.71	812.50	16.02	93.33
						Average	**94.11**

10.1.1.4 265 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	265	509.60	67.41	19.59	3249.50	63.64	94.41
75%	265	408.10	50.73	19.63	2436.80	47.84	94.30
50%	265	300.10	34.00	19.68	1624.90	31.97	94.03
25%	265	179.30	17.21	19.71	812.50	16.01	93.03
						Average	**93.94**

10.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 5 minutes for each line.

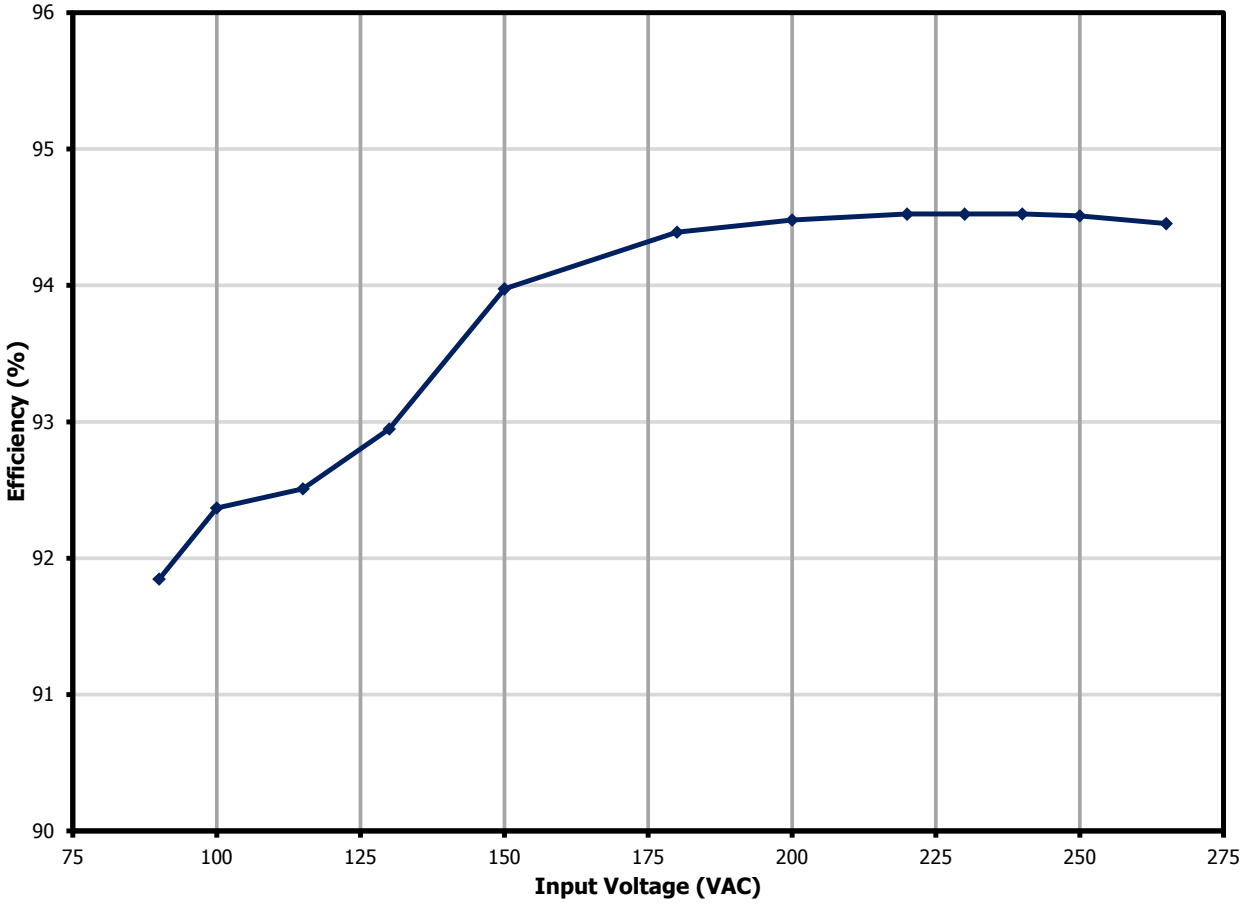

Figure 8 – Full Load Efficiency vs. Line.

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10.1.3 Efficiency vs. Load

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

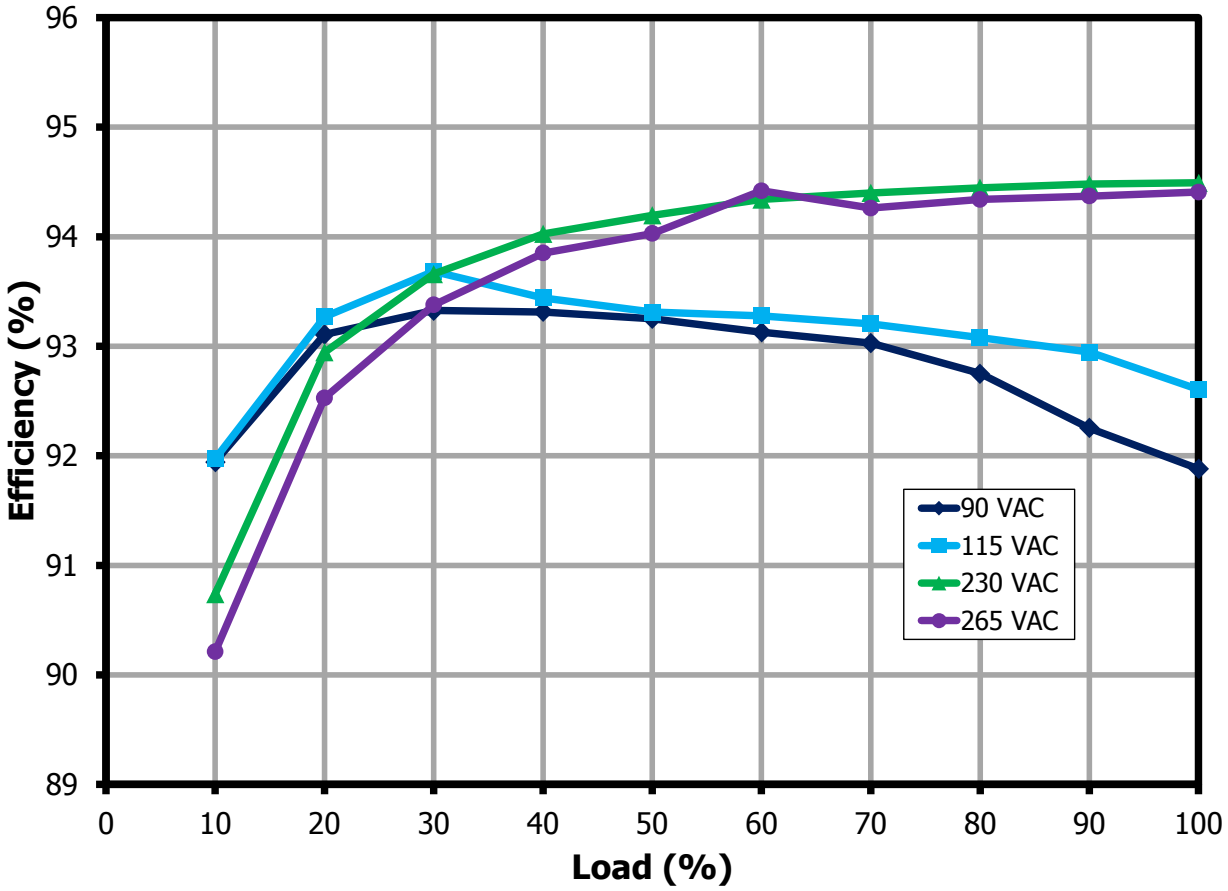

Figure 9 – Efficiency vs. Percentage Load.

10.2 *Available Standby Output Power*

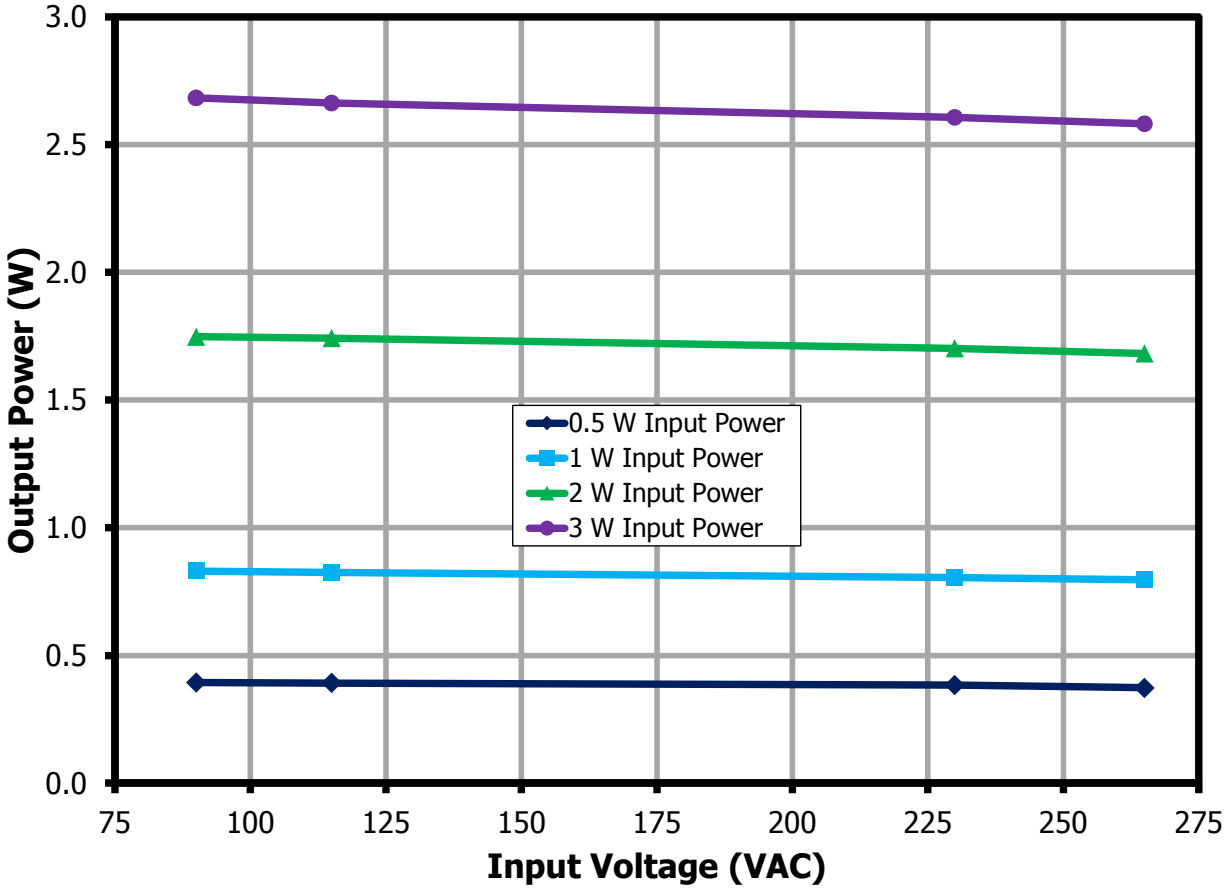

Figure 10 – Available Standby Output Power for 0.5 W, 1 W, 2 W and 3 W Input Power.

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10.3 ***No-Load Input Power***

Test Condition: Soak for 5 minutes each line and 2-minute integration time.

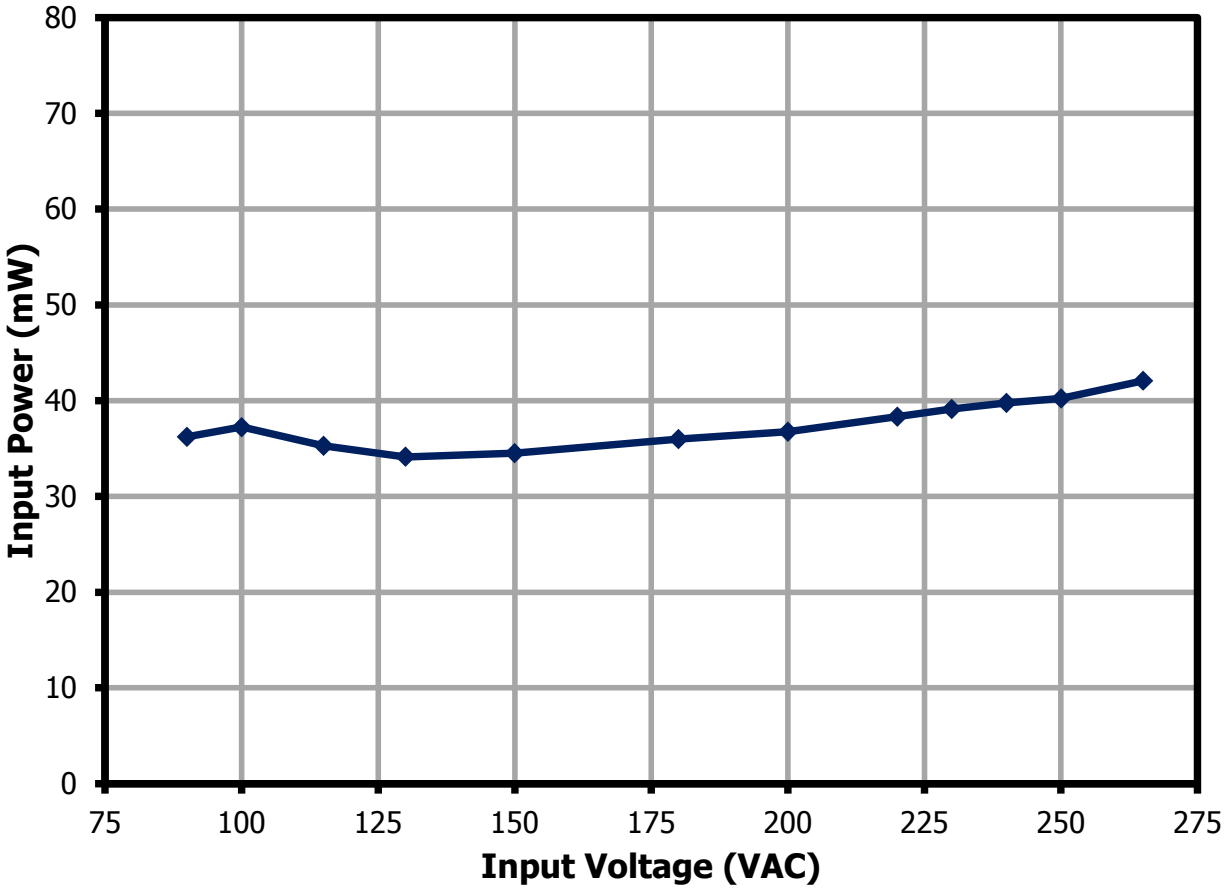

Figure 11 – No-Load Input Power vs. Line at Room Temperature.

10.4 *Line Regulation*

Test Condition: Soak for 5 minutes for each line.

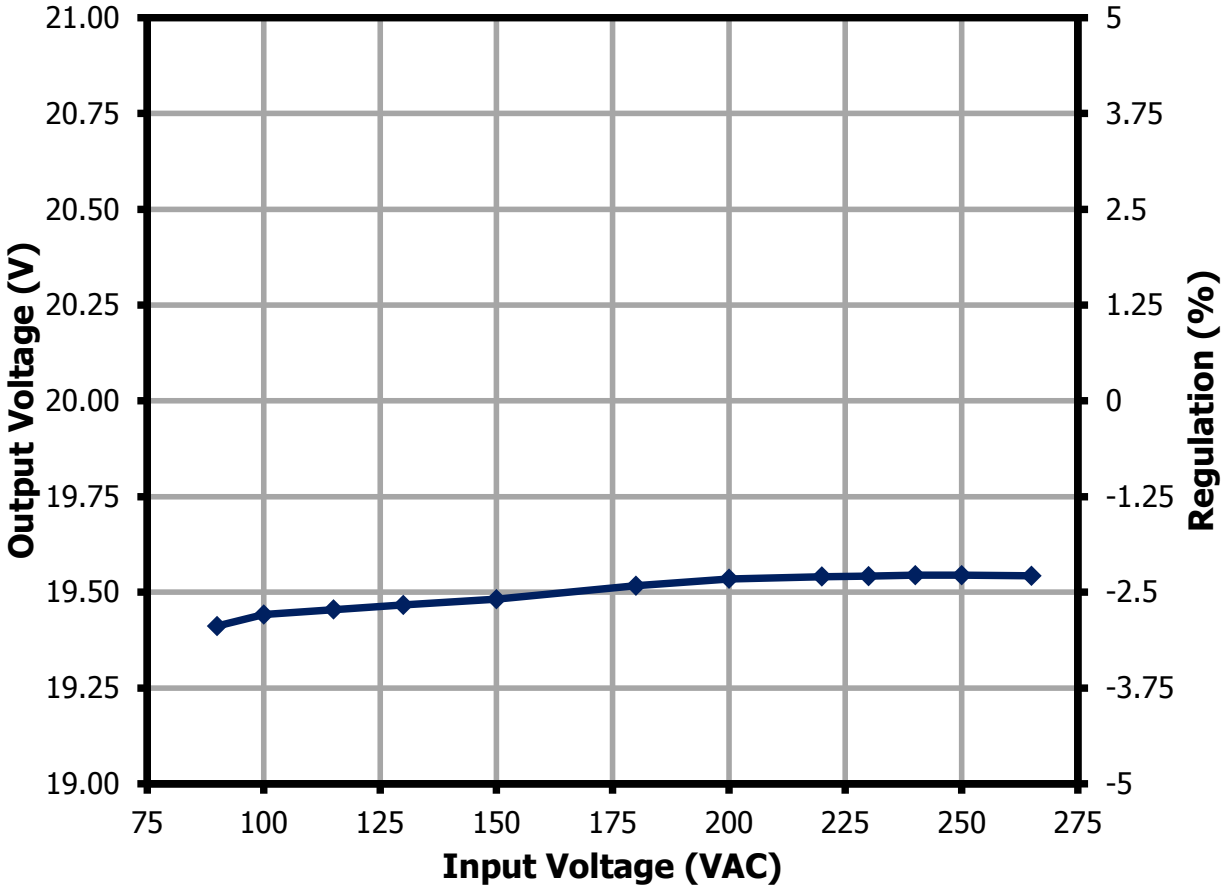

Figure 12 – Output Voltage vs. Line Voltage.

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10.5 ***Load Regulation***

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

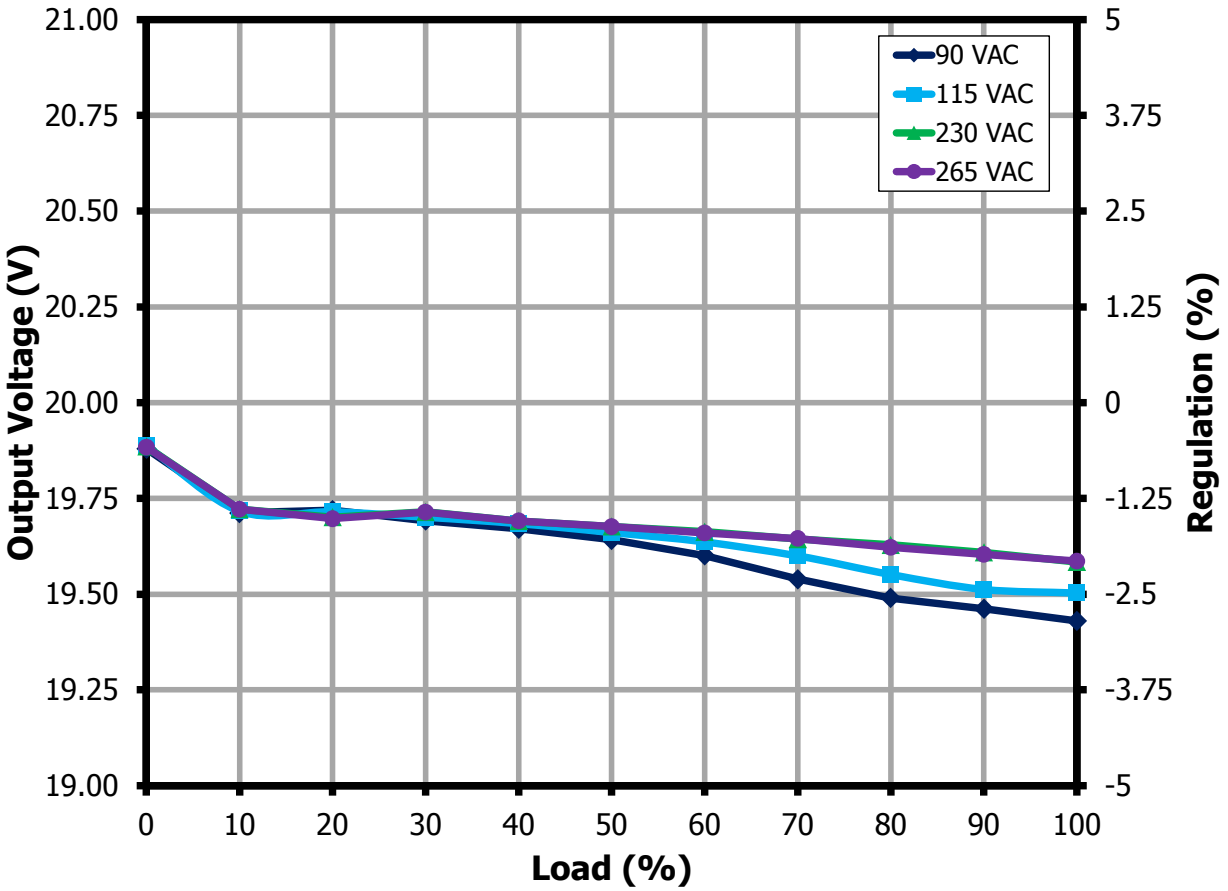

Figure 13 – Output Voltage vs. Percent Load.

11 Waveforms

11.1 *Load Transient Response*

Test Condition: Frequency = 500 Hz, Duty cycle = 50 %, Slew Rate = 800 mA / µs

11.1.1 0% - 100% Load Change

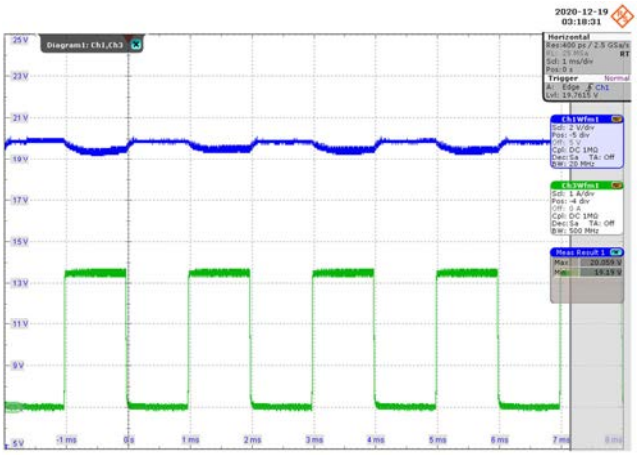

Figure 14 – 90 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.19 V.

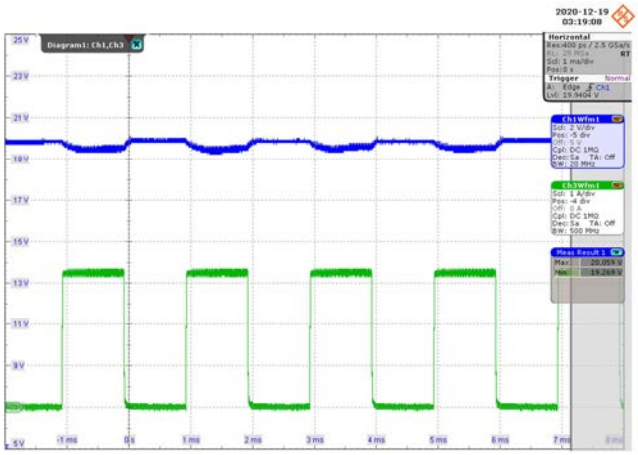

Figure 15 – 115 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.27 V.

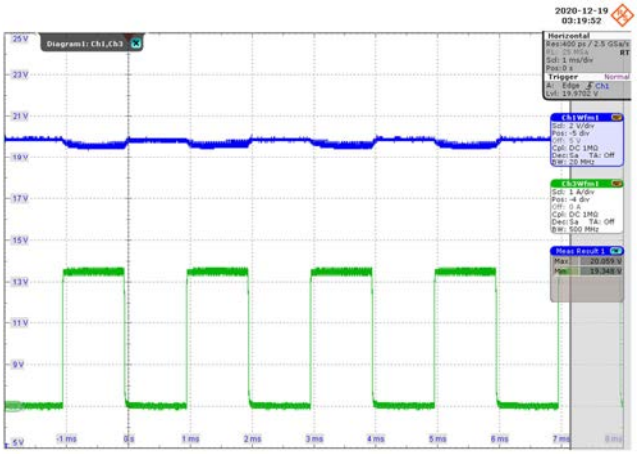

Figure 16 – 230 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.35 V.

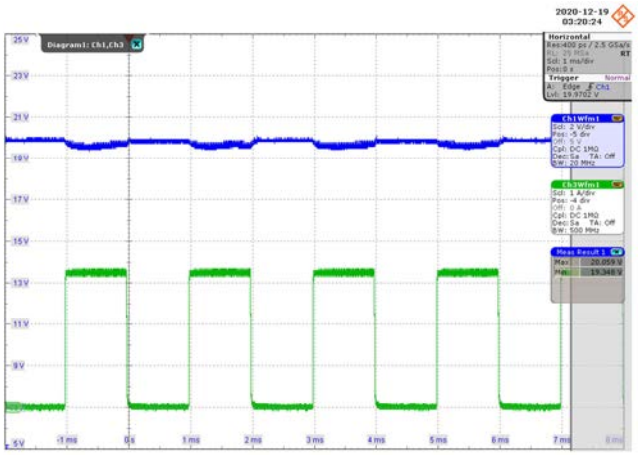

Figure 17 – 265 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 20.06 V, V_{MIN}: 19.35 V.

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11.1.2 50% - 100% Load Change

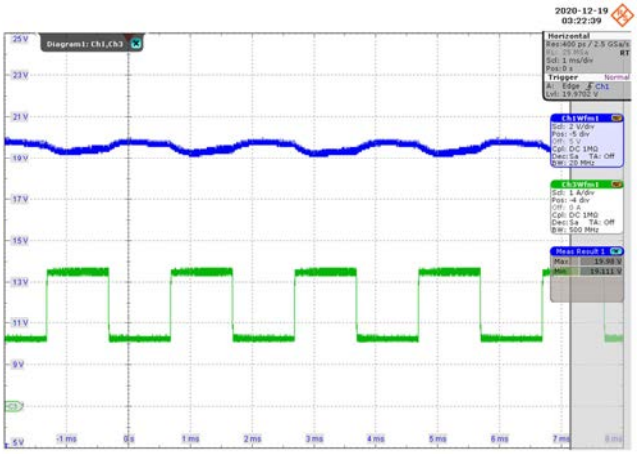

Figure 18 – 90 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.11 V.

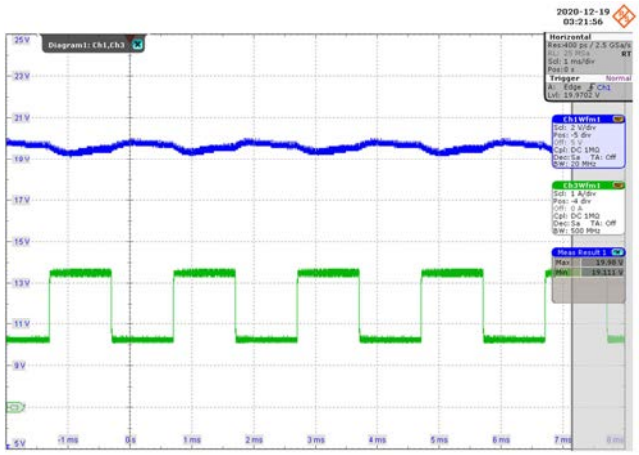

Figure 19 – 115 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.11 V.

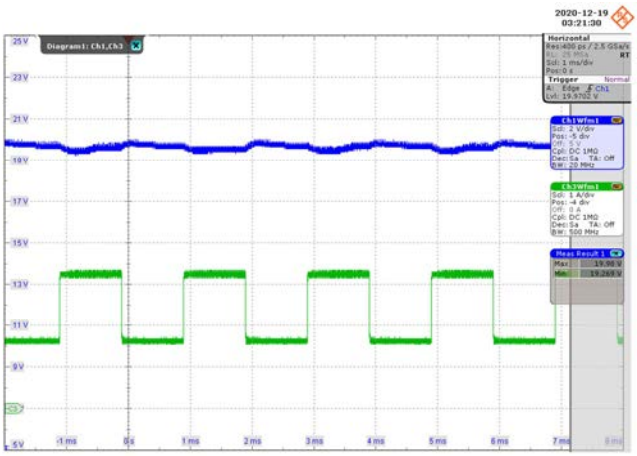

Figure 20 – 230 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.27 V.

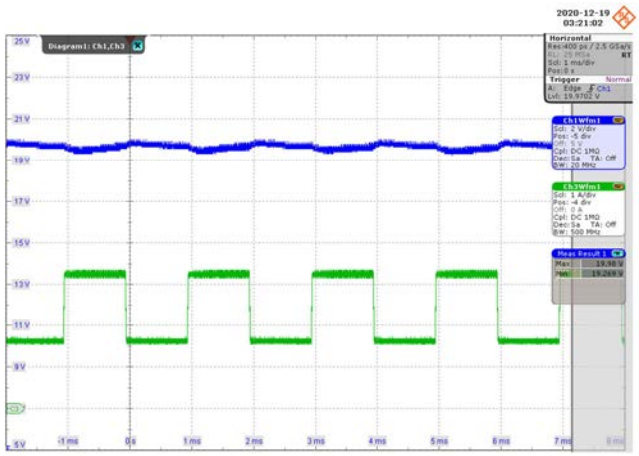

Figure 21 – 265 VAC 60 Hz.
CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 19.98 V, V_{MIN}: 19.27 V.

11.2 *Output Voltage at Start-up*

11.2.1 CC Mode

11.2.1.1 100% Load

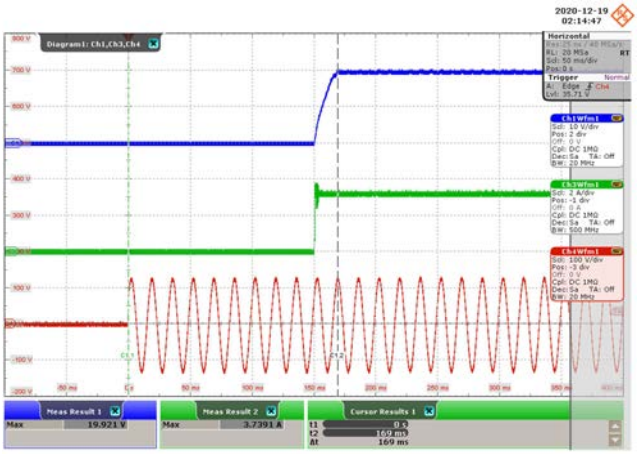

Figure 22 – 90 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 169 ms.

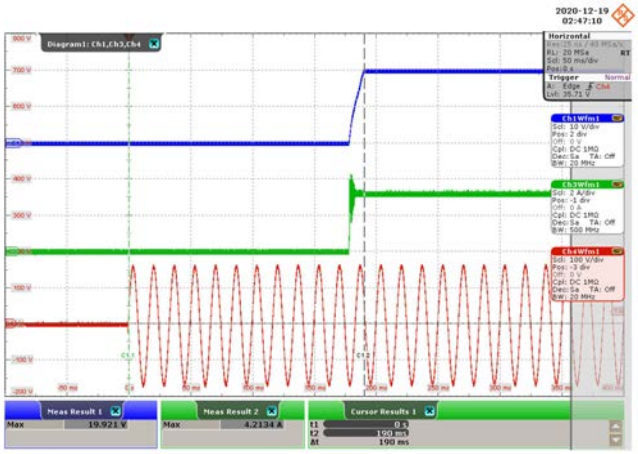

Figure 23 – 115 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 190 ms.

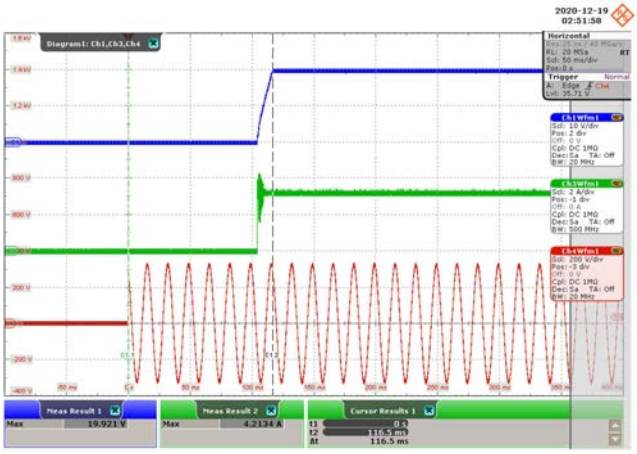

Figure 24 – 230 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 116.5 ms.

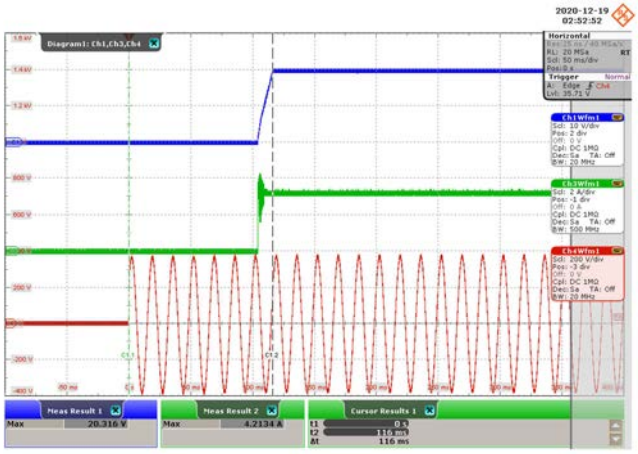

Figure 25 – 265 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 116 ms.

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11.2.1.2 0% Load

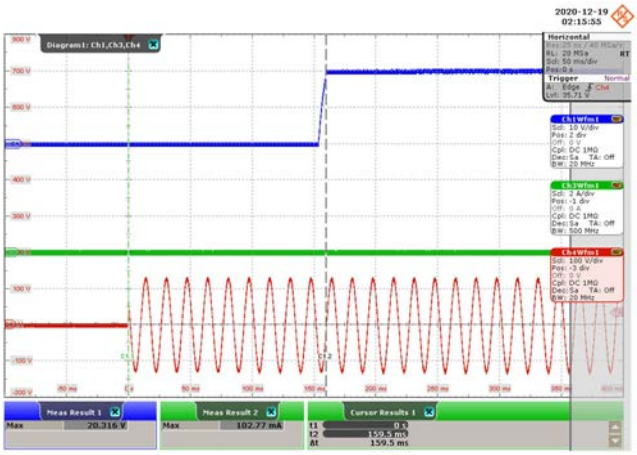

Figure 26 – 90 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 159.5 ms.

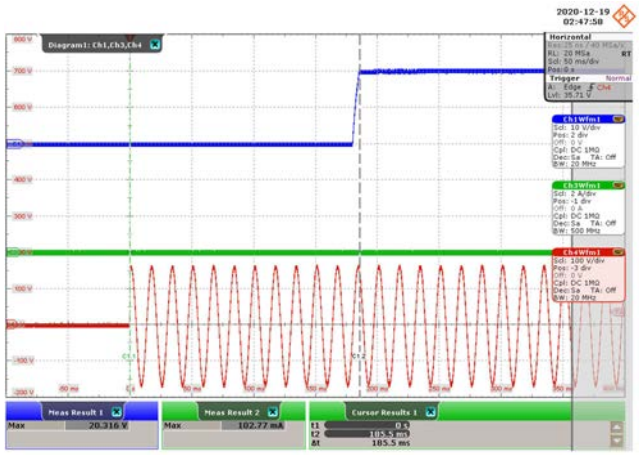

Figure 27 – 115 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 185.5 ms.

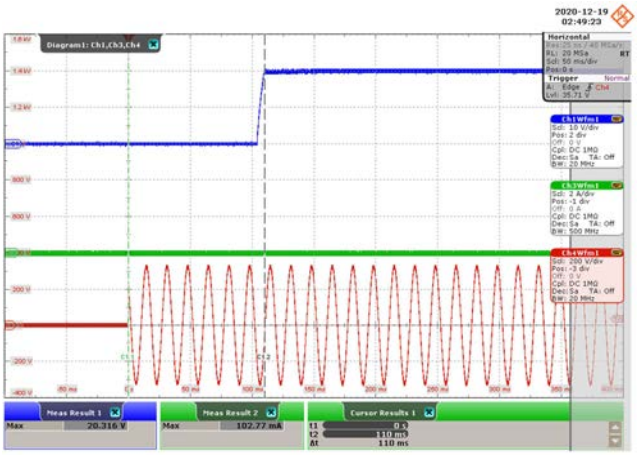

Figure 28 – 230 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 110 ms.

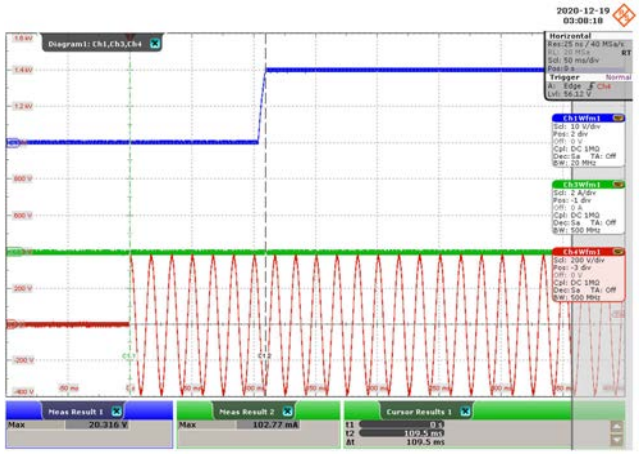

Figure 29 – 265 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 109.5 ms.

11.2.2 CR Mode

11.2.2.1 100% Load

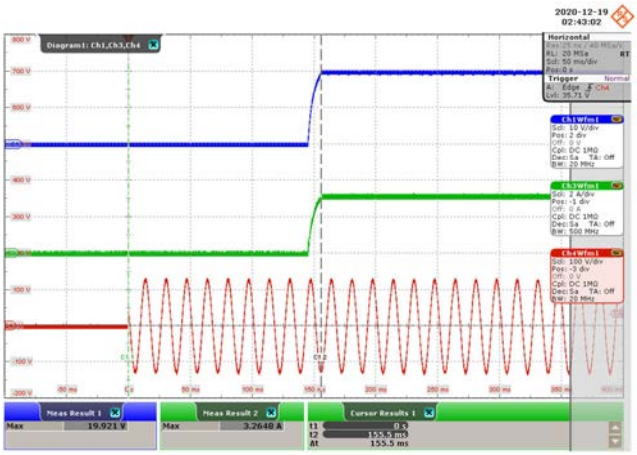

Figure 30 – 90 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 155.5 ms.

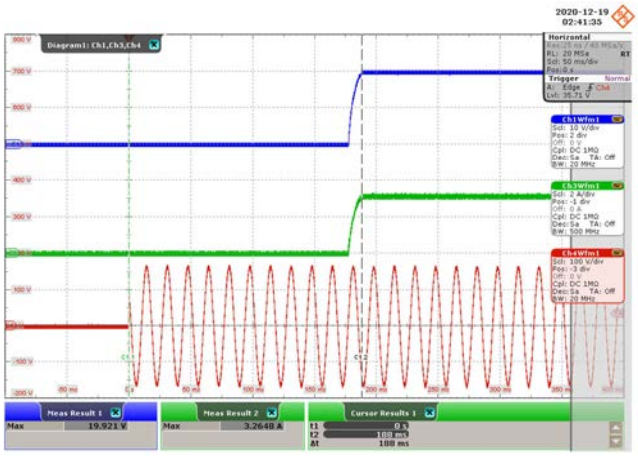

Figure 31 – 115 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 100 V / div., 50 ms / div.
On-Time Delay = 188 ms.

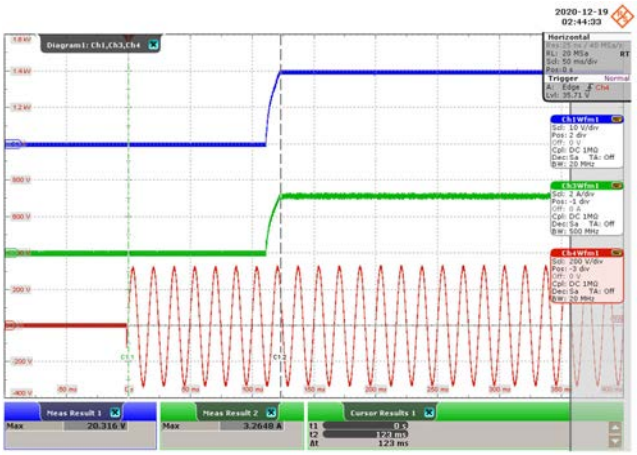

Figure 32 – 230 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 123 ms.

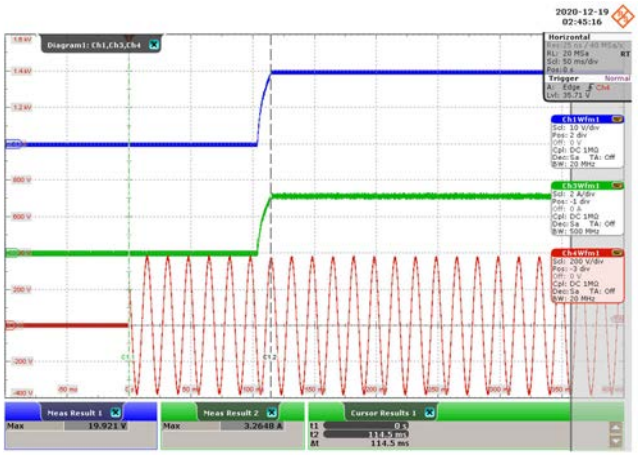

Figure 33 – 265 VAC 60 Hz.
CH1: V_{OUT}, 10 V / div., 50 ms / div.
CH3: I_{OUT}, 2 A / div., 50 ms / div.
CH4: V_{IN}, 200 V / div., 50 ms / div.
On-Time Delay = 114.5 ms.

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11.1 *MinE-CAP Waveforms*

11.1.1 Normal Operation at 100% Load

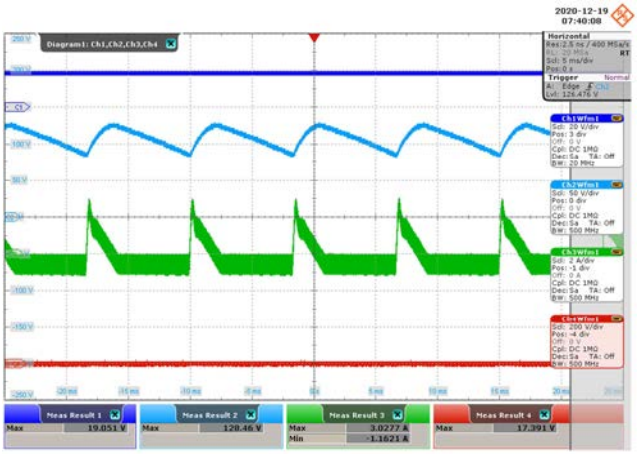

Figure 34 – 90 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
V_{LV_CAP} = 128.46 $V_{MAX.}$

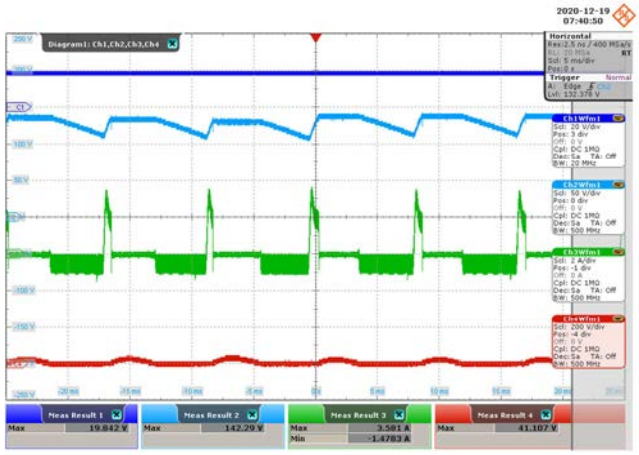

Figure 35 – 115 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
V_{LV_CAP} = 142.29 $V_{MAX.}$

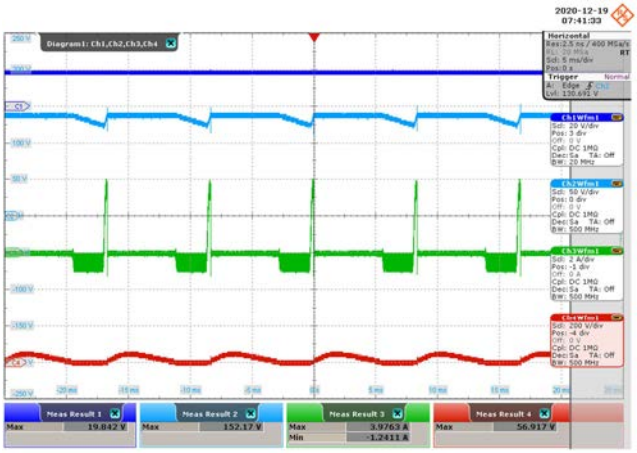

Figure 36 – 132 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
V_{LV_CAP} = 152.17 $V_{MAX.}$

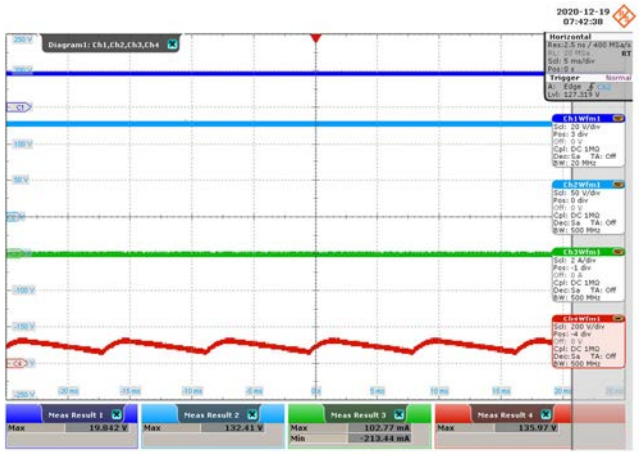

Figure 37 – 180 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
V_{LV_CAP} = 132.41 $V_{MAX.}$

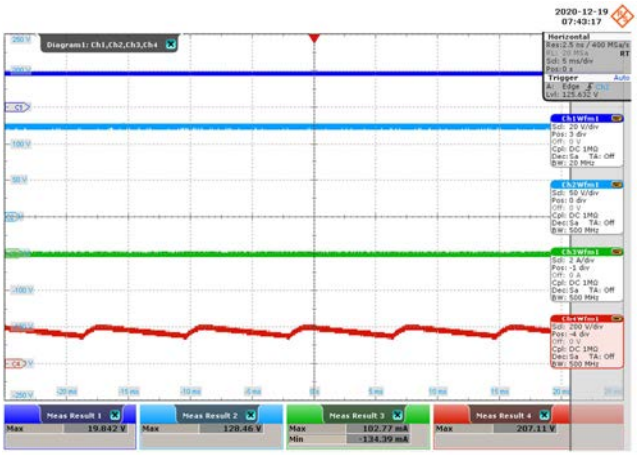

Figure 38 – 230 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{LV\ CAP}$ = 128.46 $V_{MAX.}$

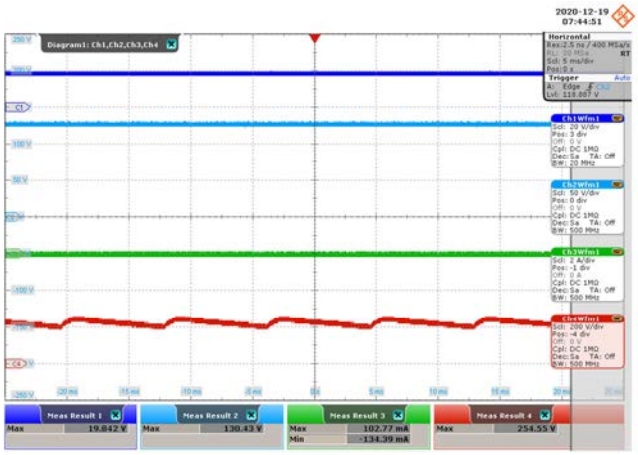

Figure 39 – 265 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 5 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 5 ms / div.
CH3: I_{DS}, 2 A / div., 5 ms / div.
CH4: V_{DS}, 200 V / div., 5 ms / div.
$V_{LV\ CAP}$ = 130.43 $V_{MAX.}$

11.1.1 Start-up at 100% Load

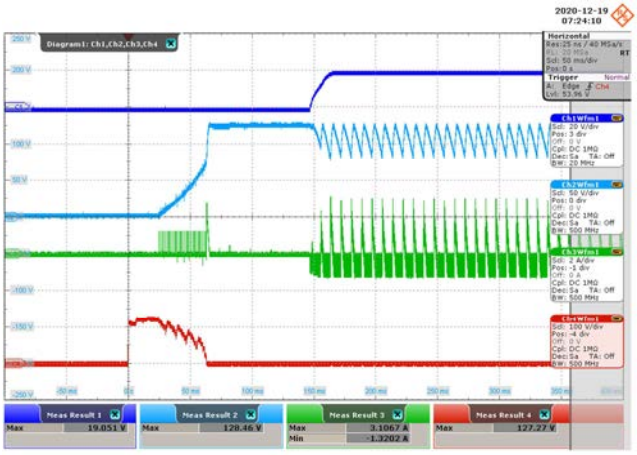

Figure 40 – 90 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 50 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 50 ms / div.
CH3: I_{DS}, 2 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
V_{LV_CAP} = 128.46 $V_{MAX.}$

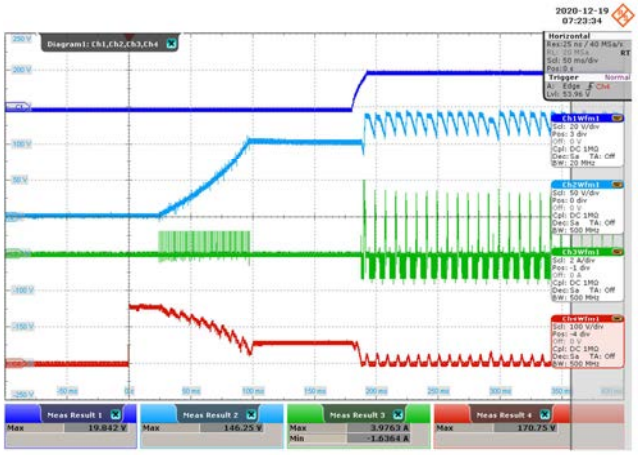

Figure 41 – 115 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 50 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 50 ms / div.
CH3: I_{DS}, 2 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
V_{LV_CAP} = 146.25 $V_{MAX.}$

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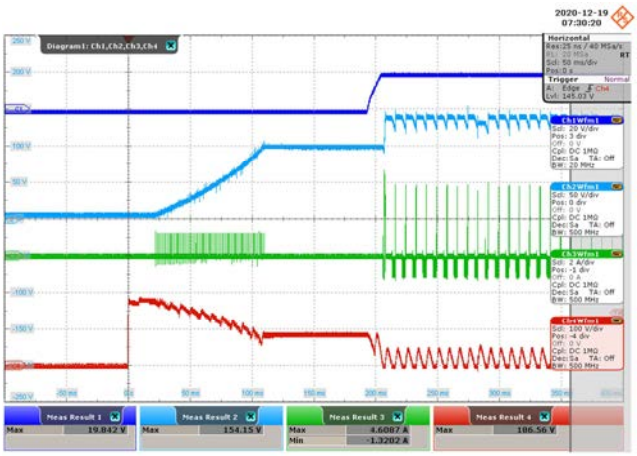

Figure 42 – 132 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 50 ms / div.
CH2: V_{LV_CAP}, 50 V / div., 50 ms / div.
CH3: I_{DS}, 2 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
V_{LV_CAP} = 154.15 $V_{MAX.}$

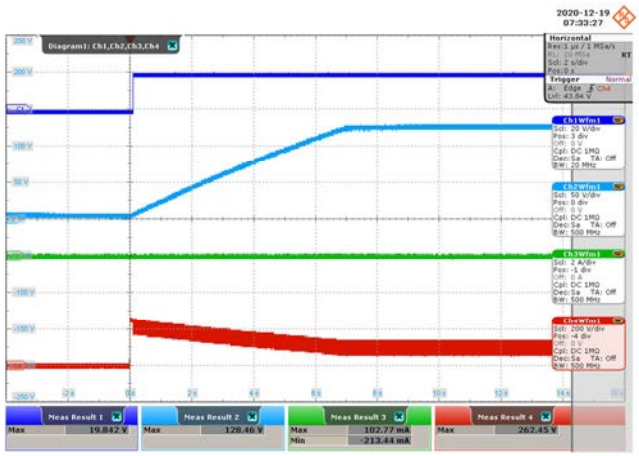

Figure 43 – 180 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 2 s / div.
CH2: V_{LV_CAP}, 50 V / div., 2 s / div.
CH3: I_{DS}, 2 A / div., 2 s / div.
CH4: V_{DS}, 200 V / div., 2 s / div.
V_{LV_CAP} = 128.46 $V_{MAX.}$

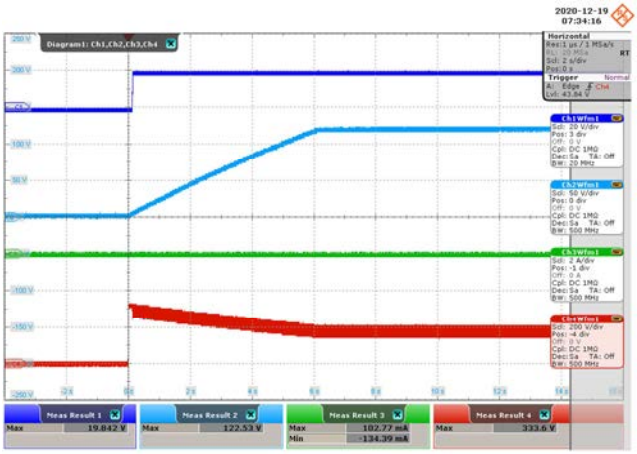

Figure 44 – 230 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 2 s / div.
CH2: V_{LV_CAP}, 50 V / div., 2 s / div.
CH3: I_{DS}, 2 A / div., 2 s / div.
CH4: V_{DS}, 200 V / div., 2 s / div.
V_{LV_CAP} = 122.53 $V_{MAX.}$

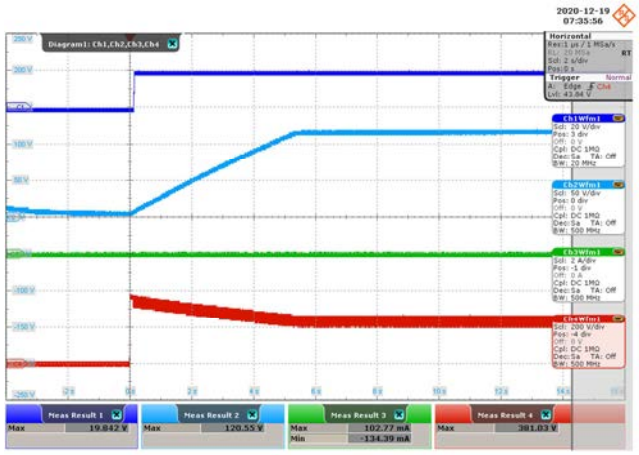

Figure 45 – 265 VAC 60 Hz.
CH1: V_{OUT}, 20 V / div., 2 s / div.
CH2: V_{LV_CAP}, 50 V / div., 2 s / div.
CH3: I_{DS}, 2 A / div., 2 s / div.
CH4: V_{DS}, 200 V / div., 2 s / div.
V_{LV_CAP} = 120.55 $V_{MAX.}$

11.2 *Switching Waveforms*

11.2.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

11.2.1.1 100% Load

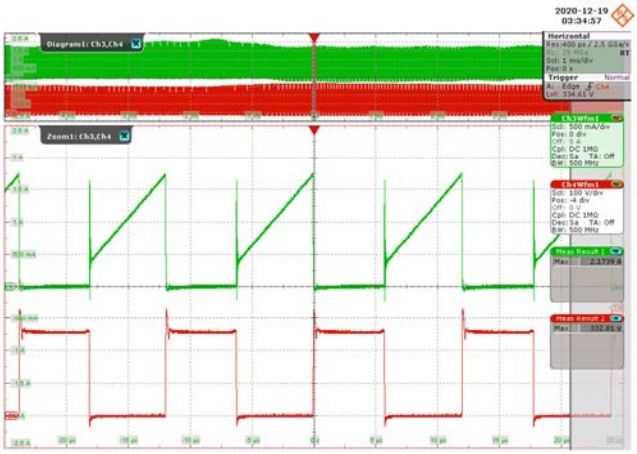

Figure 46 – 90 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 332.81 V, $I_{DS(MAX)}$ = 2.17 A.

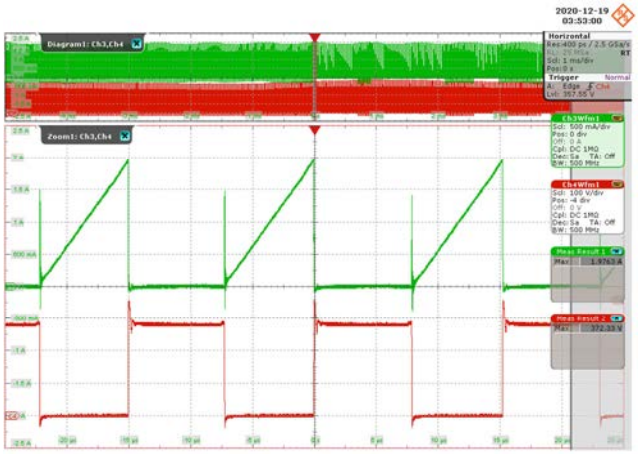

Figure 47 – 115 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 372.33 V, $I_{DS(MAX)}$ = 1.98 A.

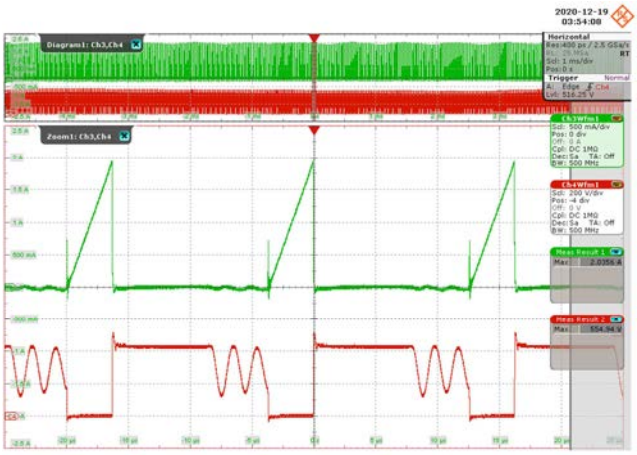

Figure 48 – 230 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 554.94 V, $I_{DS(MAX)}$ = 2.04 A.

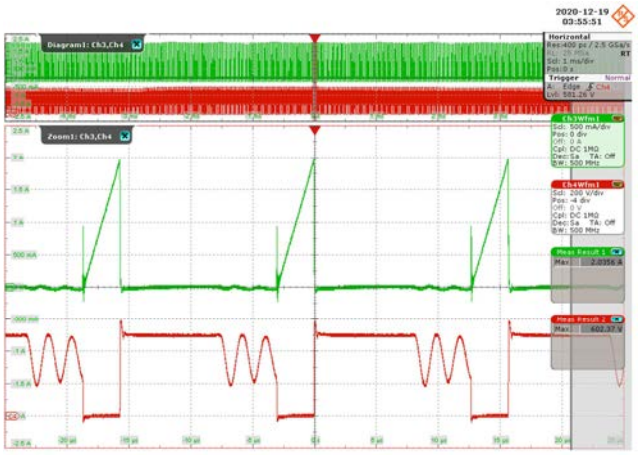

Figure 49 – 265 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 602.37 V, $I_{DS(MAX)}$ = 2.04 A.

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11.2.1.2 0% Load

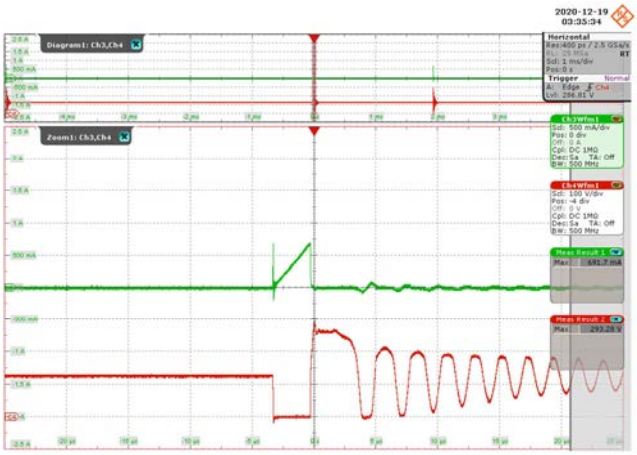

Figure 50 – 90 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 293.28 V, $I_{DS(MAX)}$ = 0.69 A.

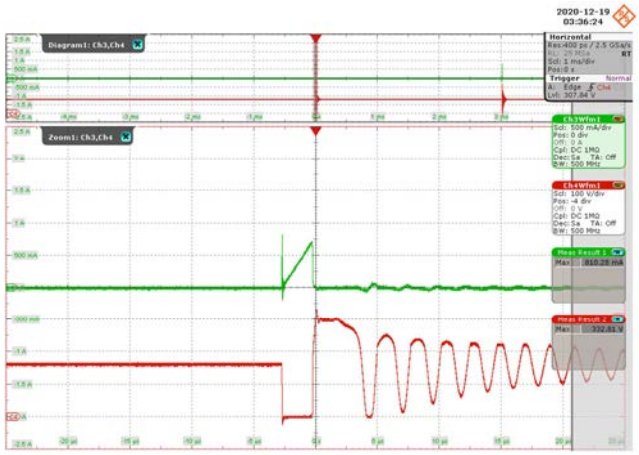

Figure 51 – 115 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 100 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 332.81 V, $I_{DS(MAX)}$ = 0.81 A.

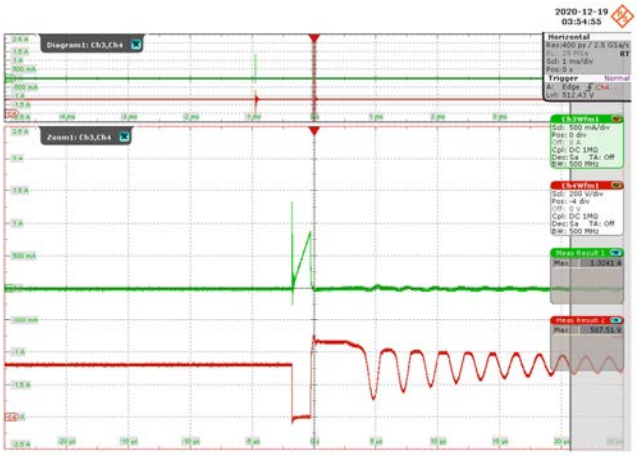

Figure 52 – 230 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 507.51 V, $I_{DS(MAX)}$ = 1.32 A.

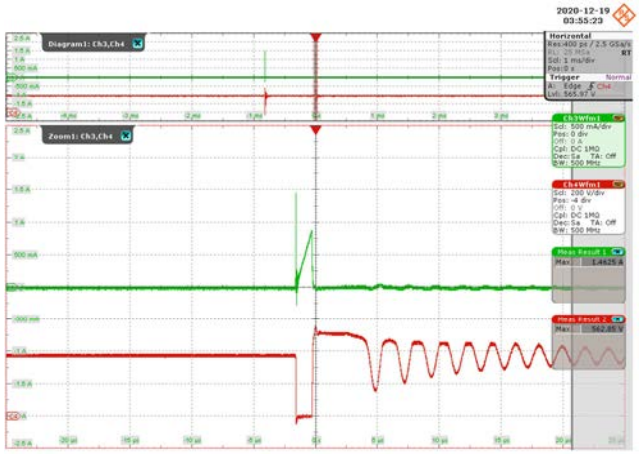

Figure 53 – 265 VAC 60 Hz.
CH3: I_{DS}, 500 mA / div., 1 ms / div.
CH4: V_{DS}, 200 V / div., 1 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 562.85 V, $I_{DS(MAX)}$ = 1.46 A.

11.2.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

11.2.2.1 100% Load

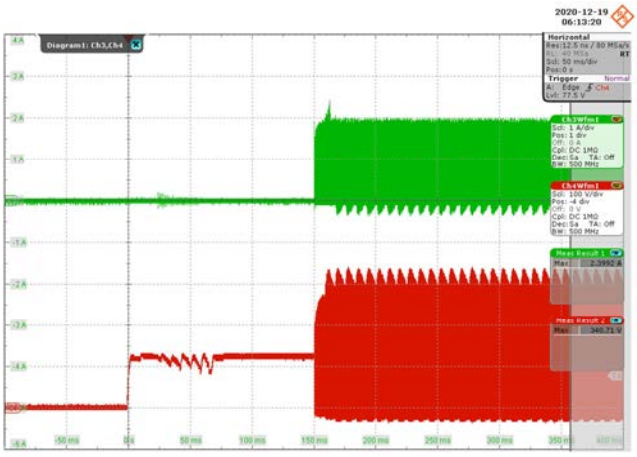

Figure 54 – 90 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 340.71 V, $I_{DS(MAX)}$ = 2.40 A.

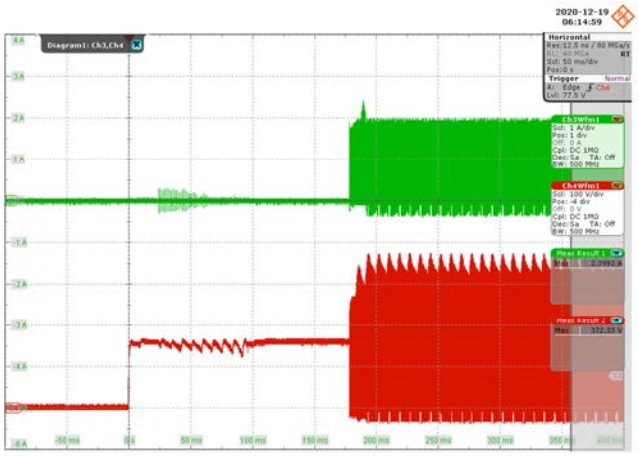

Figure 55 – 115 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 372.33 V, $I_{DS(MAX)}$ = 2.40 A.

Figure 56 – 230 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 200 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 547.04 V, $I_{DS(MAX)}$ = 2.52 A.

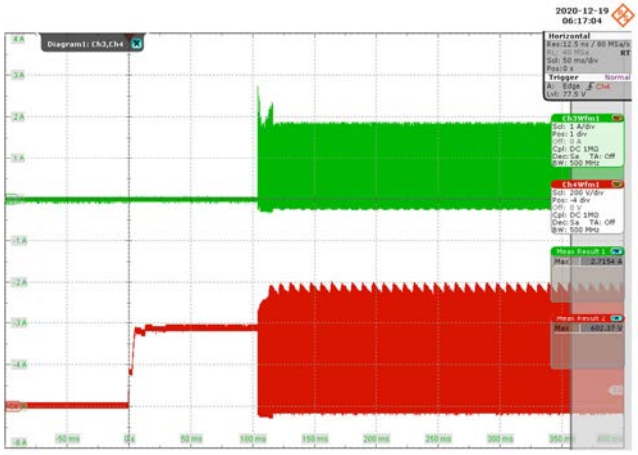

Figure 57 – 265 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 200 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 602.37 V, $I_{DS(MAX)}$ = 2.72 A.

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11.2.2.2 0% Load

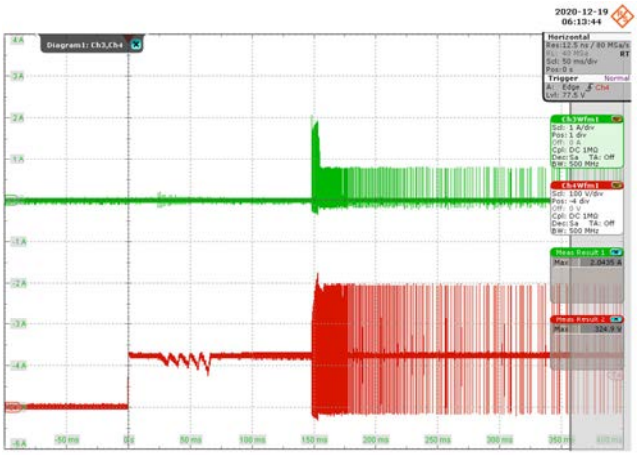

Figure 58 – 90 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 324.90 V, $I_{DS(MAX)}$ = 2.04 A.

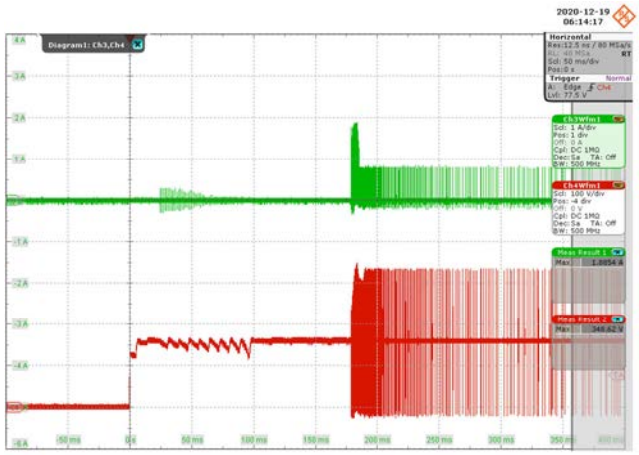

Figure 59 – 115 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 100 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 348.62 V, $I_{DS(MAX)}$ = 1.89 A.

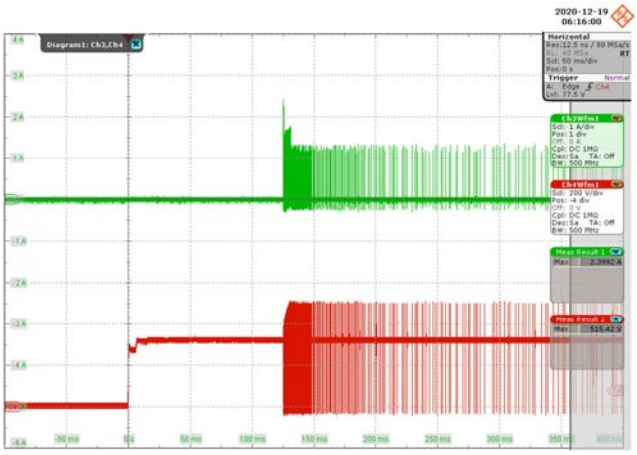

Figure 60 – 230 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 200 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 515.42 V, $I_{DS(MAX)}$ = 2.40 A.

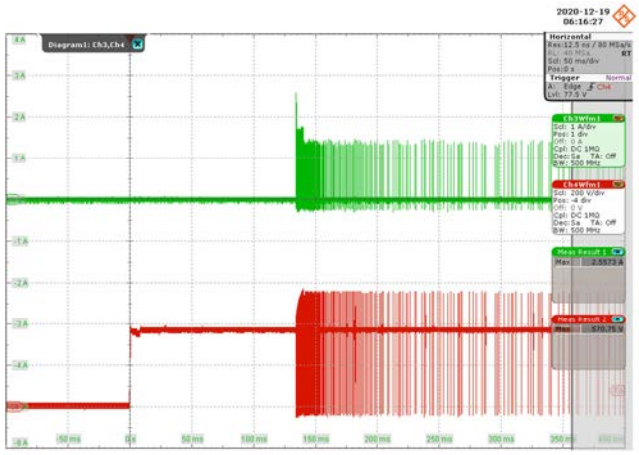

Figure 61 – 265 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 50 ms / div.
CH4: V_{DS}, 200 V / div., 50 ms / div.
$V_{DS(MAX)}$ = 570.75 V, $I_{DS(MAX)}$ = 2.56 A.

11.2.3 SR FET Voltage and Current at Normal Operation

11.2.3.1 100% Load

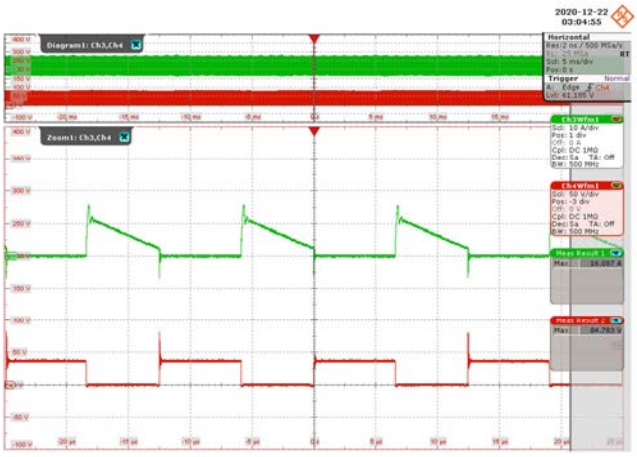

Figure 62 – 90 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 84.78 V, $I_{DS(MAX)}$ = 16.09 A.

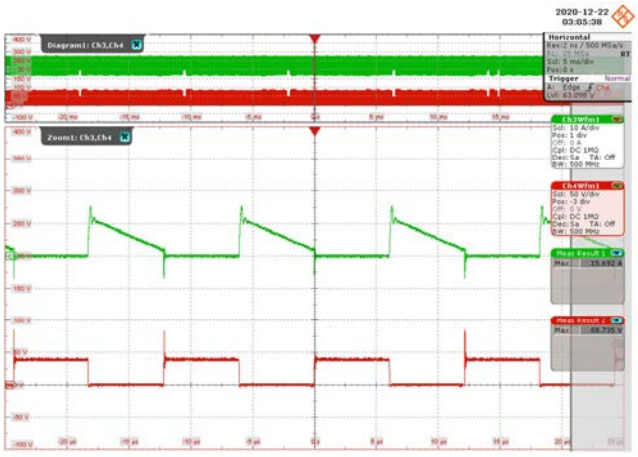

Figure 63 – 115 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 88.74 V, $I_{DS(MAX)}$ = 15.69 A.

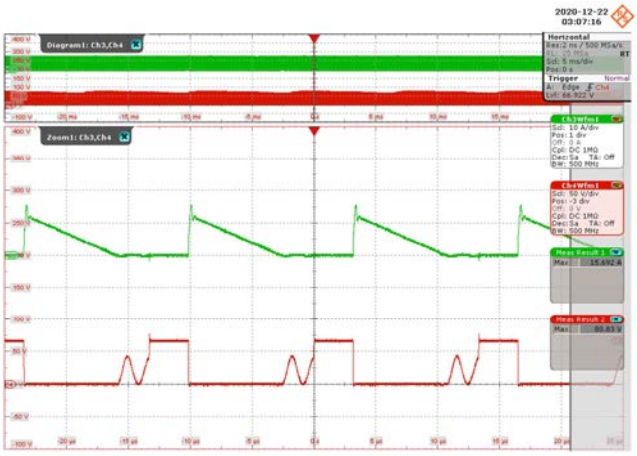

Figure 64 – 230 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 80.83 V, $I_{DS(MAX)}$ = 15.69 A.

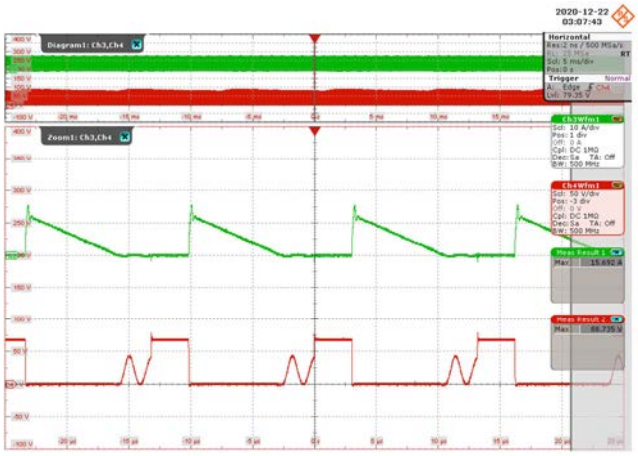

Figure 65 – 265 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 88.74 V, $I_{DS(MAX)}$ = 15.69 A.

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11.2.3.2 0% Load

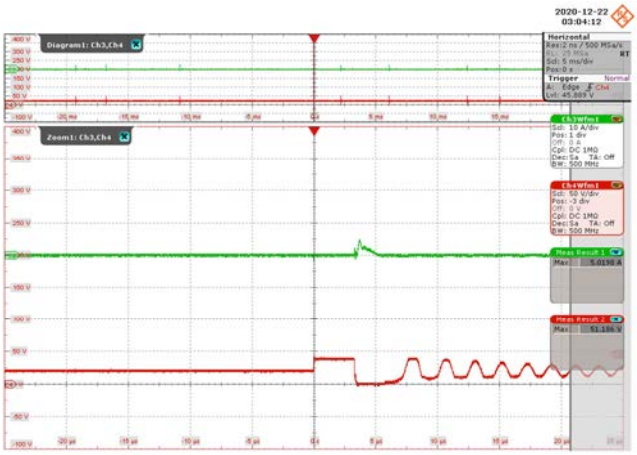

Figure 66 – 90 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 51.19 V, $I_{DS(MAX)}$ = 5.02 A.

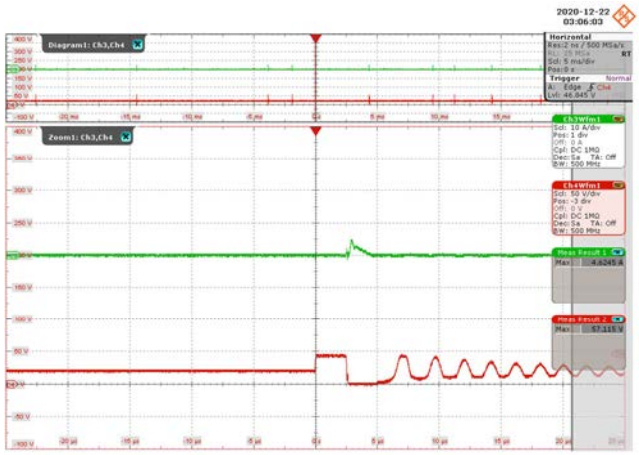

Figure 67 – 115 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 57.12 V, $I_{DS(MAX)}$ = 4.62 A.

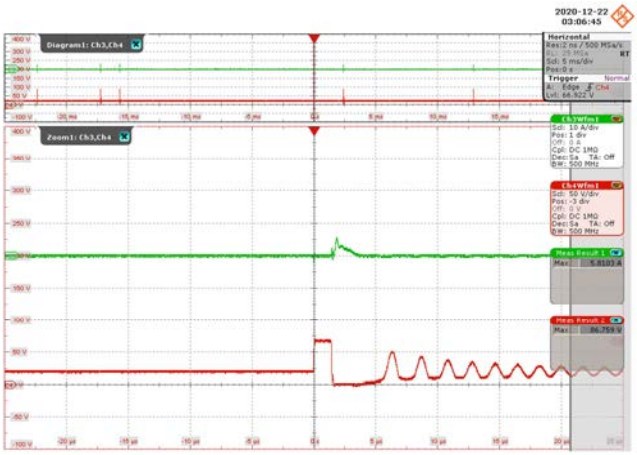

Figure 68 – 230 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 86.76 V, $I_{DS(MAX)}$ = 5.81 A.

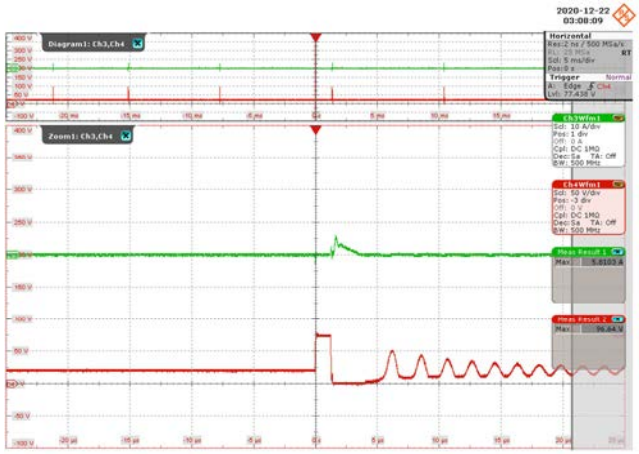

Figure 69 – 265 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 96.64 V, $I_{DS(MAX)}$ = 5.81 A.

11.2.4 SR FET Voltage and Current at Start-up Operation

11.2.4.1 100% Load

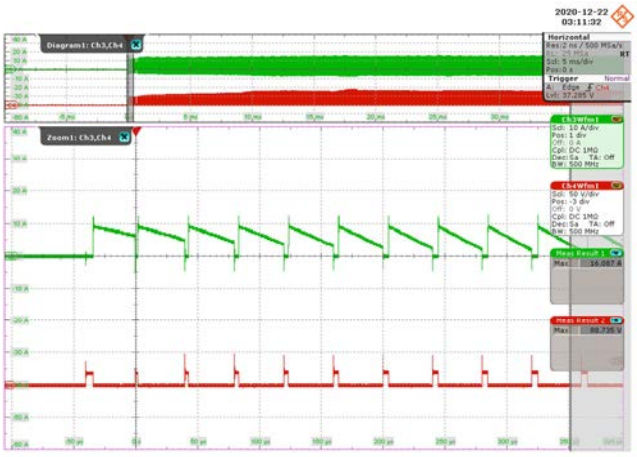

Figure 70 – 90 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 88.74 V, $I_{DS(MAX)}$ = 16.09 A.

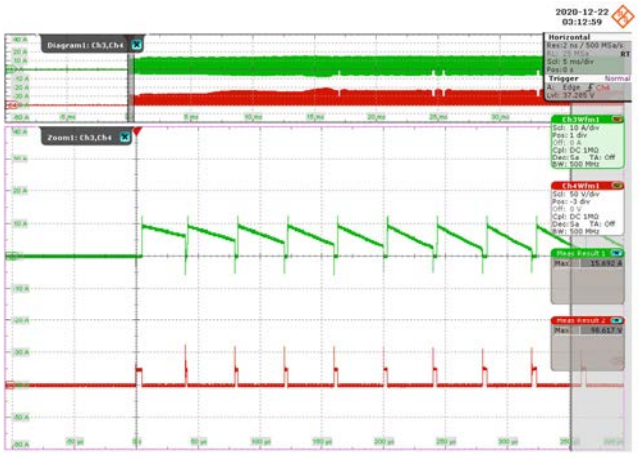

Figure 71 – 115 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 98.62 V, $I_{DS(MAX)}$ = 15.69 A.

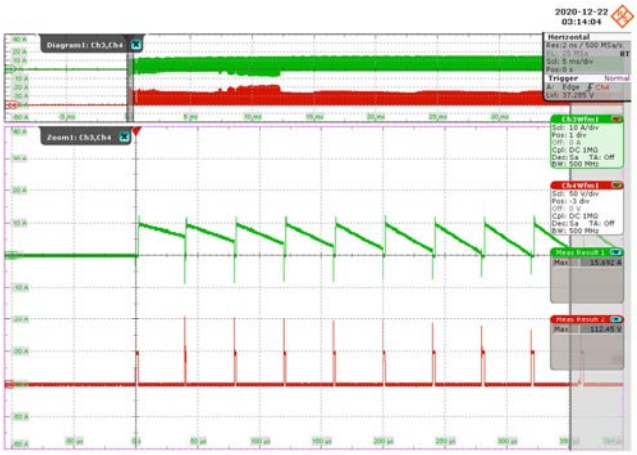

Figure 72 – 230 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 112.45 V, $I_{DS(MAX)}$ = 15.69 A.

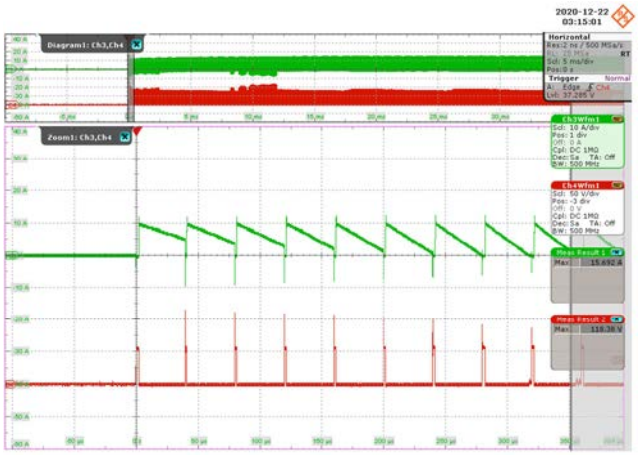

Figure 73 – 265 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 118.38 V, $I_{DS(MAX)}$ = 15.69 A.

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11.2.4.2 0% Load

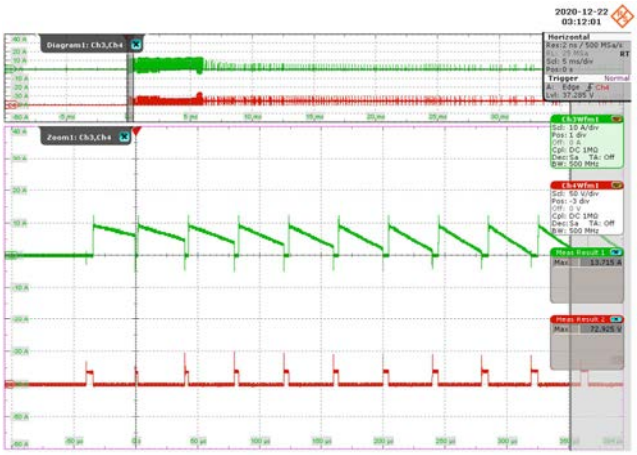

Figure 74 – 90 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 72.93 V, $I_{DS(MAX)}$ = 13.72 A.

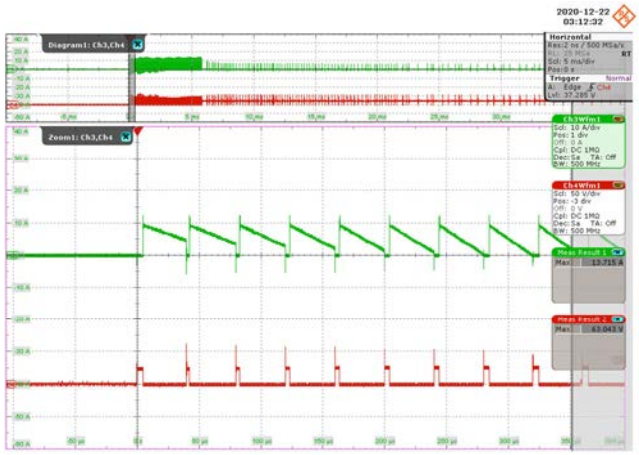

Figure 75 – 115 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 63.04 V, $I_{DS(MAX)}$ = 13.72 A.

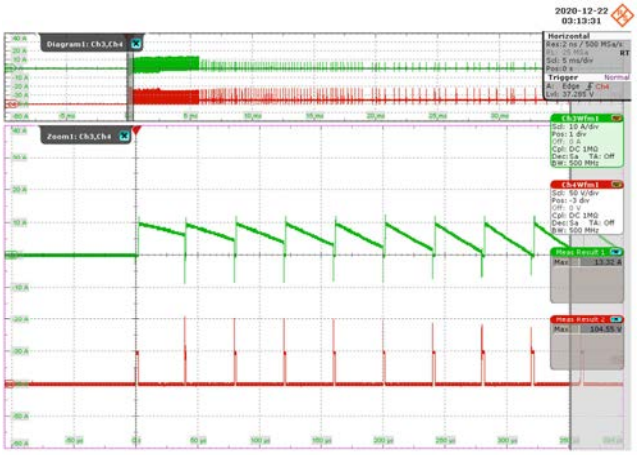

Figure 76 – 230 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 104.55 V, $I_{DS(MAX)}$ = 13.32 A.

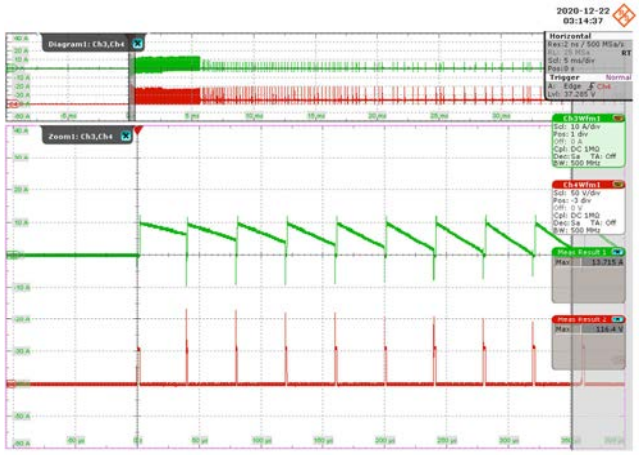

Figure 77 – 265 VAC 60 Hz.
CH3: I_{DS}, 10 A / div., 5 ms / div.
CH4: V_{DS}, 50 V / div., 5 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$ = 116.40 V, $I_{DS(MAX)}$ = 13.72 A.

11.3 *Fault Condition*

11.3.1 Output Short-Circuit

Test Condition: Short circuit applied at the end of PCB during start-up

Figure 78 – 90 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 500 ms / div.
CH4: V_{DS}, 100 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 218.18 V, $I_{DS(MAX)}$ = 2.37 A.

Figure 79 – 115 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 500 ms / div.
CH4: V_{DS}, 100 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 269.57 V, $I_{DS(MAX)}$ = 2.92 A.

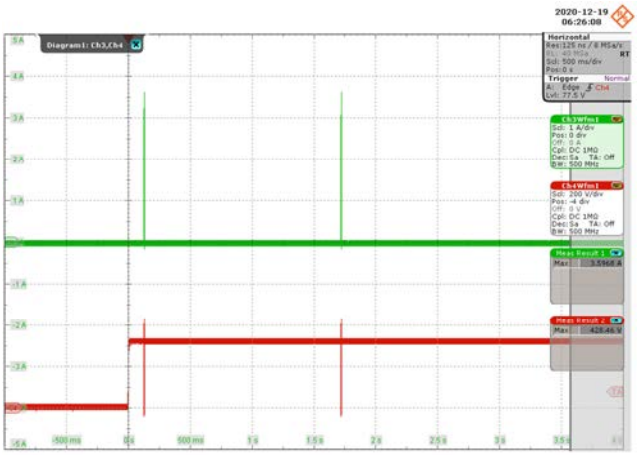

Figure 80 – 230 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 500 ms / div.
CH4: V_{DS}, 100 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 428.46 V, $I_{DS(MAX)}$ = 3.60 A.

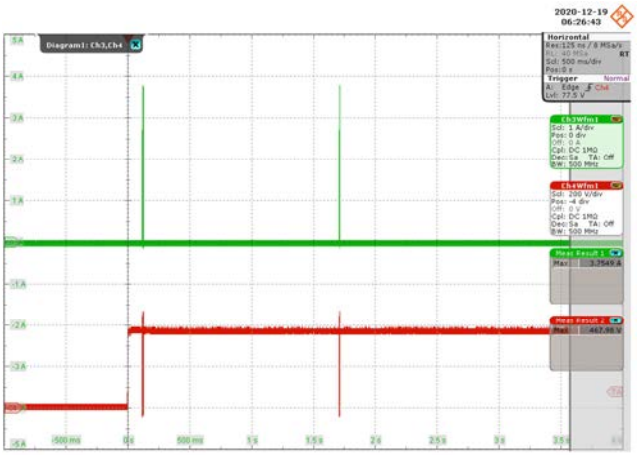

Figure 81 – 265 VAC 60 Hz.
CH3: I_{DS}, 1 A / div., 500 ms / div.
CH4: V_{DS}, 100 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 467.98 V, $I_{DS(MAX)}$ = 3.75 A.

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11.4 *Output Voltage Ripple*

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V X7R ceramic type and one (1) 47 μF / 25 V aluminum electrolytic KZE series from Nippon Chemi-Con. It is recommended to make the capacitor leads as short as possible so as to further reduce the magnitude of spurious signals. The aluminum electrolytic type capacitor is also polarized, so proper polarity across DC outputs must be maintained (see below).

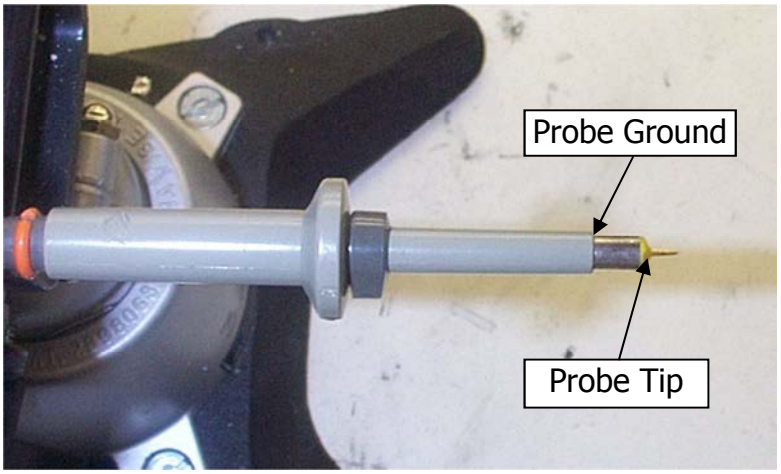

Figure 82 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

Figure 83 –Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.4.2 Measurement Results

Note: All ripple measurements were taken at the end of PCB.

11.4.2.1 100% Load Condition

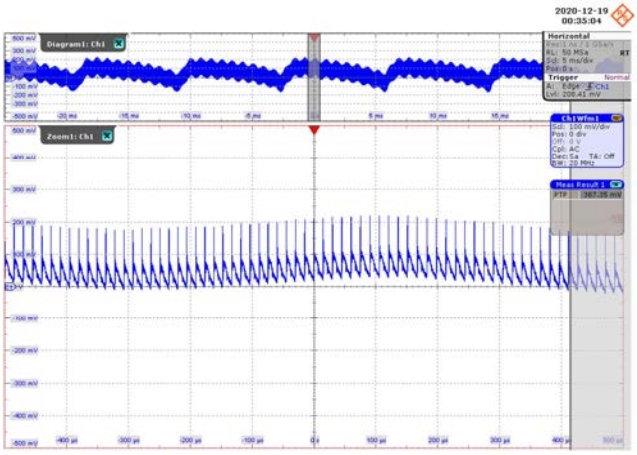

Figure 84 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 387.35 mV.

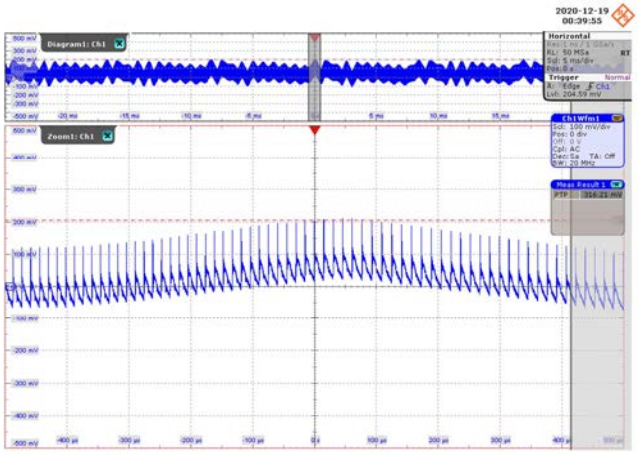

Figure 85 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 316.21 mV.

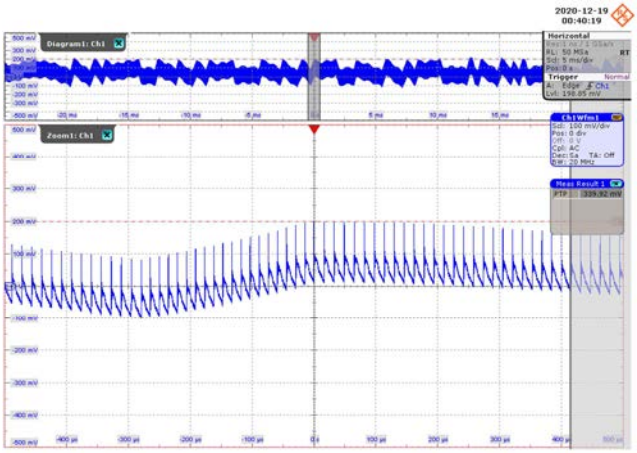

Figure 86 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 339.92 mV.

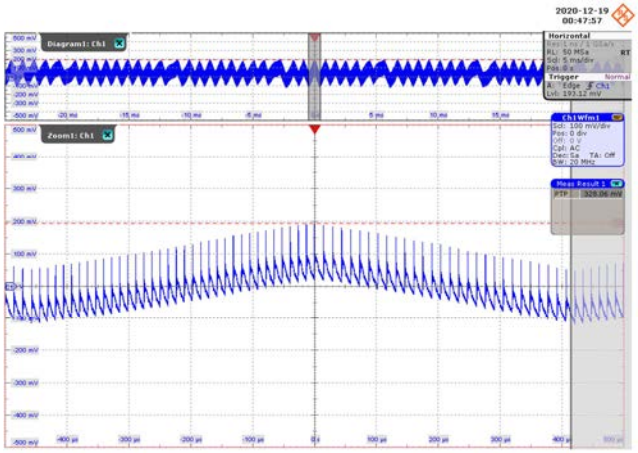

Figure 87 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 328.06 mV.

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11.4.2.2 75% Load Condition

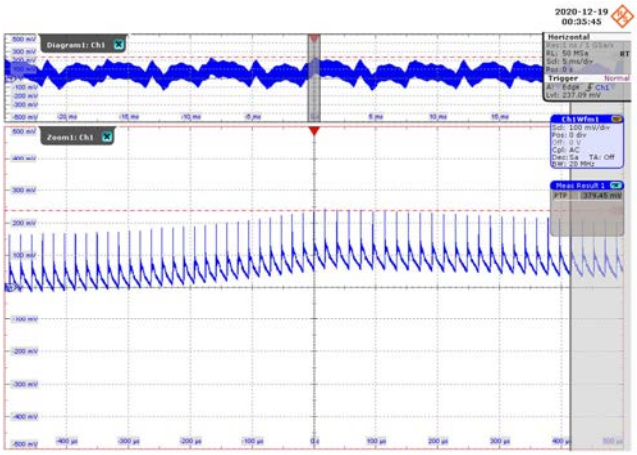

Figure 88 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 379.45 mV.

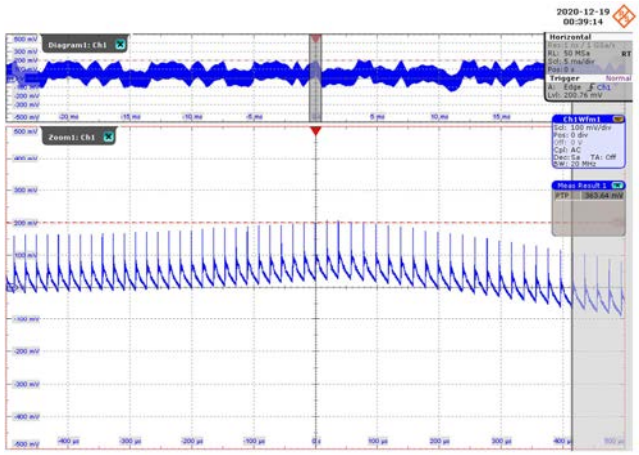

Figure 89 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 363.64 mV.

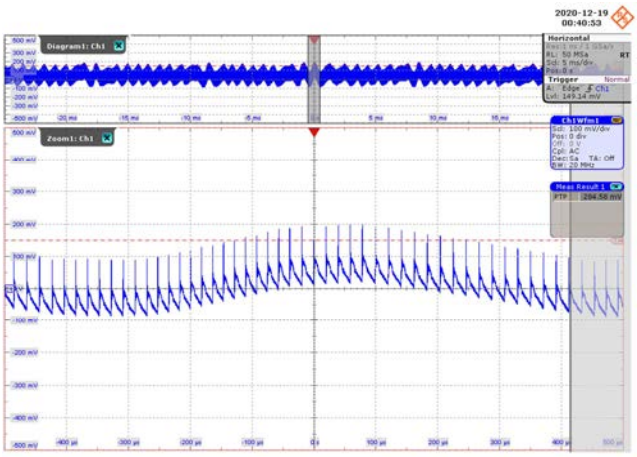

Figure 90 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 284.58 mV.

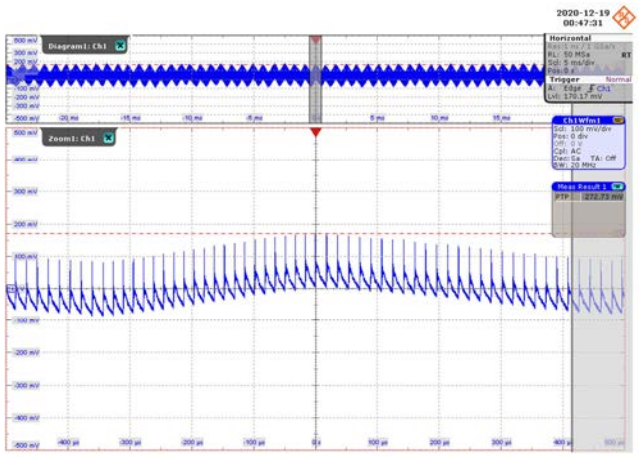

Figure 91 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 272.73 mV.

11.4.2.3 50% Load Condition

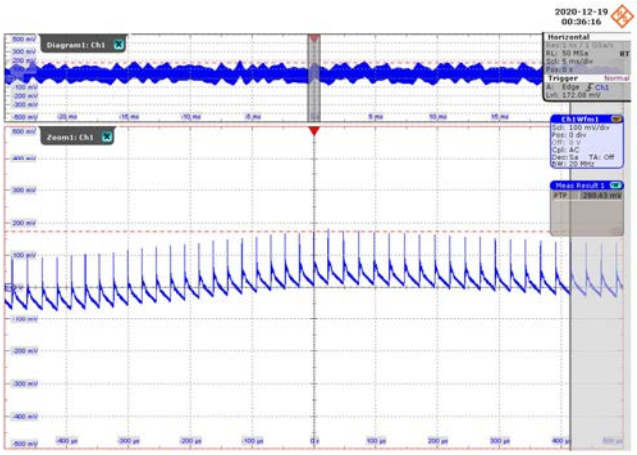

Figure 92 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 280.63 mV.

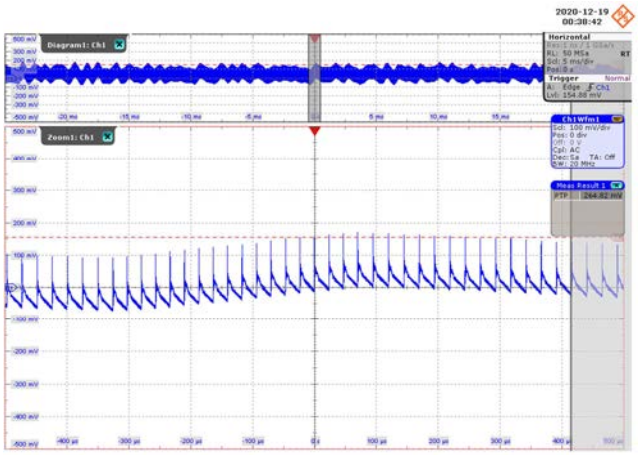

Figure 93 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 264.82 mV.

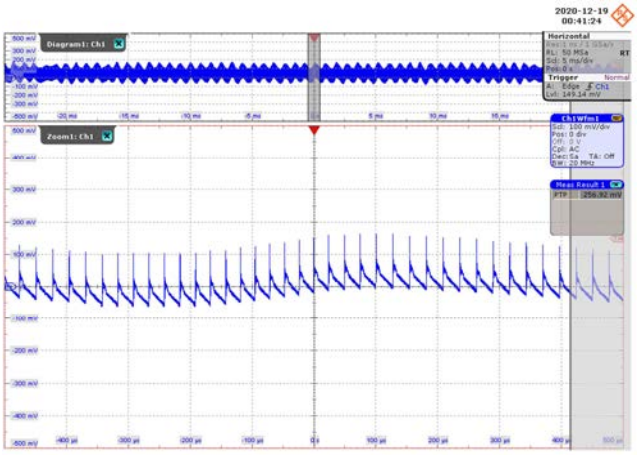

Figure 94 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 256.92 mV.

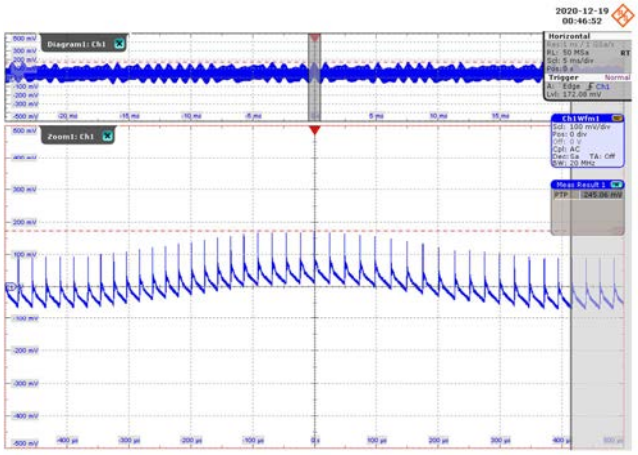

Figure 95 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 245.06 mV.

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11.4.2.4 25% Load Condition

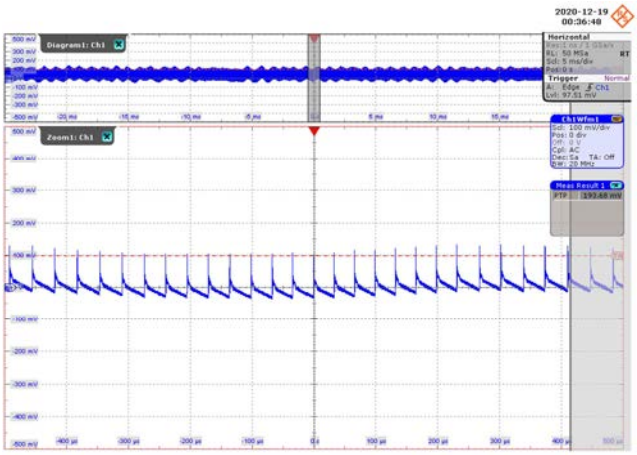

Figure 96 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 193.68 mV.

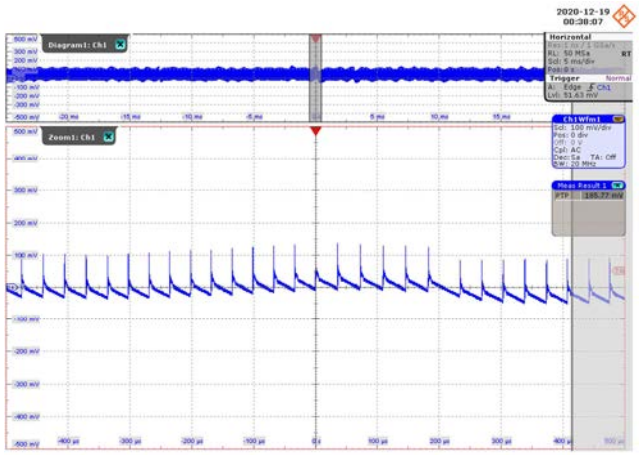

Figure 97 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 185.77 mV.

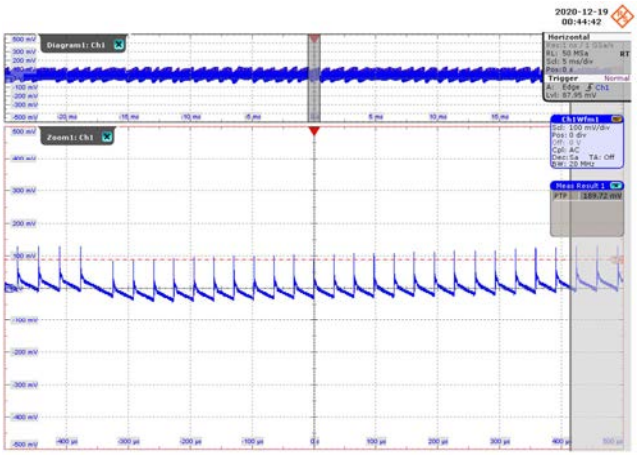

Figure 98 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 189.72 mV.

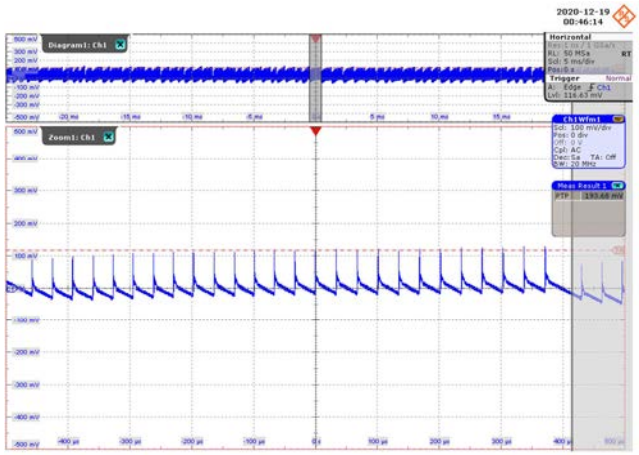

Figure 99 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 193.68 mV.

11.4.2.5 0% Load Condition

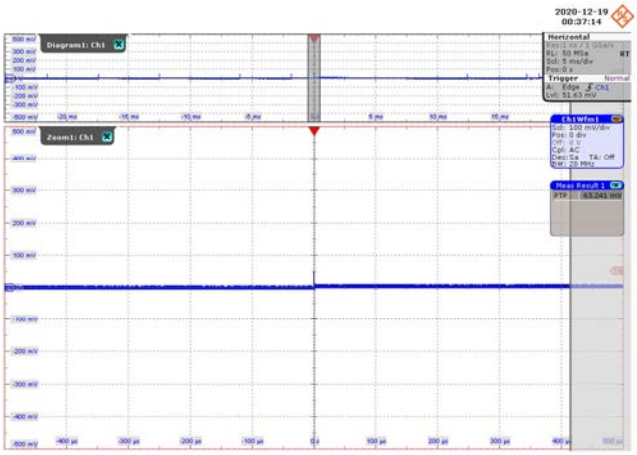

Figure 100 – 90 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 63.24 mV.

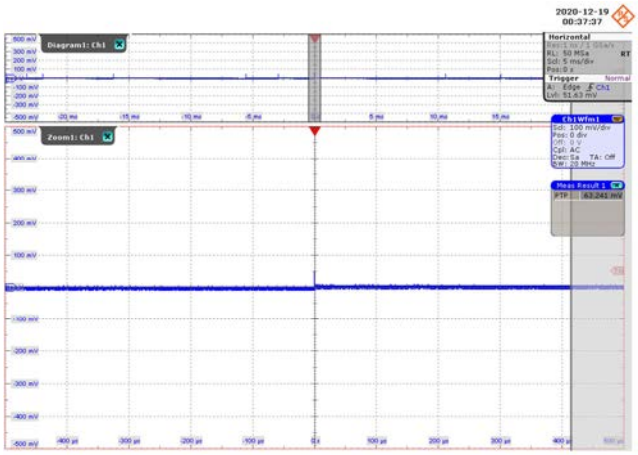

Figure 101 – 115 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 63.24 mV.

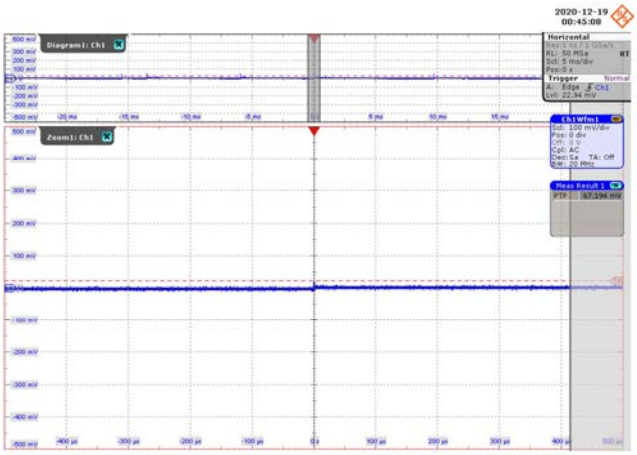

Figure 102 – 230 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 67.19 mV.

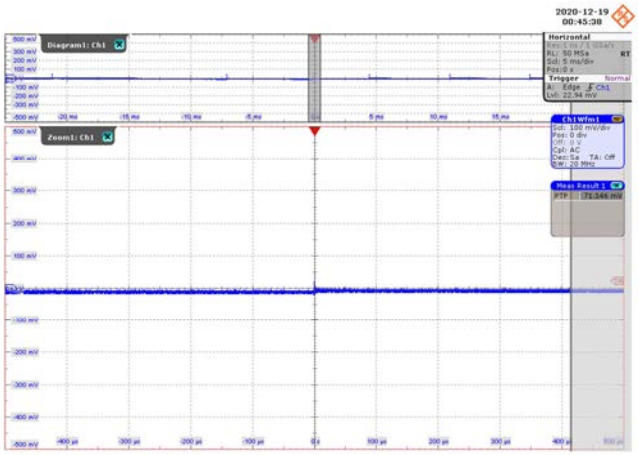

Figure 103 – 265 VAC 60 Hz.
CH1: V_{RIPPLE}, 100 mV / div., 5 ms / div.
Zoom: 100 µs / div.
Output Ripple = 71.15 mV.

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11.4.3 Output Ripple Voltage Graph from 0% - 100%

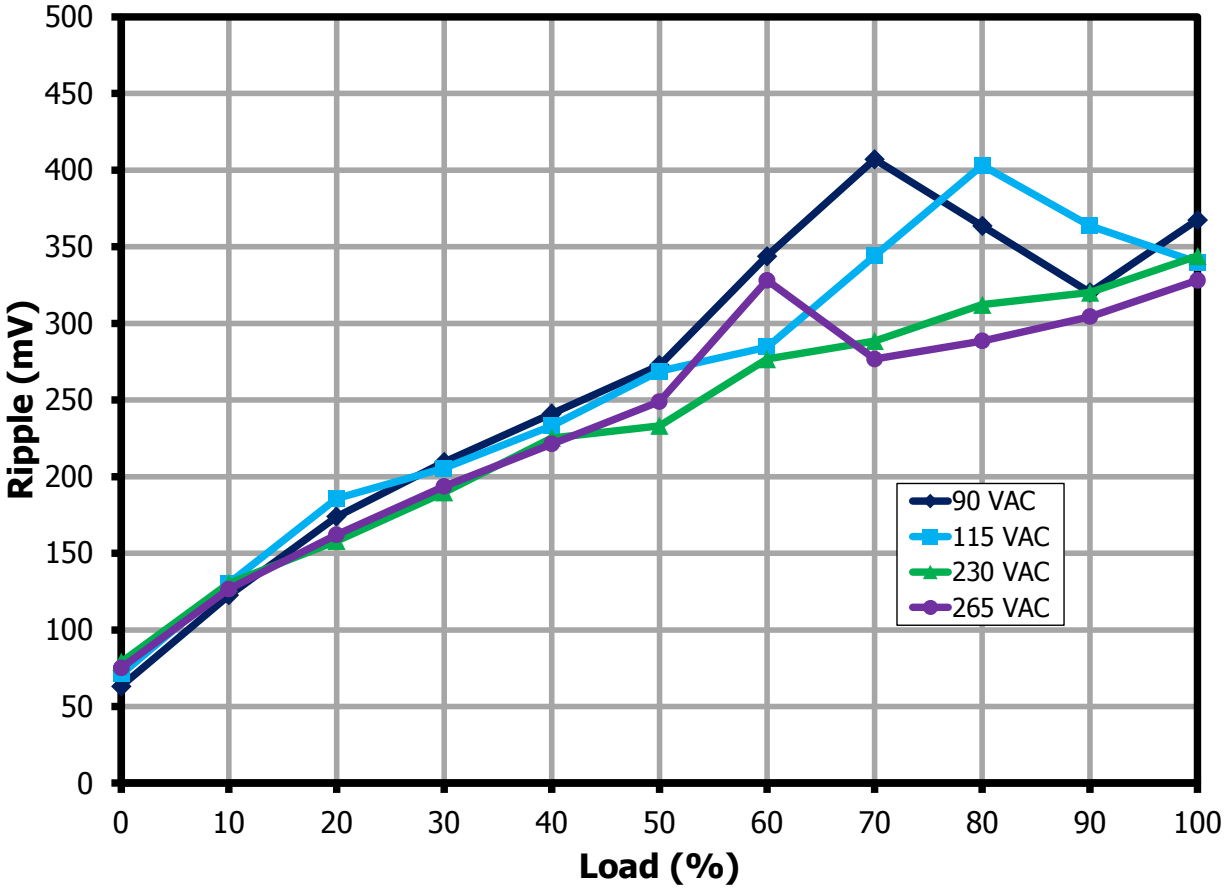

Figure 104 – Measured at the End of PCB, at Room Temperature.

12 Thermal Performance

12.1 *Test Set-Up*

Thermal evaluation was performed under two conditions: (1) room temperature and (2), 40 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for at least an hour under full load conditions.

Figure 105 – Thermal Performance Set-up Using Thermal Chamber.

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12.2 *Thermal Performance at Room Temperature*

12.2.1 90 VAC at Room Temperature

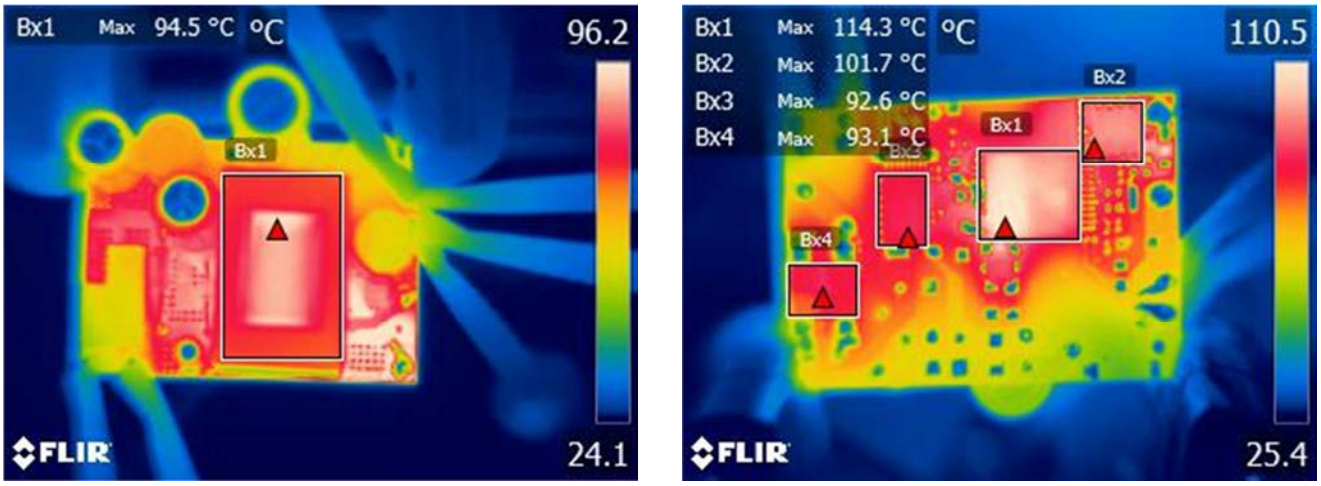

Figure 106 – Thermal Performance at 90 VAC.

Component	Temperature (°C)
Ambient	24.1
SR FET (Q1)	101.7
INN3679C (U1)	114.3
MinE-CAP (U4)	92.6
Transformer (T2)	94.5
Bridge (BR1)	93.1

12.2.2 265 VAC at Room Temperature

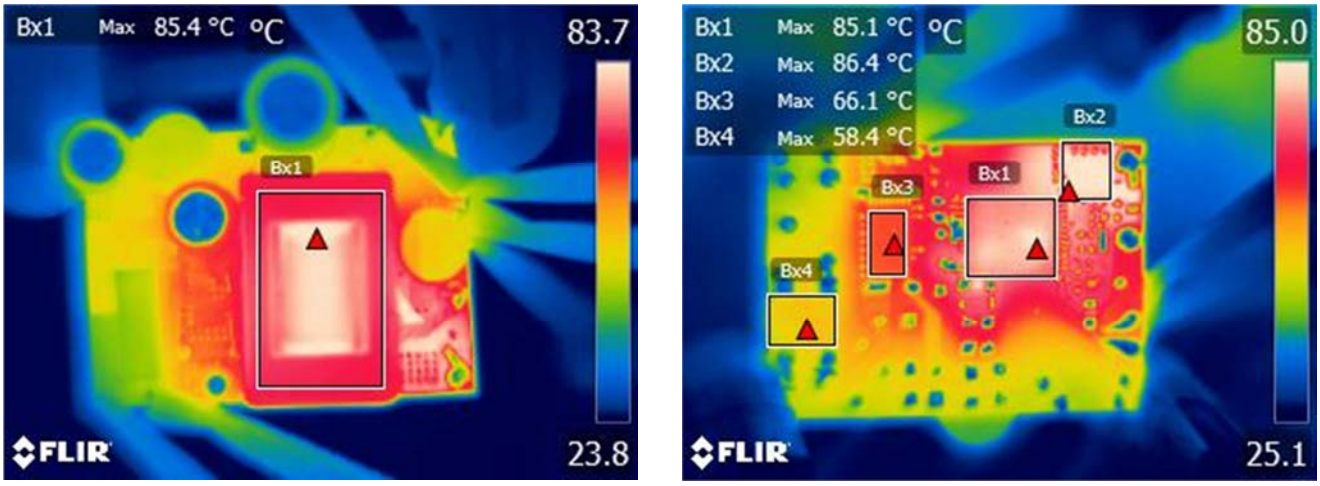

Figure 107 – Thermal Performance at 265 VAC.

Component	Temperature (°C)
Ambient	23.8
SR FET (Q1)	86.4
INN3679C (U1)	85.1
MinE-CAP (U4)	66.1
Transformer (T2)	85.4
Bridge (BR1)	58.4

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12.3 *Thermal Performance at 40 °C*

12.3.1 90 VAC at 40 °C

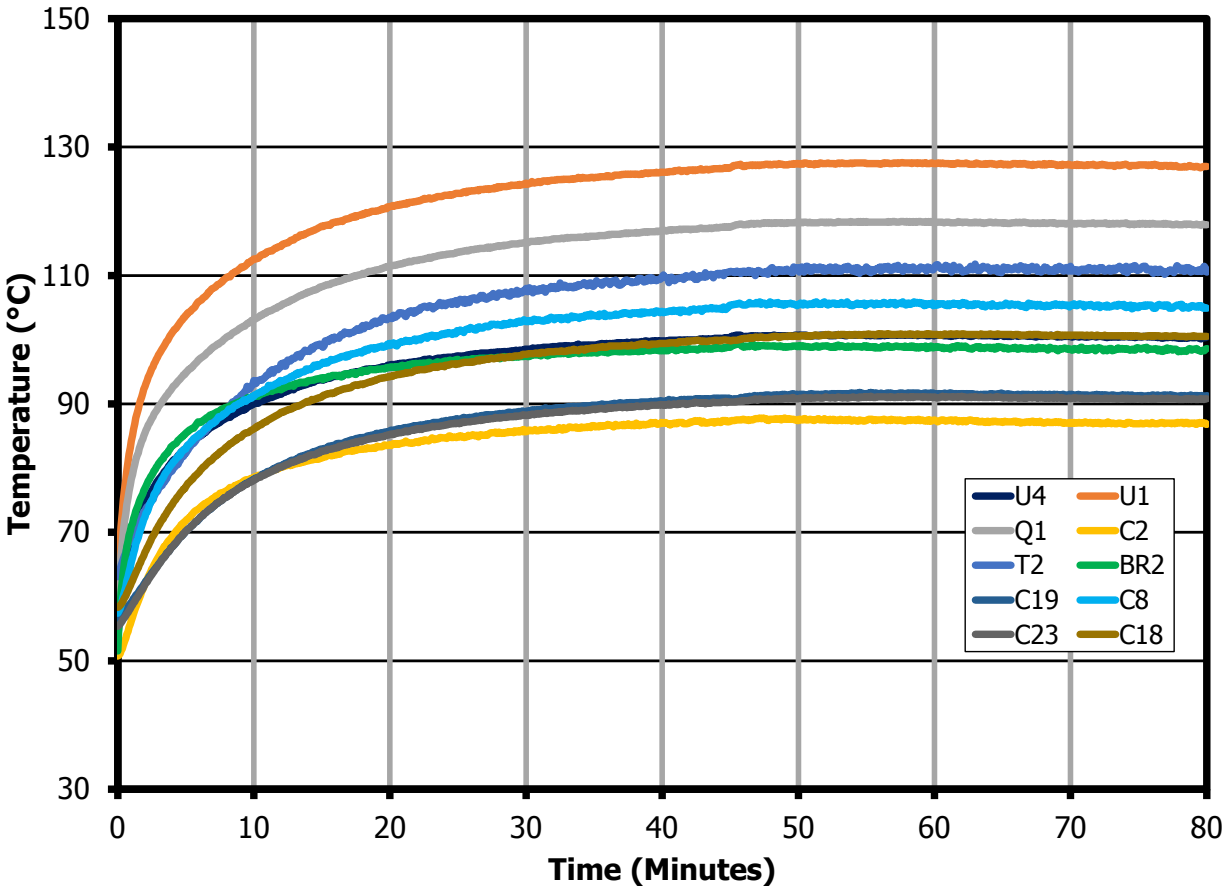

Figure 108 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	40.3
SR FET (Q1)	117.9
INN3679C (U1)	127.0
MinE-CAP (U4)	100.4
Transformer (T2)	110.5
Bridge (BR1)	98.6
HV Capacitor1 (C2)	86.8
LV Capacitor1 (C19)	91.3
Output Capacitor (C8)	104.9
HV Capacitor2 (C18)	100.5
LV Capacitor2 (C23)	90.8

12.3.2 265 VAC at 40 °C

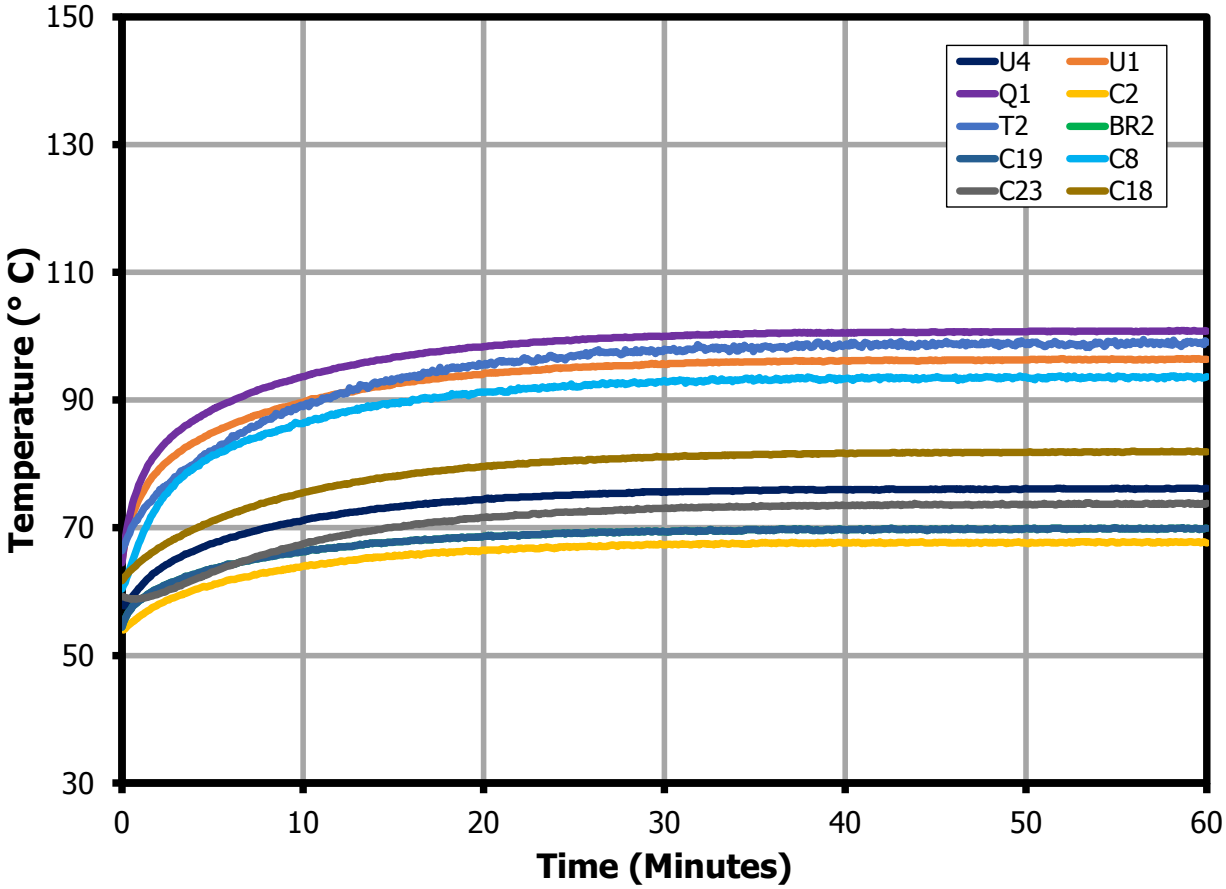

Figure 109 – Thermal Performance at 265 VAC, Full Load.

Component	Temperature (°C)
Ambient	40.1
SR FET (Q1)	100.8
INN3679C (U1)	96.4
MinE-CAP (U4)	76.2
Transformer (T2)	99.0
Bridge (BR1)	69.9
HV Capacitor1 (C2)	67.8
LV Capacitor1 (C19)	76.6
Output Capacitor (C8)	93.7
HV Capacitor2 (C18)	81.9
LV Capacitor2 (C23)	73.8

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12.3.3 90 VAC at 50 °C, Time to reach OTP: 31 minutes

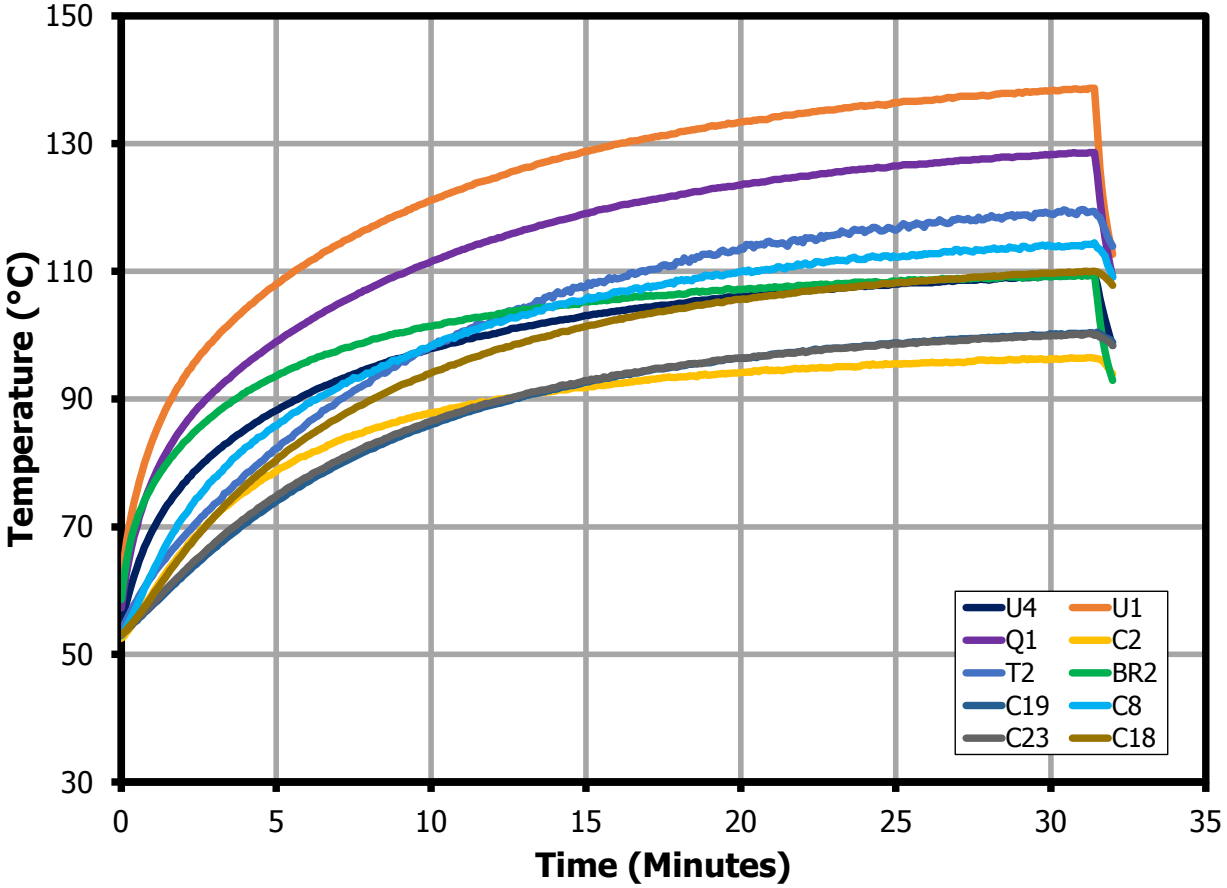

Figure 110 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	51.3
SR FET (Q1)	128.6
INN3679C (U1)	138.7
MinE-CAP (U4)	109.5
Transformer (T2)	119.4
Bridge (BR1)	109.5
HV Capacitor1 (C2)	96.4
LV Capacitor1 (C19)	100.1
Output Capacitor (C8)	114.5
HV Capacitor2 (C18)	110.0
LV Capacitor2 (C23)	100.0

12.3.4 90 VAC at 60 °C, Time to reach OTP: 15 minutes

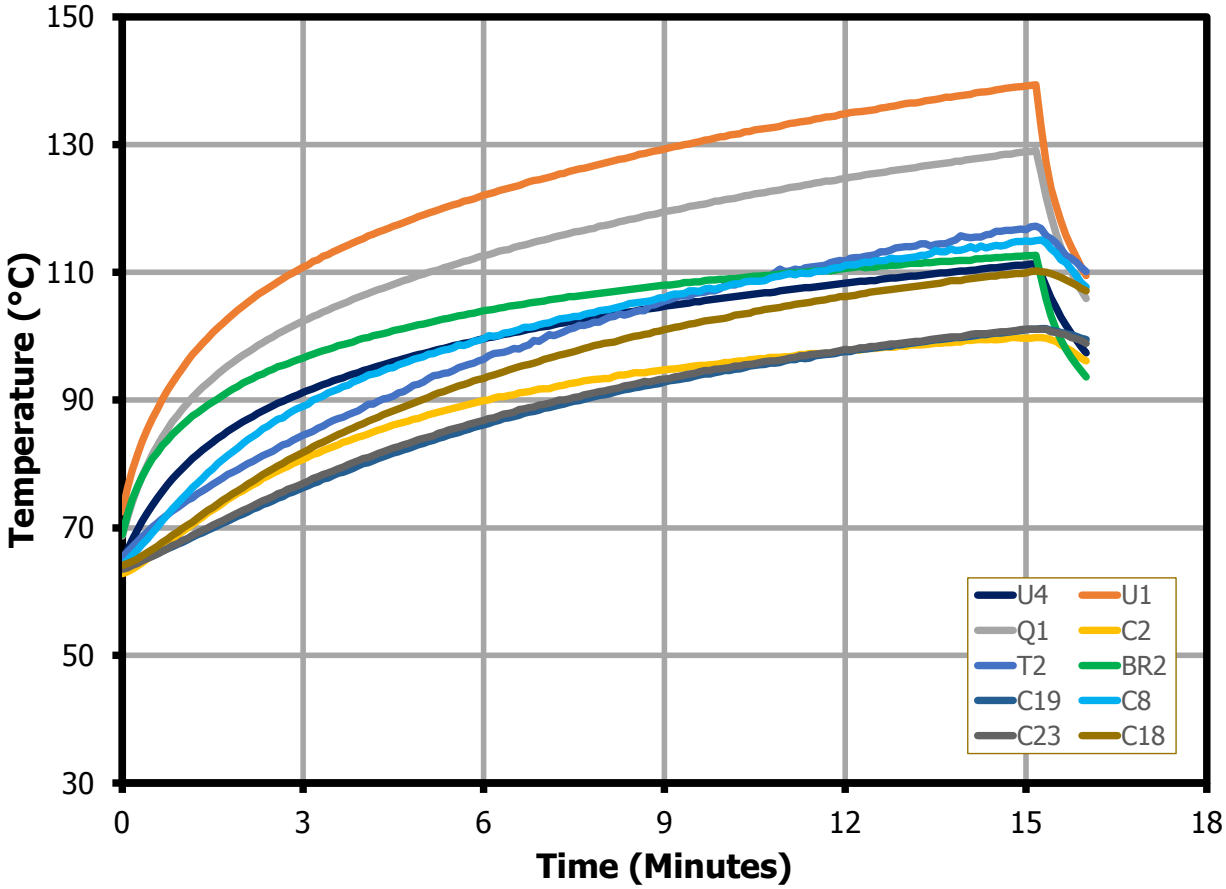

Figure 111 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	60.1
SR FET (Q1)	129.1
INN3679C (U1)	139.4
MinE-CAP (U4)	111.3
Transformer (T2)	117.2
Bridge (BR1)	112.7
HV Capacitor1 (C2)	99.8
LV Capacitor1 (C19)	101.1
Output Capacitor (C8)	115.0
HV Capacitor2 (C18)	110.2
LV Capacitor2 (C23)	101.1

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13 Conducted EMI

13.1 *115 VAC 3.25 A Resistive Load*

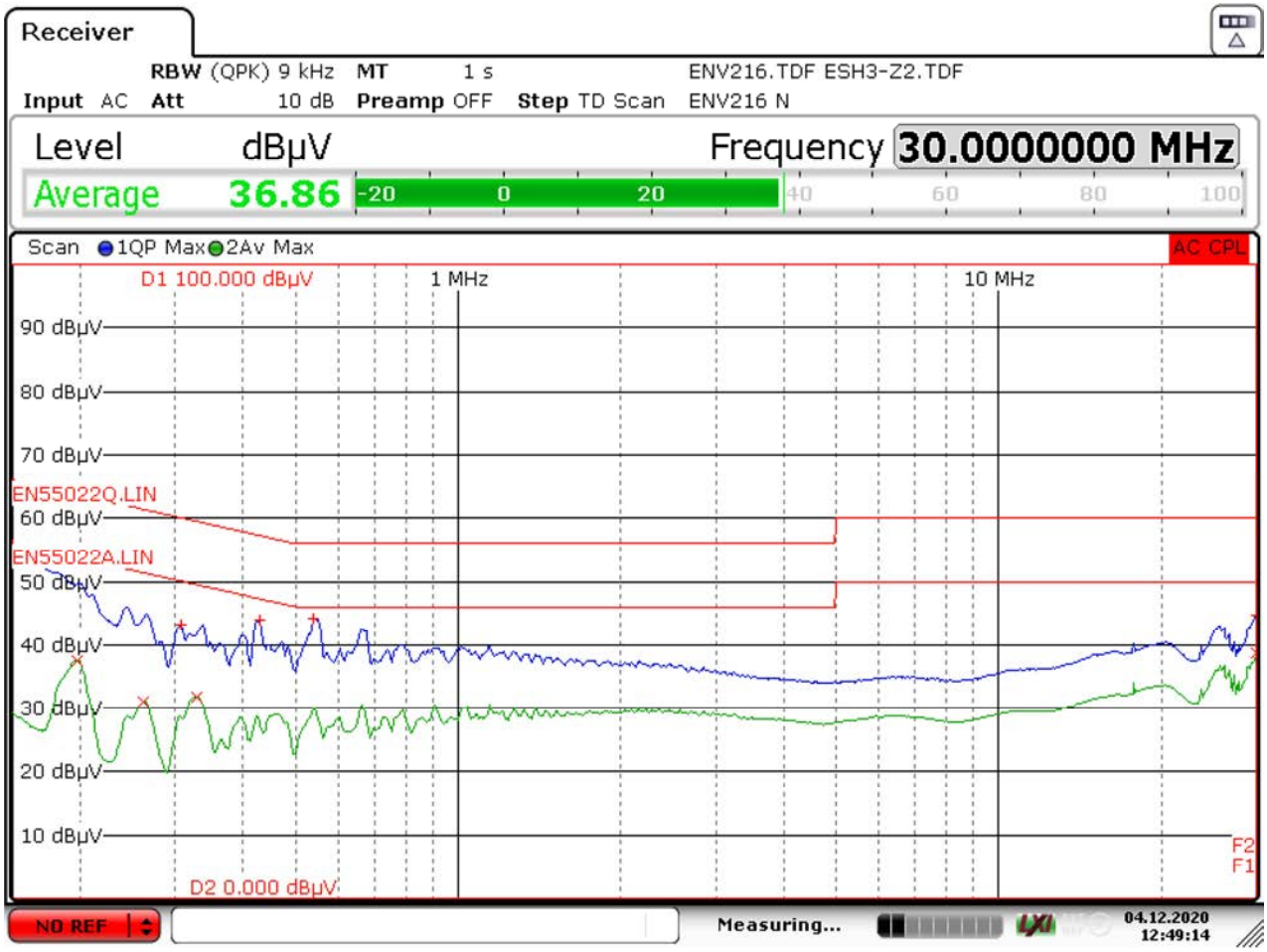

Figure 112 – Floating Ground EMI at 115 VAC.

13.2 ***230 VAC 3.25 A Resistive Load***

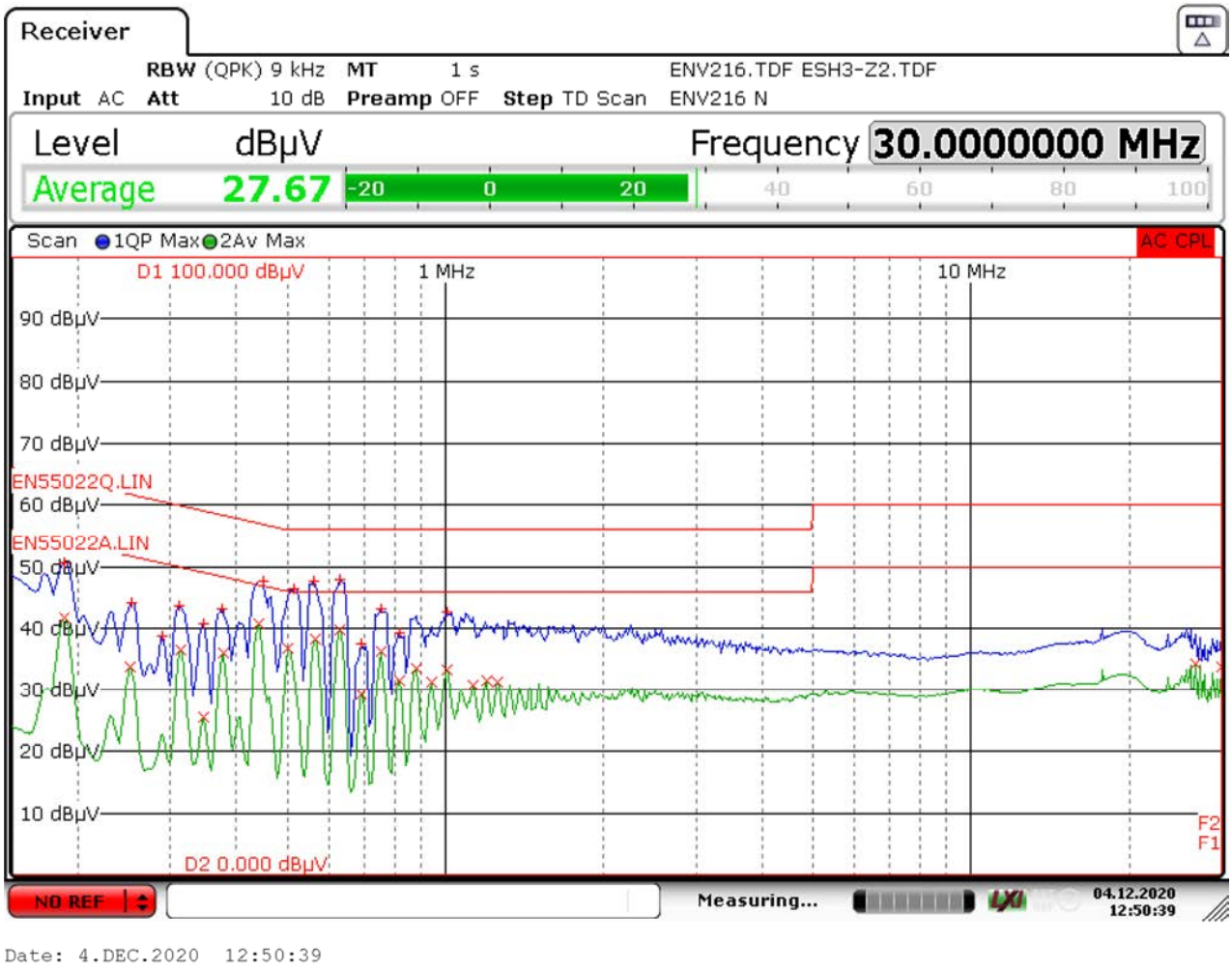

Figure 113 – Floating Ground EMI at 230 VAC.

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14 Line Surge

Differential input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

14.1 *Differential Mode Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

14.1.1 1000 V 90º Differential Mode Surge

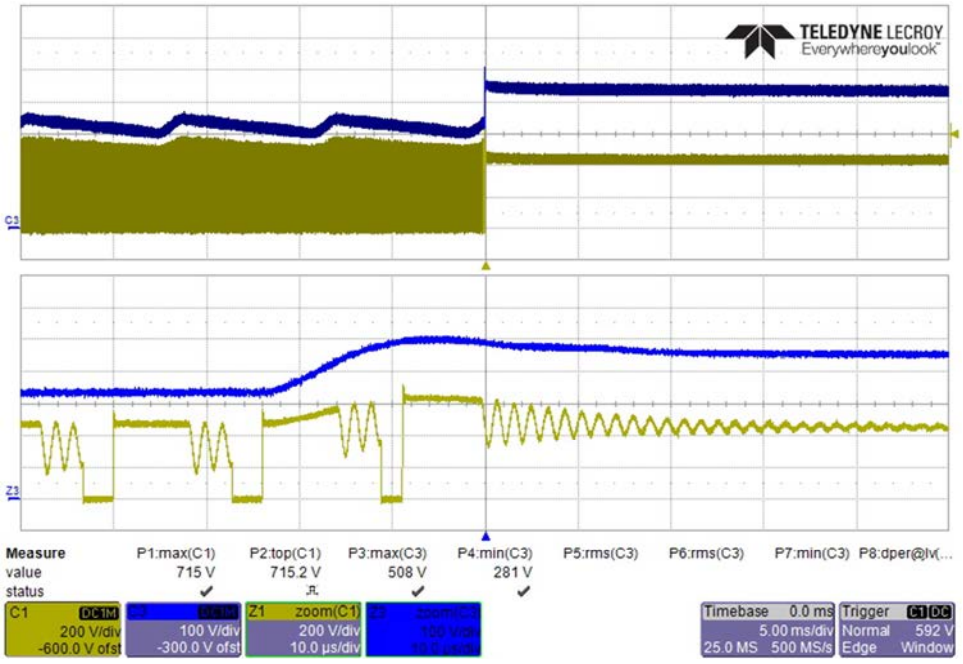

Figure 114 – Drain Voltage and Bulk Voltage (C18), 230 VAC, Full Load.

14.1.2 -1000 V 270º Differential Mode Surge

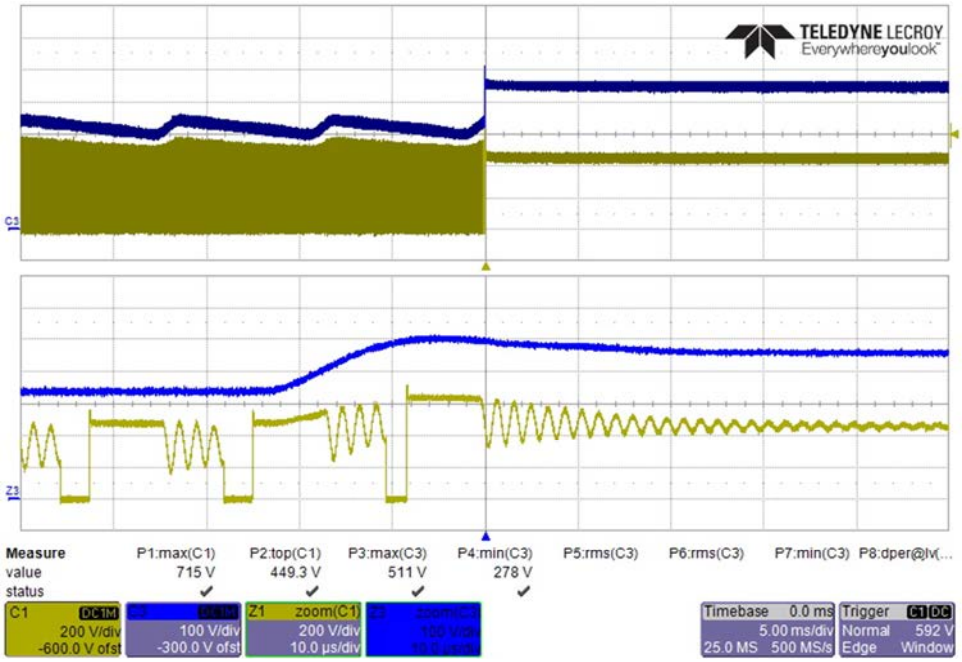

Figure 115 – Drain Voltage and Bulk Voltage (C18), 230 VAC, Full Load.

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15 ESD

Note: ESD performance was tested on limited number of units. All ESD strikes were applied at end of cable.

Passed ±8 kV contact discharge.

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
+8	VOUT	10	Pass
	GND	10	Pass
-8	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage observed.

Passed ±15 kV Air discharge.

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+15	VOUT	10	Pass
	GND	10	Pass
-15	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage was observed.

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
25-Mar-21	VRA	1.0	Initial Release.	Apps & Mktg

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